# uMCP Specification

## 64GB UFS
## + 4GB LPDDR4X

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## Document Title

uMCP
64GB UFS Flash / 4GB LPDDR4X

## Revision History

| Rev No. | History | Draft Date | Remark |
|---|---|---|---|
| 1.0 | Final Version | Sep 2020 | |
| 1.1 | Updated UFS Spec - Power Down Sequence<br>2.2.5 Vcc Power Down Sequence<br>2.2.6 Vccq2 Power Down Sequence | Dec 2020 | |
| 1.2 | Updated Jedec D version<br>Updated Clock timings | Sep 2021 | |

# Features

**[ uMCP ]**

● Operation Temperature

- (-25)°C ~ 85°C

● Package

- 254-ball FBGA
- Lead & Halogen Free

**[ UFS ]**

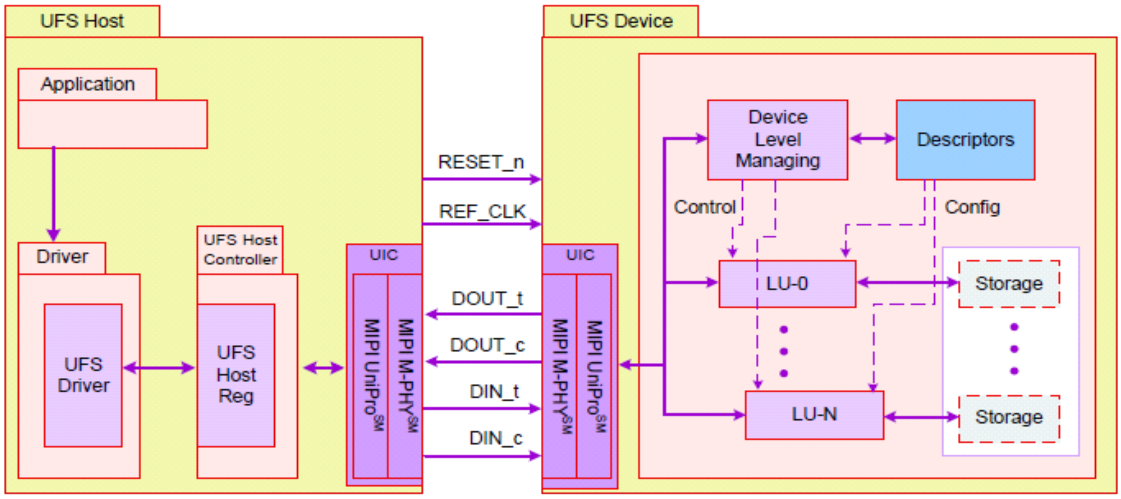
- **UFS2.2 compatible**
  - backward compatibility with UFS2.0/UFS2.1
- **Operating Voltage Range**
  - $V_{cc}$ (NAND) : 2.7V - 3.6V
  - $V_{ccq}$ (CTRL) : Not Used
  - $V_{ccq2}$ (CTRL) : 1.7V - 1.95V
- **Temperature**
  - Operation Temperature (-25℃ ~ +85℃)
  - Storage Temperature (-40℃ ~ +85℃)
- **Reference**
  - JEDEC UFS Specification V2.2
  - MIPI UniPro Specification V1.61
  - MIPI M-PHY Specification V3.0
  - JEDEC UFS HPB Extension v1.0
- **Supported Features**
  - Erase / Discard / Purge / Wipe
  - PWM G1~G4 / HS-G1~G3
  - 1L/2L
  - Command Queuing / Cache
  - RPMB / BOOT LU
  - Power-on/HW/EndPoint/LU Reset
  - BKOP
  - High Priority LU
  - Reliable Write Operation
  - Write Protect, Secure Write Protect
  - Task Management operations
  - Secure Removal Type
  - Power Management operations
  - MAX 32 LU supported
  - Device Health Descriptor
  - Field Firmware Update
  - Host Performance Booster (HPB)
  - WriteBooster

**[ LPDDR4X ]**

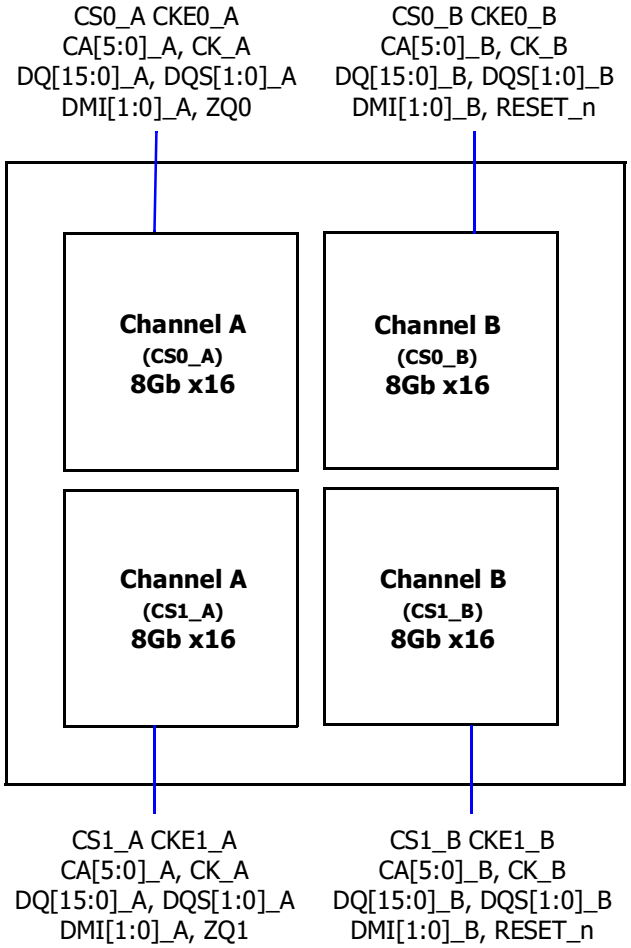
- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2 = 1.1V (1.06V to 1.17V)
- VDDQ = 0.6V (0.57V to 0.65V)
- Programmable CA ODT and DQ ODT with VSSQ termination
- VOH compensated output driver
- Single data rate command and address entry
- Double data rate architecture for data Bus;
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS
- Auto refresh and self refresh supported
- All bank auto refresh and directed per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- Background ZQ Calibration

## Functional Block Diagram

### UFS Block Diagram

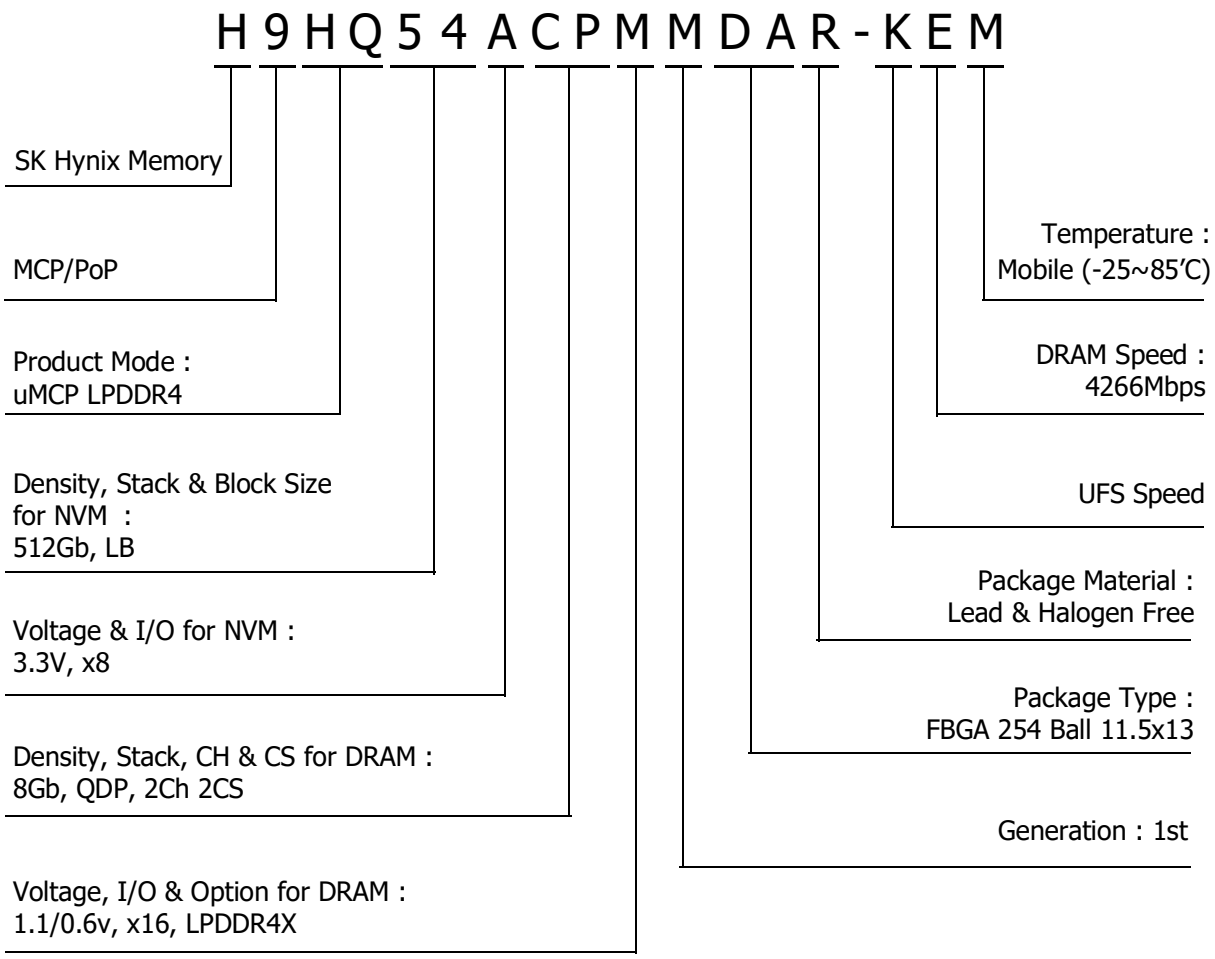



### DRAM

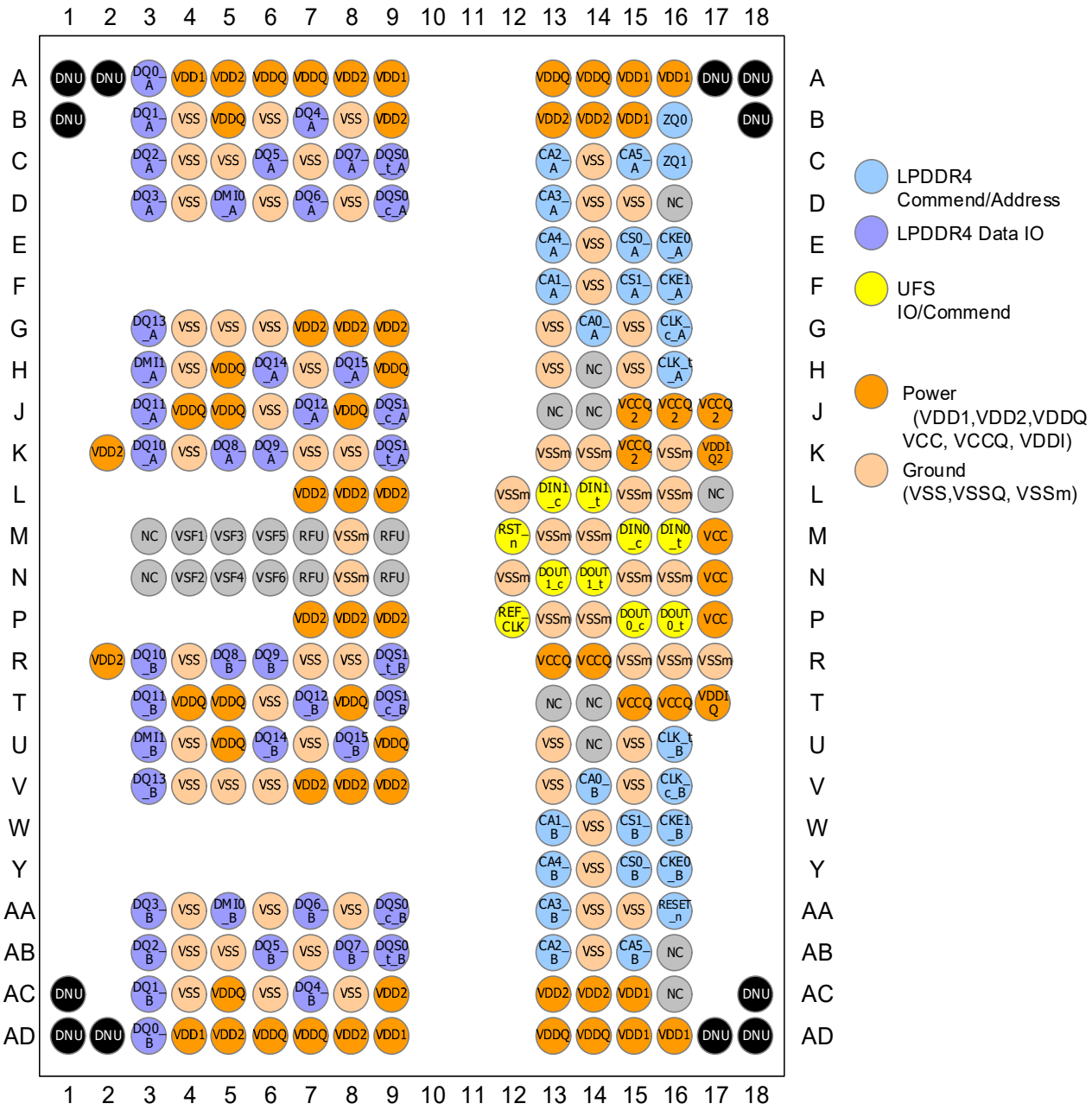


## Ordering Information

| Part Number | Memory Combination | Operation Voltage | Density | Speed | Package |
|---|---|---|---|---|---|
| H9HQ54ACPMMDAR-KEM | UFS<br>LPDDR4X | 3.3V<br>1.1V/0.6V | 64GB (x8)<br>4GB (x16) | 4266Mbps | 254Ball FBGA<br>(Lead & Halogen Free) |



## Ball ASSIGNMENT




*Top View* *254ball MCP*

## UFS Pin Description

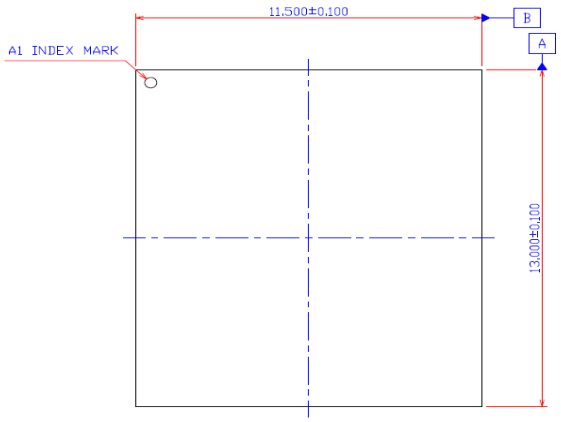
| Name | Type | Description |
|---|---|---|
| $V_{cc}$ | Supply | 3.3V supply voltage for the memory devices |
| $V_{ccq}$ | Supply | 1.2V supply voltage for the memory controller<br>Not used internally for SK hynix's UFS2.2 |
| $V_{ccq2}$ | Supply | 1.8V supply voltage for the memory controller |
| VDDi | Input | Input terminal to provide bypass capacitor for internal regulator.<br>No need to connect external capacitor. Not used internally |
| VDDiQ | Input | Input terminal to provide bypass capacitor for internal regulator.<br>No need to connect external capacitor. |
| VDDiQ2 | Input | Input terminal to provide bypass capacitor for internal regulator.<br>Connect 1µF capacitor from VDDiQ2 to ground. |
| Vss | Supply | Supply voltage ground |
| RST_n | Input | Input hardware reset signal. This is an active low signal. |
| REF_CLK | Input | Input reference clock |
| DIN0_t<br>DIN0_c | Input | Downstream data lane 1. Differential input signals into UFS device from the host. DIN0_t is the positive node of the differential signal pair. |
| DIN1_t/<br>DIN1_c | Input | Downstream data lane 2.<br>Differential input signals into UFS device from the host. |
| DOUT0_t/<br>DOUT0_c | Output | Upstream data lane 1.<br>Differential output signals from the UFS device to the host.<br>DOUT0_t is the positive node of the differential signal pair. |
| DOUT1_t/<br>DOUT1_c | Output | Upstream data lane 2.<br>Differential output signals from the UFS device to the host. |
| C+/C- | Input | Optional charge pump capacitor terminal.<br>Not used internally for SK hynix's UFS2.2 |
| CPOUT1/<br>CPOUT2 | Input | Optional charge pump output capacitor terminal.<br>Not used internally for SK hynix's UFS2.2 |
| NC | Input | No connect |
| RFU | - | Reserved for Future Use |
| VSF | - | Vendor Specific Function. |

## DRAM Pin Description

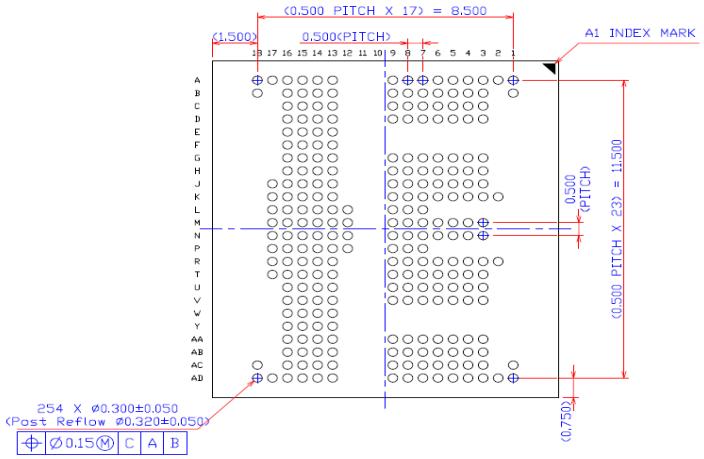
| Symbol | Type | Description |
|---|---|---|
| CK_t_A, CK_c_A<br>CK_t_B, CK_c_B | Input | **Clock :** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair. |
| CKE_A<br>CKE_B | Input | **Clock Enable :** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal. |
| CS_A<br>CS_B | Input | **Chip Select :** CS is part of the command code. Each channel (A & B) has its own CS signal. |
| CA[5:0]_A,<br>CA[5:0]_B | Input | **Command / Address Inputs :** Provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals. |
| ODT_CA_A<br>ODT_CA_B | Input | **CA ODT Control :** The ODT_CA pin is ignored by LPDDR4x devices. ODT-CS /CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS |
| DQ[15:0]_A,<br>DQ[15:0]_B | I/O | **Data Input / Output :** Bi-direction data bus. |
| DQS[1:0]_t_A,<br>DQS[1:0]_c_A,<br>DQS[1:0]_t_B,<br>DQS[1:0]_c_B | I/O | **Read Strobe :** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes. |
| DMI[1:0]_A,<br>DMI[1:0]_B | I/O | **Data Mask Inversion :** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting. |
| ZQ | Reference | **Calibration Reference :** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor. |
| VDD1, VDD2, VDDQ | Supply | **Power Supplies :** Isolated on the die for improved noise immunity. |
| VSS | GND | **Ground Reference :** Power supply ground reference. |
| RESET_n | Input | **RESET :** When asserted LOW, the RESET pin resets both channels of the die. |

## Package Information

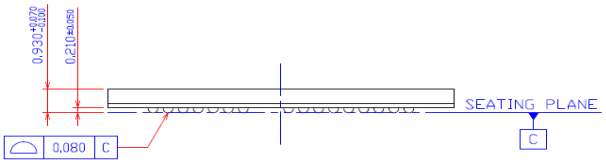
254 Ball 0.5mm pitch 11.5mm x 13.0mm FBGA [t = 1.0mm max]




TOP VIEW




BOTTOM VIEW




FRONT VIEW

# UFS2.2 3D-V6

(64GB-256GB)

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## Revision History

| Rev No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.1 | Preliminary version | Feb 2020 | Preliminary |
| 1.0 | Update v1.0 Version | Mar 2020 | |
| 1.1 | Update Connection Guide specification (13page)<br>1) VCCQ2(1.8v), C3: Min 2.2 --> 4.7<br>2) VDDiQ, CVDDIQ : Min 1 --> 0 | Jun 2020 | |
| 1.2 | Update 64GB Performance (14page)<br>1) Read 830 --> 890MB/s<br>2) Write (Write-Booster On) 410 --> 450MB/s | Aug 2020 | |
| 1.3 | Update 64GB dWriteBoosterBufferMaxNAllocUnits (37page)<br>0400h --> 0C00h | Sep 2020 | |
| 1.4 | Update Power Down Sequence<br>2.2.5 Vcc Power Down Sequence<br>2.2.6 Vccq2 Power Down Sequence | Dec 2020 | |

# 1. SK hynix UFS Introduction

## 1.1. General Description

SK hynix UFS product consists of NAND flash and UFS controller.
UFS has the built-in intelligent controller which manages interface protocols, wear leveling, bad block management, garbage collection, and ECC. The first UFS of SK hynix is compatible with JEDEC standard UFS2.2 specification and supports UniPro v1.61 and M-PHY v3.0 (HS-G1/G2/G3 Rate A/B, PWM-G1/G2/G3/G4, Dual-lane).

## 1.2. Key Features

- **UFS2.2 compatible**
  - backward compatibility with UFS2.0/UFS2.1

- **Operating Voltage Range**
  - $V_{cc}$ (NAND) : 2.7V - 3.6V
  - $V_{ccq}$ (CTRL) : Not Used
  - $V_{ccq2}$ (CTRL) : 1.7V - 1.95V

- **Temperature**
  - Operation Temperature (-25℃ ~ +85℃)
  - Storage Temperature (-40℃ ~ +85℃)

- **Reference**
  - JEDEC UFS Specification V2.2
  - MIPI UniPro Specification V1.61
  - MIPI M-PHY Specification V3.0
  - JEDEC UFS HPB Extension v1.0

- **Supported Features**
  - Erase / Discard / Purge / Wipe
  - PWM G1~G4 / HS-G1~G3
  - 1L/2L
  - Command Queuing / Cache
  - RPMB / BOOT LU
  - Power-on/HW/EndPoint/LU Reset
  - BKOP
  - High Priority LU
  - Reliable Write Operation
  - Write Protect, Secure Write Protect
  - Task Management operations
  - Secure Removal Type
  - Power Management operations
  - MAX 32 LU supported
  - Device Health Descriptor
  - Field Firmware Update
  - Host Performance Booster (HPB)
  - WriteBooster

## 1.3. Connection Guide

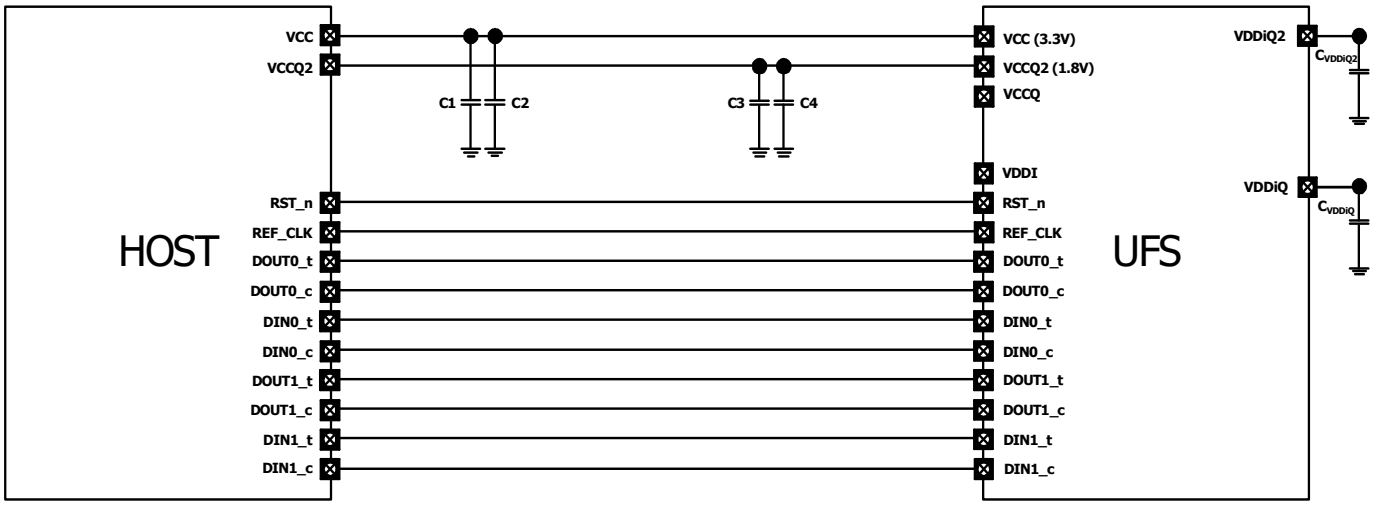


**Figure 1 - Connection Guide Diagram**

- If host does not support 2nd lane, then make 2nd signal line(DIN1_t, DIN1_C, DOUT1_t, DOUT1_C) float.

**Table 1 - Connection Guide Specification**

**[Unit : µF]**

| Parameter | Symbol | Min | Max | Recommend | Remark |
|---|---|---|---|---|---|
| $V_{cc}$ (3.3V) | $C_1$ | 4.7 | 10 | 4.7 | Capacitor should be connected with $V_{cc}$ and Vss as close as possible |
| | $C_2$ | 0.1 | 1 | 0.1 | |
| $V_{ccq2}$ (1.8V) | $C_3$ | 4.7 | 10 | 4.7 | Capacitor should be connected with $V_{ccq2}$ and Vss as close as possible |
| | $C_4$ | 0.1 | 1 | 0.1 | |
| VDDiQ | $C_{VDDiQ}$ (Optional) | 0 | 4.7 | 1 | Capacitor should be connected with $V_{DDiQ}$ and $V_{SS}$ as close as possible<br>The connection of $C_{VDDiQ}$ capacitor that would be nice to have |
| VDDiQ2 | $C_{VDDiQ2}$ | 1 | 4.7 | 1 | Capacitor should be connected with $V_{DDiQ2}$ and $V_{SS}$ as close as possible |

# 2. UFS Characteristics

## 2.1. Performance

| Density | Sequential (MB/s) | | Test Condition |
|---|---|---|---|
| | Read | Write (Write-Booster On/Off) | |
| 64GB | 540 | 410/140 | HS-G3B 1L Fast Mode |
| 128GB | 540 | 450/250 | |
| 256GB | 540 | 450/400 | |
| 64GB | 890 | 450/140 | HS-G3B 2L Fast Mode |
| 128GB | 1000 | 700/250 | |
| 256GB | 1000 | 850/400 | |

- Device level test without file system overhead.
- Queue depth 8
- Seq. Chunk size: 512KB
- Enabled feature: Cache on

## 2.2. Power

UFS Power Mode Management

| UFS Power Mode | Unipro Power Mode | M-PHY Power Mode | $V_{cc}$ Power | $V_{ccq2}$ Power |
|---|---|---|---|---|
| Active | FAST_STATE | HS-BURST | On | On |
| Idle | SLEEP_STATE | STALL | On | On |
| Hibernate | HIBERNATE_STATE | HIBERN8 | On | On |
| Sleep | HIBERNATE_STATE | HIBERN8 | Off[1)] | On |
| PowerDown | OFF_STATE | UNPOWERED | Off[1)] | Off[1)] |

Notes
1. Host may turn off the power for power consumption reduction.

### 2.2.1. Active Power Mode

| | Density | Room Temperature = 25℃ | |
|---|---|---|---|
| | | $I_{CC}$ | $I_{CCQ2}$ |
| HS-G3-1L | 256GB (4x512Gb) | 250mA | 350mA |
| HS-G3-2L | | 250mA | 450mA |

- $V_{cc}$ = 3.3V, $V_{ccq2}$ = 1.8V, $V_{ccq}$ Not Used Internally
- HS-G3B 1L/2L Fast Mode, Not 100% tested
- The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

### 2.2.2. Hibernate Power Mode

| Density | HS Gear3 x 1 lane | | HS Gear3 x 2 lane | |
|---|---|---|---|---|
| | $I_{CC}$ (3.3v) [1)] | $I_{CCQ2}$ (1.8v) [1)] | $I_{CC}$ (3.3v) [2)] | $I_{CCQ2}$ (1.8v) [2)] |
| 256GB (4x512Gb) | 150uA | 570uA | 150uA | 570uA |

- Host shall issue "HIBERN8 Enter" to enter hibernate power mode. Room Temperature 25'C over a period of 100ms

Notes
1. Not 100% tested, Typical Value.
2. The measurement for max RMS current is the average RMS current consumption over a period 100ms

### 2.2.3. Sleep Power Mode

| Density | HS Gear3 x 1 lane | | HS Gear3 x 2 lane | |
|---|---|---|---|---|
| | $I_{CC}$ (3.3v) [1] | $I_{CCQ}$ (1.8v) [1] | $I_{CC}$ (3.3v) [2] | $I_{CCQ2}$ (1.8v) [2] |
| 256GB (4x512Gb) | 0uA | 570uA | 0uA | 570uA |

- Host shall issue SSU(Sleep) and "HIBERN8 Enter" to enter Sleep, Room Temperature 25'C over a period of 100ms
- $V_{cc}$ Off ($V_{cc}$ = 0V)

Notes
1. Not 100% tested, Typical Value
2. The measurement for max RMS current is the average RMS current consumption over a period 100ms

### 2.2.4. UFS Power Mode Transition Diagram

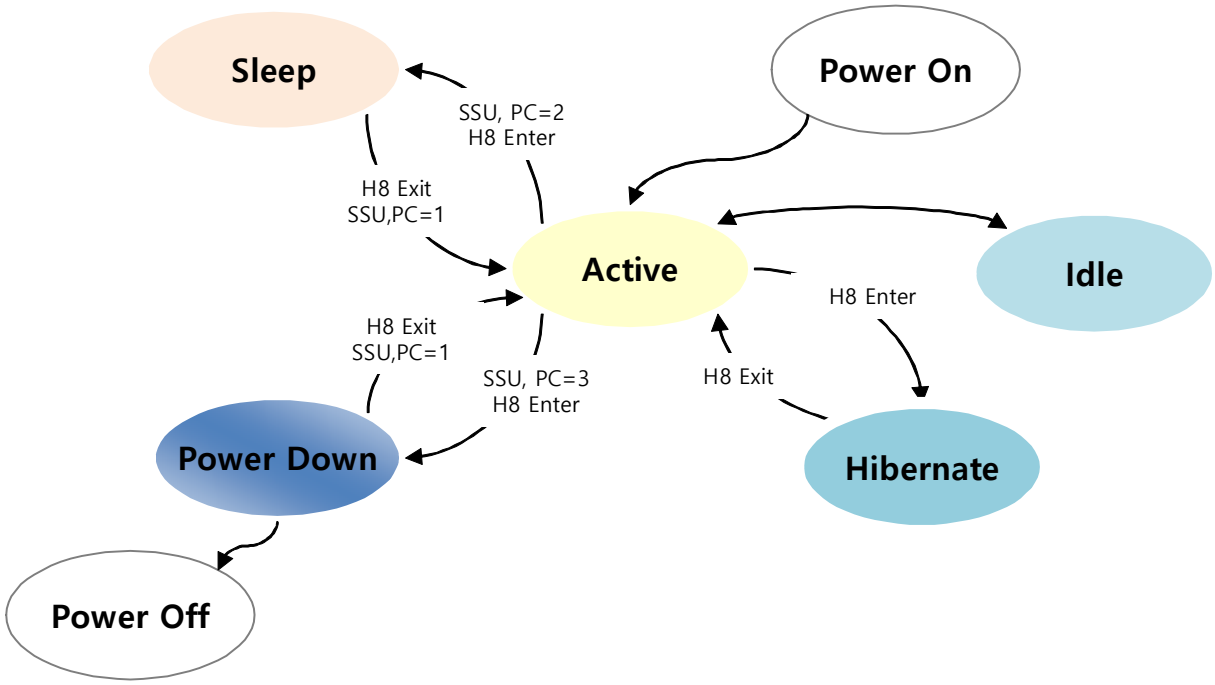


**Figure 2 - Power Mode State**

- Host shall issue "Hibern8 enter" to enter hibernate power mode.
- In Sleep power mode, $V_{cc}$ may be turned off to reduce power consumption.
- Both $V_{cc}$ and $V_{ccq2}$ may be turned off at PowerDown mode.

### 2.2.5. VCC Power Down Sequence




- Once Vcc drops under 2.0v, it shall be driven down Vcc to below 0.5v and stay low for at least 1ms before Vcc powered up

### 2.2.6. VCCQ2 Power Down Sequence




- Once Vccq2 drops under 1.1v, it shall be driven down Vccq2 to below 0.2v and stay low for at least 1ms before Vccq2 powered up

## 2.3. Temperature & Humidity

### 2.3.1. Temperature Condition

| Density | Temperature | Remark |
|---|---|---|
| Operation Temperature[1)] | -25℃ ~ 85℃ | - |
| Storage Temperature | -40℃ ~ 85℃ | - |

Notes
1. The operating temperature is the UFS case surface temperature on the center of top side of the case

### 2.3.2. Humidity Condition

| Density | Humidity | Remark |
|---|---|---|
| Operation Humidity | 0% RH ~ 95% RH (Non-Condensing) | - |
| Storage Humidity | 0% RH ~ 95% RH (Non-Condensing) | - |

## 2.4. Bandwidth

| Bandwidth | Description | Remark |
|---|---|---|
| PWM-G1 | 3 ~ 9 Mbps | Mandatory |
| PWM-G2 | 6 ~ 18 Mbps | Mandatory |
| PWM-G3 | 12 ~ 36 Mbps | Mandatory |
| PWM-G4 | 24 ~ 72 Mbps | Mandatory |
| HS-G1 | Rate A = 1,248 Mbps (19.2/38.4/26/52MHz)<br>Rate B = 1,459.2 Mbps (19.2/38.4MHz)<br>1,456 Mbps (26/52 MHz) | Mandatory |
| HS-G2 | Rate A = 2,496 Mbps (19.2/38.4/26/52MHz)<br>Rate B = 2,918.4 Mbps (19.2/38.4MHz)<br>2,912 Mbps (26/52 MHz) | Mandatory |
| HS-G3 | Rate A = 4,992 Mbps (19.2/38.4/26/52MHz)<br>Rate B = 5,836.8 Mbps (19.2/38.4MHz)<br>5,824 Mbps (26/52 MHz) | Optional<br>(Support) |

## 2.5. User Density Size

| Capacity | User Density | Ratio | qTotalRawDeviceCapacity |
|---|---|---|---|
| 64GB | 59.58GB | 93.1% | 0x7738000 |
| 128GB | 119.17GB | 93.1% | 0xEE64000 |
| 256GB | 238.34GB | 93.1% | 0x1DCBC000 |

- User Density and Ratio are the values before LU configuration
- RPMB Size is excluded in User density size.

## 2.6. Device LU Partitioning

UFS Device shall support up to 32 Logical Units and one RPMB LU. Two of 32 Logical Units can be configured as boot LU A & B.

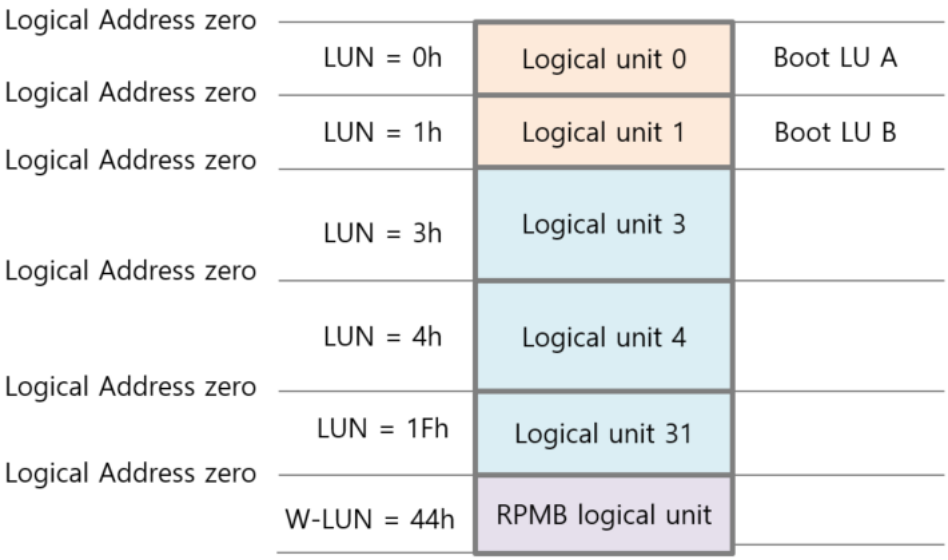


**Figure 3 - Example of UFS Device Memory Organization**

| LUs | Supported Size |
|---|---|
| BOOT LU | 4MB ~ 256MB |
| RPMB LU | 16MB |

# 3. UFS Feature Notes

## 3.1. Field Firmware Update (FFU)

SK hynix supports microcode download based Field Firmware Update using WRITE BUFFER command. For more details, see as the following chart like given below.

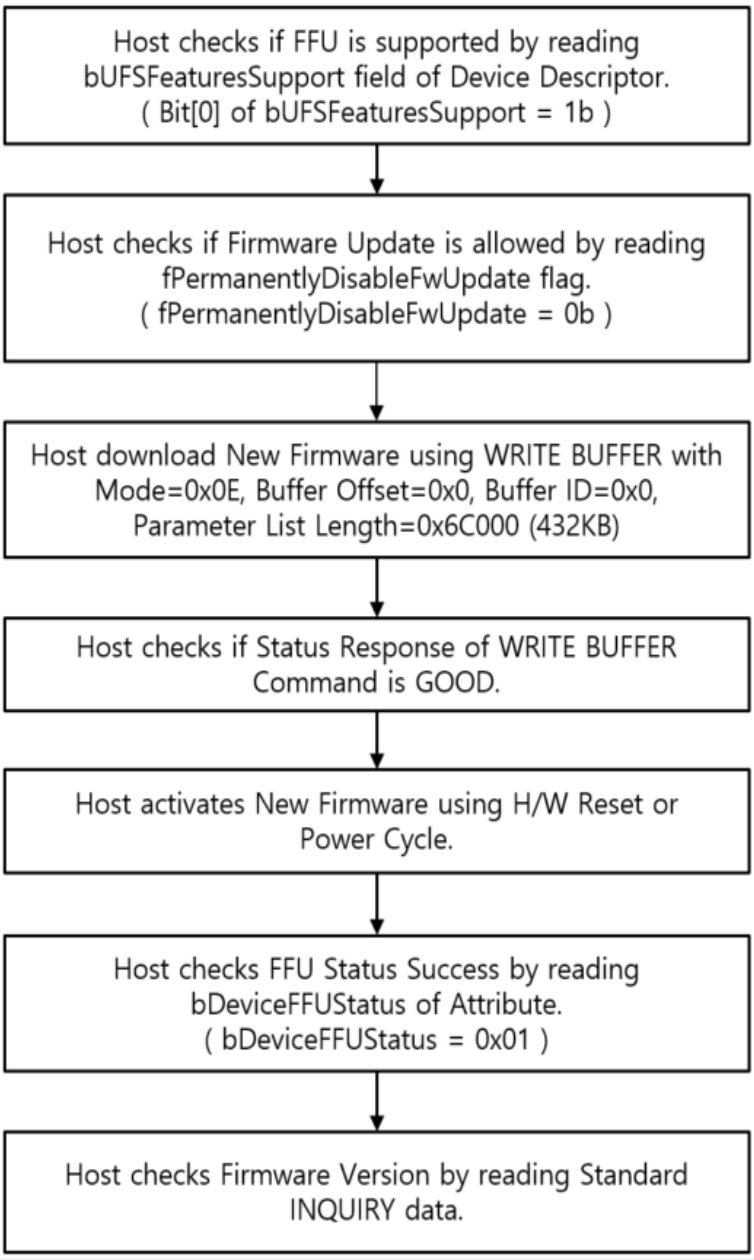


**Figure 4 - FFU Flow Chart**

### 3.1.1. WRITE BUFFER Command Parameters

| WRITE BUFFER Command Parameters | | | | |
|---|---|---|---|---|
| **Byte** | **Bit** | **Parameters** | **Value** | **Remark** |
| 0 | 7:0 | OPCODE | 3Bh | |
| 1 | 4:0 | MODE | 0Eh | Field Firmware Update |
| 2 | 7:0 | BUFFER ID | 00h | Buffer 0 supported |
| 3:5 | 7:0 | BUFFER OFFSET | 00h | Buffer 0 byte offset |
| 6:8 | 7:0 | PARAMETER LIST LENGTH | 6C000h | F/W binary size in bytes (432KB) |
| 9 | 7:0 | CONTROL | 00h | |

### 3.1.2. FFU related parameters in Device Descriptor

| FFU related Fields of Device Descriptor | | | | |
|---|---|---|---|---|
| **Offset** | **Size** | **Name** | **MDV** | **Remark** |
| 1Fh | 1 | bUFSFeaturesSupport | B1h | FFU feature supported<br>TOO-HIGH/TOO-LOW_TEMPERATURE supported<br>Host Performance Booster (HPB) |
| 20h | 1 | bFFUTimeout | 03h | Max FFU Timeout is 3 seconds. |

### 3.1.3. FFU related parameters in Attributes

| FFU related Attribute | | | | |
|---|---|---|---|---|
| **IDN** | **Size** | **Name** | **Access Property** | **Remark** |
| 14h | 1 | bDeviceFFUStatus | Read Only | Device FFU Status<br>00h: No information<br>01h: Successful microcode update<br>02h: Microcode corruption error<br>03h: Internal error<br>04h: Microcode version mismatch<br>05h-FEh: Reserved<br>FFh: General Error |

## 3.2. Supported VPD Pages

SK hynix supports VPD pages like below table.

| EVPD | Page Code | VPD Page Name |
|---|---|---|
| 0 | 00h | Standard INQUIRY Data |
| 1 | 00h | Supported VPD Pages VPD page |
| 1 | 80h | Unit Serial Number VPD page |
| 1 | 83h | Device Identification VPD page |
| 1 | 86h | Extended INQUIRY Data VPD page |
| 1 | 87h | Mode Page Policy VPD page |
| 1 | B0h | Block Limits VPD Page |
| 1 | B1h | Block Device Characteristics VPD Page |
| 1 | B2h | Thin Provisioning VPD page |

## 3.3. Mode Pages

SK hynix supports UFS supported pages.

| Page Code | | SUBPage Code | Page Name | Support |
|---|---|---|---|---|
| 00h | | - | Vendor specific | Not Support |
| 01h ~ 1Fh (SCSI Specific) | 0Ah | 00h (Device specific STANDARD page) | CONTROL | Support |
| | 01h | | READ-WRITE ERROR RECOVERY | Support |
| | 08h | | CACHING | Support |
| | - | 01h~DFh | Device Specific SUBPAGE | Not Support |
| | - | E0h~FEh | Vendor Specific SUBPAGE | Not Support |
| | - | FFh | ALL SUBPAGES | Not Support |
| 20h ~ 3Eh (Vendor Specific) | - | 00h | Vendor Specific STANDARD | Not Support |
| | - | 01h~FEh | Vendor Specific SUBPAGE | Not Support |
| | - | FFh | ALL SUBPAGES | Not Support |
| 3Fh (Return ALL pages) | 3Fh | 00h | ALL PAGES | Support |
| | 3Fh | 01h~FEh | Reserved | Reserved |
| | 3Fh | FFh | ALL SUBPAGES | Not Support |

# 4. UFS General Parameters

## 4.1. Power Supplies

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Supply Voltage (memory) | $V_{cc}$ | 2.7 | 3.6 | V | |
| Supply Voltage (controller and IO) | $V_{ccq}$ | 1.1 | 1.3 | V | Not Used |
| Supply Voltage (secondary for controller and IO) | $V_{ccq2}$ | 1.70 | 1.95 | V | |
| Supply power-up for 3.3V | tPRUH | | 35 | ms | |
| Supply power-up for 1.8V | tPRUL | | 25 | ms | |
| Supply power-up for 1.2V | tPRUV | | 20 | ms | Not Used |

## 4.2. Reset Signal

### 4.2.1. Reset Signal Electrical Parameters

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Input HIGH voltage | $V_{IH}$ | 0.65 * VCCQ | VCCQ + 0.3 | V | |
| Input LOW voltage | $V_{IL}$ | VSS - 0.3 | 0.35 * VCCQ | V | |

### 4.2.2. Reset Timing Parameters

| Symbol | Min | Max | Unit | Description |
|---|---|---|---|---|
| tRSTW | 1 | - | µs | RST_n Pulse Width |
| tRSTH | 1 | - | µs | RST_n High Period (Interval) |
| tRSTF | 100 | - | ns | RST_n Filter |

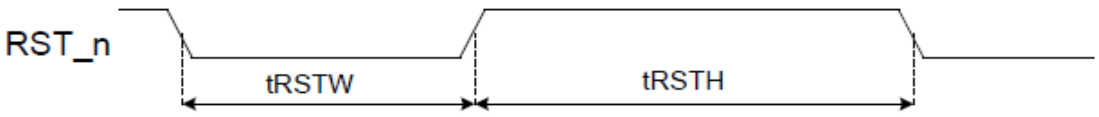


**Figure 5 - Reset Timing**

## 4.3. Reference Clock

The M-PHY specification defines the reference clock optional for the State Machine Type I [MIPI M-PHY].

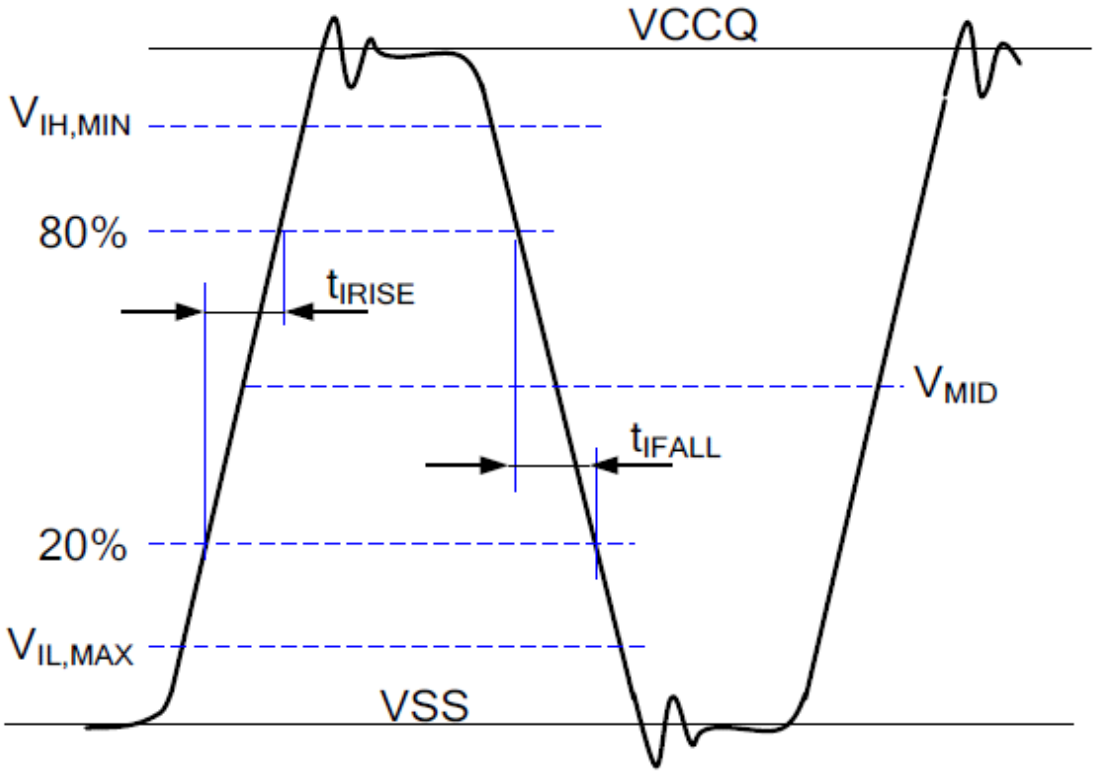


**Figure 6 - Clock Input Levels, Rise Time, and Fall Time**

| Parameter | Symbol | Min | Max | Unit | Remark |
|---|---|---|---|---|---|
| Frequency | $f_{ref}$ | 19.2<br>26 (Default)<br>38.4<br>52 | | MHz | 1 |
| Frequency Error | $f_{ERROR}$ | -150 | +150 | ppm | |
| Input High Voltage | $V_{IH}$ | 0.65*VCCQ | VCCQ+0.3 | V | 2 |
| Input Low Voltage | $V_{IL}$ | VSS-0.3 | 0.35*VCCQ | V | 2 |
| Input Clock Rise Time | $t_{IRISE}$ | - | 2 | ns | 3 |
| Input Clock Fall Time | $t_{IFALL}$ | - | 2 | ns | 3 |
| Duty Cycle | $t_{DC}$ | 45 | 55 | % | 4 |
| Phase Noise | N | - | -66 | dBC | 5 |
| Noise Floor Density<br>(REFCLK Noise floor density from 50KHz to 10MHz) | $N_{Density}$ | - | -140 | dBC/Hz | 6 |
| Input Impedance | $RL_{RX}$ | 100 | | kΩ | 7 |
| | $CL_{RX}$ | 5 | | pF | |
| Input Leakage Current | $I_{LKG}$ | - | 10 | μA | |

Notes

1. HS-BURST rates A and B are achieved with integer multipliers of $f_{ref}$.
2. Above Figure shows the input levels $V_{IL}$, MAX to $V_{IH}$, MIN.
3. Clock rise time and clock fall time shall be measured from 20% to 80% of the window defined by $V_{IL}$, MAX to $V_{IH}$, MIN
4. Clock duty cycle shall be measured at the Crossings of the REF_CLK signal with the midpoint VMID, defined as: VMID = ($V_{IL}$,MAX + $V_{IH}$,MIN) / 2
5. Integrated single side band phase noise from 50KHz to 10MHz. This parameter refers to the random jitter only.
6. White noise floor. This parameter refers to the random jitter only.
7. $RL_{RX}$ and $CL_{RX}$ include Rx package and Rx input impedance.

## 4.4. Bus Signal Levels

### 4.4.1. Output Level

SK hynix UFS supports two different amplitudes.

1) the Large Amplitude (LA)
2) the Small Amplitude (SA)

Every M-TX in every LINK will start communication with LA after power up or reset.
Option to switch to SA mode shall be supported via a Configuration Attribute.

DOUT_t / DOUT_c pair should satisfy VCM_TX

$$V_{CM_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2}$$

$V_{TXDP}$ / $V_{TXDN}$ = Positive / Negative Signal Voltage

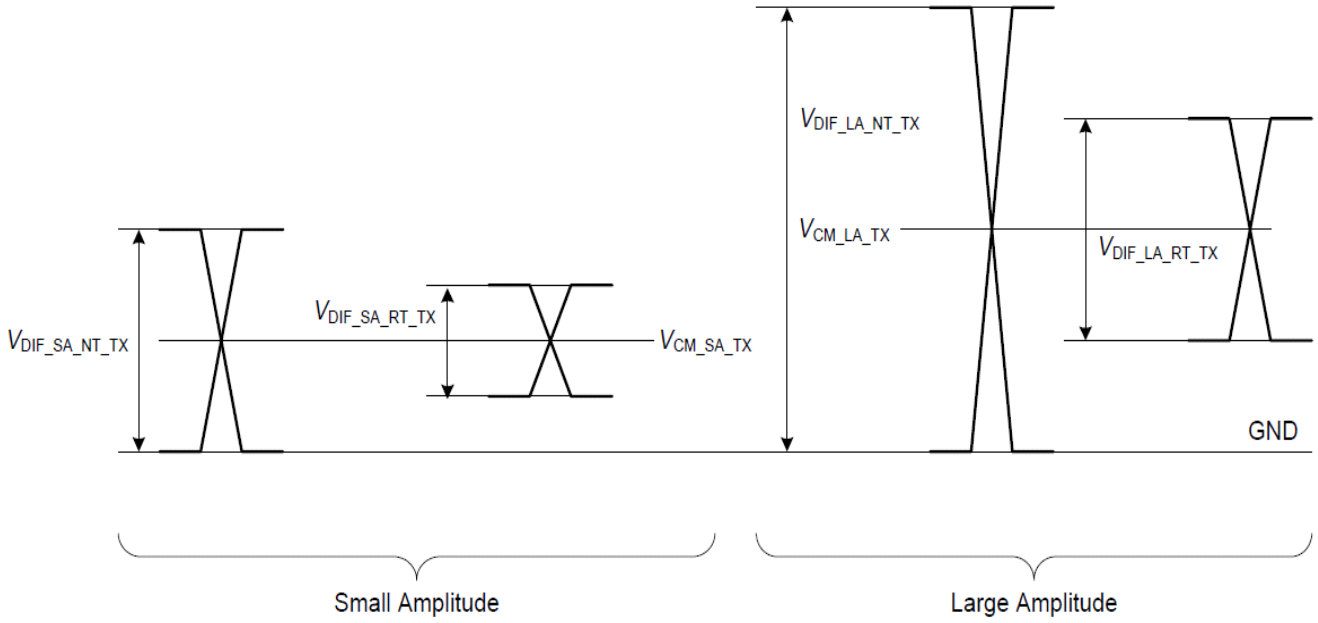


**Figure 7 - M-TX Signal Levels**

#### 4.4.1.1. Common M-TX Parameters

| Symbol | Min | Max | Unit | Description |
|---|---|---|---|---|
| $V_{DIF_DC_LA_RT_TX}$ | 160 | 240 | mV | Large Amplitude differential TX DC voltage when the M-TX is terminated |
| $V_{DIF_AC_LA_RT_TX}$ | 140 | 250 | mV | Large Amplitude differential TX AC voltage when the M-TX is terminated |
| $V_{DIF_DC_LA_NT_TX}$ | 320 | 480 | mV | Large Amplitude differential TX DC voltage when the M-TX is NOT terminated |
| $V_{DIF_AC_LA_NT_TX}$ | 280 | 500 | mV | Large Amplitude differential TX AC voltage when the M-TX is NOT terminated |
| $V_{DIF_DC_SA_RT_TX}$ | 100 | 130 | mV | Small Amplitude differential TX DC voltage when the M-TX is terminated |
| $V_{DIF_AC_SA_RT_TX}$ | 80 | 140 | mV | Small Amplitude differential TX AC voltage when the M-TX is terminated |
| $V_{DIF_DC_SA_NT_TX}$ | 200 | 260 | mV | Small Amplitude differential TX DC voltage when the M-TX is NOT terminated |
| $V_{DIF_AC_SA_NT_TX}$ | 160 | 280 | mV | Small Amplitude differential TX AC voltage when the M-TX is NOT terminated |
| $V_{CM_LA_TX}$ | 160 | 260 | mV | Large Amplitude common-mode TX Voltage |
| $V_{CM_SA_TX}$ | 80 | 190 | mV | Small Amplitude common-mode TX Voltage |
| $R_{SE_TX}$ | 40 | 60 | Ω | Single-ended Output Resistance |

### 4.4.2. Input Level

DIN_t / DIN_c pair should satisfy VCM_RX.

$$V_{CM_RX}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2}$$

| Symbol | Value | | Unit | Description |
|---|---|---|---|---|
| | Min | Max | | |
| **M-RX Electrical** | | | | |
| $V_{DIF_RT_RX}$ | 60 | 245 | mV | Differential RX voltage amplitude in terminated state. Defined for CJTPAT. |
| $V_{DIF_NT_RX}$ | 120 | 490 | mV | Differential RX voltage amplitude when the M-RX is not terminated. Defined for CJTPAT |
| $V_{CM_RX}$ | 25 | 330 | mV | RX common-mode voltage. Defined for CJTPAT |
| **M-RX Resistance** | | | | |
| $R_{DIF_RX}$ | 80 | 110 | Ω | Differential input resistance. Defined over $V_{DIF_RX}$ Range |

## 5. Latency Time

| Timing Parameter | Value | Remark |
|---|---|---|
| Read | MAX 100ms | |
| Write | MAX 200ms | |
| SYNC CACHE | MAX 300ms | |
| BKOP Termination Latency | MAX 40ms | bBackgroundOpsTermLat |
| Format (Wipe) | MAX 1 min | |

- File system overhead is not considered
- Not 100% tested but tested with worst corner.

# 6. UPIU Transaction Codes

SK hynix UFS supports following UPIU transaction codes. Each command is used with corresponding UPIU. It is not allowed to use undefined codes. Refer to UFS specification for more detail information.

| Initiator To Target | Transaction Code | Target to Initiator | Transaction Code |
|---|---|---|---|
| NOP Out | 00 0000b | NOP In | 10 0000b |
| Command | 00 0001b | Response | 10 0001b |
| Data Out | 00 0010b | Data In | 10 0010b |
| Task Management Request | 00 0100b | Task Management Response | 10 0100b |
| Reserved | 01 0001b | Ready To Transfer | 11 0001b |
| Query Request | 01 0110b | Query Response | 11 0110b |
| Reserved | 01 1111b | Reject UPIU | 11 1111b |
| Reserved | Others | Reserved | Others |

## 6.1. UFS SCSI Command

| Command name | Opcode | Command name | Opcode |
|---|---|---|---|
| FORMAT UNIT | 04h | SECURITY PROTOCOL IN | A2h |
| INQUIRY | 12h | SECURITY PROTOCOL OUT | B5h |
| MODE SELECT (10) | 55h | SEND DIAGNOSTIC | 1Dh |
| MODE SENSE (10) | 5Ah | START STOP UNIT | 1Bh |
| PRE-FETCH (10) | 34h | SYNCHRONIZE CACHE (10) | 35h |
| PRE-FETCH (16) | 90h | SYNCHRONIZE CACHE (16) | 91h |
| READ (6) | 08h | TEST UNIT READY | 00h |
| READ (10) | 28h | UNMAP | 42h |
| READ (16) | 88h | VERIFY (10) | 2Fh |
| READ BUFFER | 3Ch | WRITE (6) | 0Ah |
| READ CAPACITY (10) | 25h | WRITE (10) | 2Ah |
| READ CAPACITY (16) | 9Eh | WRITE (16) | 8Ah |
| REPORT LUNS | A0h | WRITE BUFFER | 3Bh |
| REQUEST SENSE | 03h | | |

# 7. UFS Descriptors, Flags, Attributes

The UFS modules support following UFS descriptors defined in UFS specification. Refer to UFS specification for more detail information.

| DESCRIPTOR TYPE | DESCRIPTOR IDN | DESCRIPTOR TYPE | DESCRIPTOR IDN |
|---|---|---|---|
| DEVICE | 00h | RFU | 06h |
| CONFIGURATION | 01h | GEOMETRY | 07h |
| UNIT | 02h | POWER | 08h |
| RFU | 03h | DEVICE HEALTH | 09h |
| INTERCONNECT | 04h | RFU | 0Ah~FFh |
| STRING | 05h | | |

## 7.1. Device Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 59h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 00h | Device Descriptor Type Identifier |
| 02h | 1 | bDevice | 00h | 00h: Device |
| 03h | 1 | bDeviceClass | 00h | 00h: Mass Storage |
| 04h | 1 | bDeviceSubClass | 00h | 00h: Embedded Bootable |
| 05h | 1 | bProtocol | 00h | 00h: SCSI |
| 06h | 1 | bNumberLU | User Conf. | Number of Logical Units (Default: 00h) |
| 07h | 1 | bNumberWLU | 04h | 04h: 4 Well known logical units exist |
| 08h | 1 | bBootEnable | User Conf. | 00h: Boot feature disabled (Default)<br>01h: Bootable feature enabled |
| 09h | 1 | bDescrAccessEn | User Conf. | 00h: Device Descriptor access disabled (Default)<br>01h: Device Descriptor access enabled |
| 0Ah | 1 | bInitPowerMode | User Conf. | 00h: UFS-Sleep Mode<br>01h: Active Mode (Default) |
| 0Bh | 1 | bHighPriorityLUN | User Conf. | 00h-07h: Configured LUN has high priority<br>7Fh: All logical units have the same priority (Default) |
| 0Ch | 1 | bSecureRemovalType | User Conf. | 00h: Information removed by an erase of the physical memory (Default)<br><br>01h: Information removed by overwriting the addressed locations with a<br>single character followed by an erase.<br><br>02h: Information removed by overwriting the addressed locations with a<br>character, its complement, then a random character.<br><br>03h: Information removed using a vendor define mechanism. |
| 0Dh | 1 | bSecurityLU | 01h | 01h: RPMB |
| 0Eh | 1 | bBackgroundOpsTermLat | 04h | bBackgroundOpsTermLat defines the maximum latency for the termination of ongoing background operations.<br>The latency is expressed in units of 10ms. |
| 0Fh | 1 | bInitActiveICCLevel | User Conf. | bInitActiveICCLevel defines the<br>bActiveICCLevel value after power on or reset<br><br>Valid range: 00h to 0Fh. (Default 00h) |
| 10h | 2 | wSpecVersion | 0220h | Specification version 2.20 |
| 12h | 2 | wManufactureDate | Device Specific | Manufacturing Date<br>ex) 0120h = Jan. 2020 |
| 14h | 1 | iManufacturerName | 01h | Index to Manufacturer Name String |
| 15h | 1 | iProductName | 02h | Index to Product Name String |
| 16h | 1 | iSerialNumber | 03h | Index to Serial Number String |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 17h | 1 | iOemID | 04h | Index to OEM ID String |
| 18h | 2 | wManufacturerID | 01ADh | Manufacturer ID |
| 1Ah | 1 | bUD0BaseOffset | 16h | Unit Descriptor 0 Base Offset |
| 1Bh | 1 | bUDConfigPLength | 1Ah | Unit Descr. Config. Param. Length<br>Total size of the configurable Unit Descriptor parameters |
| 1Ch | 1 | bDeviceRTTCap | 02h | RTT Capability of device Maximum number of outstanding RTTs supported by device |
| 1Dh | 2 | wPeriodicRTCUpdate | User Conf. | Frequency and method of Real-Time Clock update (Default 000h) |
| 1Fh | 1 | bUFSFeatureSupport | B1h | UFS Features Support<br>This field indicates which features are supported by the device.<br>A feature is supported if the related bit is set to one.<br>bit[0]: Field Firmware Update (FFU)<br>bit[1]: Production State Awareness (PSA)<br>bit[2]: Device Life Span<br>bit[3]: Refresh Operation<br>bit[4]: TOO_HIGH_TEMPERATURE<br>bit[5]: TOO_LOW_TEMPERATURE<br>bit[6]: Extended Temperature<br>bit[7]: Host Performance Booster (HPB)<br>Others: Reserved<br>Bit 0 shall be set to one |
| 20h | 1 | bFFUTimeout | 03h | Field Firmware Update Timeout.<br>The maximum time is expressed in units of seconds. |
| 21h | 1 | bQueueDepth | 20h | 0: The device implements the per-LU queueing architecture. |
| 22h | 2 | wDeviceVersion | Device Specific | Device version<br>64GB: 4306h<br>128GB: 4406h<br>256GB: 4506h |
| 24h | 1 | bNumSecureWPArea | 20h | Number of Secure Write Protect Areas |
| 25h | 4 | dPSAMaxDataSize | 00h | PSA Maximum Data Size |
| 29h | 1 | bPSAStateTimeout | 00h | PSA State Timeout |
| 2Ah | 1 | iProductRevisionLevel | 05h | Index to the string which contains the Product Revision Level |
| 2Bh | 5 | Reserved | | Reserved |
| 30h | 16 | Reserved | | Reserved for Unified Memory Extension standard |
| 40h | 2 | wHPBVersion | Vendor Specific | HPB Specification Version<br>Bit[15:8] = Major Version in BCD format<br>Bit[07:4] = Minor Version in BCD format<br>Bit[03:0] = Version suffix in BCD format<br>ex) version 1.03 = 0103h |
| 42h | 1 | bHPBControl | User Conf. | HPB Control Mode<br>00h: Host Control<br>01h: Device Control (Default) |
| 43h | 12 | Reserved | 00h | |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 4Fh | 4 | dExtendedUFSFeaturesSupport | 01B1h | UFS Features Support<br>This field indicates which features are supported by the device.<br>A feature is supported if the related bit is set to one.<br>bit[0]: Field Firmware Update (FFU)<br>bit[1]: Production State Awareness (PSA)<br>bit[2]: Device Life Span<br>bit[3]: Refresh Operation<br>bit[4]: TOO_HIGH_TEMPERATURE<br>bit[5]: TOO_LOW_TEMPERATURE<br>bit[6]: Extended Temperature<br>bit[7]: Host Performance Booster (HPB)<br>bit[8]: WriteBooster<br>Others: Reserved<br>Bit 0 shall be set to one |
| 53h | 1 | bWriteBoosterBufferPreserveUserSpcaeEn | User Conf. | Preserve User Space mode<br>00h: User space is reduced if WriteBooster Buffer is configured. The WriteBooster Buffer reduces the user space that can be configured at provisioning (default)<br>01h: User Space shall not be reduced if writebooster buffer is configured |
| 54h | 1 | bWriteBoosterBufferType | User Conf. | writebooster Buffer Type<br>00: LU Dedicated Buffer Type (default)<br>01: Single Shared Buffer Type |
| 55h | 4 | dNumSharedWriteBoosterBufferAllocUnits | User Conf. | The writebooster Buffer size for the shared WriteBooster Buffer Configuration. If this value is zero, then the shared WriteBooster is not configured for this device.<br>(default 0) |

## 7.2. Geometry Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 57h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 07h | Geometry Descriptor Type Identifier |
| 02h | 1 | bMediaTechnology | 00h | Reserved |
| 03h | 1 | Resrved | | Reserved |
| 04h | 8 | qTotalRawDeviceCapacity | Device Conf. | Total Raw Device Capacity<br>Total memory quantity available to the user to configure the device logical units (RPMB excluded).<br>It is expressed in units of 512 Bytes.<br>64GB: 07738000h<br>128GB: 0EE64000h<br>256GB: 1DCBC000h |
| 0Ch | 1 | bMaxNumberLU | 01h | 32 Logical Units |
| 0Dh | 4 | dSegmentSize | 00002000h | Segment Size<br>It is expressed in units of 512 Bytes |
| 11h | 1 | bAllocationUnitSize | 01h | Allocation Unit Size<br>Value expressed in number of Segments |
| 12h | 1 | bMinAddrBlockSize | 08h | Minimum addressable block size (4KB)<br>Value expressed in unit of 512 Bytes |
| 13h | 1 | bOptimalReadBlockSize | 40h | Optimal read block size<br>Value expressed in unit of 512 Bytes |
| 14h | 1 | bOptimalWriteBlockSize | 80h | Optimal write block size<br>Value expressed in unit of 512 Bytes |
| 15h | 1 | bMaxInBufferSize | 40h | Max data-in buffer size (32KB)<br>Value expressed in unit of 512 Bytes |
| 16h | 1 | bMaxOutBufferSize | 40h | Max data-out buffer size (32KB)<br>Value expressed in unit of 512 Bytes |
| 17h | 1 | bRPMB_ReadWriteSize | 40h | Maximum number of RPMB frames (256 byte of data) allowed in Security Protocol In and Security Protocol Out. |
| 18h | 1 | bDynamicCapacity ResourcePolicy | 00h | 00h: Spare blocks resource management policy is per logical unit. The host should release amount of logical blocks from each logical unit as asked by the device. |
| 19h | 1 | bDataOrdering | 00h | 00h: out-of-order data transfer is not supported by the device.<br>01h: out-of-order data transfer is supported by the device. |
| 1Ah | 1 | bMaxContexIDNumber | 0Fh | Maximum available number of contexts which are supported by the device. |
| 1Bh | 1 | bSysDataTagUnitSize | 00h | bSysDataUnitSize provides system data tag unit size, which can be calculated as in the following. (in bytes)<br>Tag Unit Size = $2^{bSysDataTagUnitSize}$ x bMinAddrBlockSize x 512 |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 1Ch | 1 | bSysDataTagResSize | 00h | This field is defined to inform the host about the maximum storage area size in bytes allocated by the device to handle system data by the tagging mechanism.<br>System Data Tag Resource Size =<br>$\text{Tag Unit Size} \times \text{floor}\left(\frac{\text{qTotalRawDeviceCapacity} \times 2^{\text{bSysDataTagResSize}-1}}{\text{Tag Unit Size}}\right)$<br>The range of valid bSysDataTagResSize values is from 0 to 6.<br>Values in range of 7 to 0xFF are reserved.<br>The formula covers a range from about 0.1% to 6.25% of the device capacity. |
| 1Dh | 1 | bSupportedSecRTypes | 09h | Supported Secure Removal Types<br>Bit map which represents the supported Secure Removal types.<br><br>Bit 0: Information removed by an erase of the physical memory<br>Bit 1: Information removed by overwriting the addressed locations with a<br>single character followed by an erase.<br>Bit 2: Information removed by overwriting the addressed locations with a<br>character, its complement, then a random character.<br>Bit 3: Information removed using a vendor define mechanism.<br>Others: Reserved<br><br>A value of one means that the corresponding Secure Removal type is supported. |
| 1Eh | 2 | wSupportedMemory Types | 8079h | Bit 0: Normal memory type<br>Bit 1: System code memory type<br>Bit 2: Non-Persistent memory type<br>Bit 3: Enhanced memory type 1<br>Bit 4: Enhanced memory type 2<br>Bit 5: Enhanced memory type 3<br>Bit 6: Enhanced memory type 4<br>Bit 15: RPMB memory type<br>* SK hynix supports SLC type for all enhanced memory type.<br>This device has no difference of each enhanced type. |
| 20h | 4 | dSystemCodeMaxNAllocU | 00h | System code memory type is not supported. |
| 24h | 2 | wSystemCodeCapAdjFac | 00h | System code memory type is not supported. |
| 26h | 4 | dNonPersistMaxNAllocU | 00h | Non-Persistent memory type is not supported. |
| 2Ah | 2 | wNonPersistCapAdjFac | 00h | Non-Persistent memory type is not supported. |
| 2Ch | 4 | dEnhanced1MaxNAllocU | Device Conf | Max Number of Allocation Units for the Enhanced memory type 1<br>64GB : 03B9Ch<br>128GB: 07732h<br>256GB: 0EE5Eh |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 30h | 2 | wEnhanced1CapAdjFac | 0300h | Capacity Adjustment Factor for the Enhanced memory type 1<br>Factor used to adjust the memory capacity of this memory property from normal memory:<br><br>Capacity Enhanced1 = CapacityNormalMem / CapAdjFac<br><br>wEnhanced1CapAdjFac = INTEGER(256 × CapAdjFac) |
| 32h | 4 | dEnhanced2MaxNAllocU | Device Conf | Enhanced memory type 2 is supported.<br>64GB : 03B9Ch<br>128GB: 07732h<br>256GB: 0EE5Eh |
| 36h | 2 | wEnhanced2CapAdjFac | 0300h | Enhanced memory type 2 is supported. |
| 38h | 4 | dEnhanced3MaxNAllocU | Device Conf | Enhanced memory type 3 is supported.<br>64GB : 03B9Ch<br>128GB: 07732h<br>256GB: 0EE5Eh |
| 3Ch | 2 | wEnhanced3CapAdjFac | 0300h | Enhanced memory type 3 is supported. |
| 3Eh | 4 | dEnhanced4MaxNAllocU | Device Conf | Enhanced memory type 4 is supported.<br>64GB : 03B9Ch<br>128GB: 07732h<br>256GB: 0EE5Eh |
| 42h | 2 | wEnhanced4CapAdjFac | 0300h | Enhanced memory type 4 is supported. |
| 44h | 4 | dOptimalLogicalBlockSize | 03333003h | Optimal Logical Block Size<br>Bit [3:0]: Normal memory type<br>Bit [7:4]: System code memory type<br>Bit [11:8]: Non-Persistent memory type<br>Bit [15:12]: Enhanced memory type 1<br>Bit [19:16]: Enhanced memory type 2<br>Bit [23:20]: Enhanced memory type 3<br>Bit [27:24]: Enhanced memory type 4<br>Bit [31:28]: Reserved<br>The optimal logical block size for each memory type can be calculated from the related dOptimalLogicalBlockSize field as indicated in the following:<br>Optimal Logical Block Size = 2^ (dOptimalLogicalBlockSize field) x bMinAddrBlockSize x 512 byte |
| 48h | 1 | bHPBRegionSize | 0Fh | HPB Region size, which can be calculated as in the following (in bytes)<br>HPB Region Size = 512B x 2^bHPBRegionSize |
| 49h | 1 | bHPBNumberLU | 20h | Maximum number of HPB LU supported by the device<br>00h: HPB is not supported by the device.<br>01h ~ 20h: Maximum number of HPB LU supported by the device<br>Others: Reserved |
| 4Ah | 1 | bHPBSubRegionSize | 0Fh | HPB Sub-Region size, which can be calculated as in the following (in bytes) and shall be a multiple of Logical Block size<br>HPB Sub-Region size = 512B x 2^bHPBSubRegion Size |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 4Bh | 2 | wDeviceMaxActiveHPBRegions | Device Conf. | Maximum number of Active HPB Regions that is supported by the device<br>64GB : 0EE7h<br>128GB: 1DCDh<br>256GB: 2000h |
| 4Dh | 2 | Reserved | 00h | |
| 4Fh | 4 | dWriteBoosterBufferMaxNAllocUnits | 00h | Maximum Total WriteBooster Buffer size which is supported by the entire device. The summation of the WriteBooster Buffer size for all LUs should be equal to or less than size value indicated by this descriptor<br>64GB : 0C00h<br>128GB: 0C00h<br>256GB: 1E00h |
| 53h | 1 | bDeviceMaxWriteBoosterLUs | 01h | Number of maximum WriteBooster Buffer supported by the device<br>Default 01h |
| 54h | 1 | bWriteBoosterBufferCapAdjFac | 03h | Capacity Adjustment Factor for the WriteBooster Buffer Memory Type<br>This Value provides the LBA space reduction multiplication factor when WriteBooster Buffer is configured in user space reduction mode. Therefore, this parameter applies only if bWriteBoosterBuffer PreservedUserSpaceEn is 00h.<br>02h: MLC NAND<br>03h: TLC NAND |
| 55h | 1 | bSupportedWriteBoosterBufferUserSpaceReductionTypes | 01h | The supportability of user space reduction mode and preserve user space mode.<br>00h: WriteBooster Buffer can be configured only in user space reduction type<br>01h: WriteBooster Buffer can be configured only in preserve user space type (Default)<br>02h: Device can be configured in either user space reduction type or preserve user space type<br>Others: Reserved |
| 56h | 1 | bSupportedWriteBoosterBufferTypes | 02h | The supportability of WriteBooster Buffer Type<br>00h: LU Based WriteBooster Buffer Configuration<br>01h: Single shared WriteBooster Buffer configuration<br>02h: Supporting both LU based WriteBooster Buffer and Single shared WriteBooster Buffer Configuration (Default)<br>Others: Reserved |

## 7.3. Unit Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 2Dh | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 02h | UNIT Descriptor Type Identifier |
| 02h | 1 | bUnitIndex | 00h to 1Fh | Unit Index |
| 03h | 1 | bLUEnable | User Conf. | Logical Unit Enable<br>00h: Logical Unit disabled (Default)<br>01h: Logical Unit enabled<br>02h: Logical Unit enabled with HPB function<br>Others: Reserved |
| 04h | 1 | bBootLunID | User Conf. | Boot LUN ID<br>00h: Not bootable (Default)<br>01h: Boot LU A<br>02h: Boot LU B<br>Others: Reserved |
| 05h | 1 | bLUWriteProtect | User Conf. | Logical Unit Write Protect<br>00h: LU not write protected (Default)<br>01h: LU write protected when fPowerOnWPEn = 1<br>02h: LU permanently write protected when fPermanentWPEn = 1<br>Others: Reserved |
| 06h | 1 | bLUQueueDepth | 00h | Logical Unit Queue Depth<br>Queue depth available in this LU.<br>Queue depth of '0' means best effort by device to service the command task. |
| 07h | 1 | bPSASensitive | 00h | 00h: LU is not sensitive to soldering.<br>01h: LU is sensitive to soldering.<br>Others: Reserved |
| 08h | 1 | bMemoryType | User Conf. | Memory Type<br>bMemoryType defines logical unit memory type.<br>00h: Normal Memory (Default)<br>01h: System code memory type<br>(Not supported)<br>02h: Non-Persistent memory type<br>(Not supported)<br>03h: Enhanced memory type 1<br>04h: Enhanced memory type 2<br>05h: Enhanced memory type 3<br>06h: Enhanced memory type 4<br>Others: Reserved |
| 09h | 1 | bDataReliability | User Conf. | Data Reliability<br>bDataReliability defines the device behavior when a power failure occurs during a write operation to the logical unit<br>00h: the logical unit is not protected. Logical unit's entire data might be lost as a result of a power failure during a write operation (Default)<br>01h: logical unit is protected. Logical unit's data is protected against power failure.<br>Others: Reserved |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 0Ah | 1 | bLogicalBlockSize | User conf. | Logical Block Size (Default 4KB)<br>The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: $2^{bLogicalBlockSize}$(i.e., bLogicalBlockSize = 0Ch corresponds to 4 KByte Logical Block Size).<br>Its minimum value is 0Ch, which corresponds to 4 Kbyte. |
| 0Bh | 8 | qLogicalBlockCount | User conf. | Logical Block Count (Default 00h)<br>Total number of addressable Logical Blocks in the LU in Logical Block Size unit.<br>qLogicalBlockCount can be configured setting the dNumAllocUnits parameter of the Configuration Descriptor. |
| 13h | 4 | dEraseBlockSize | 00h | Erase Block Size (4KB) in number of Logical Blocks.<br>dEraseBlockSize value is updated automatically by the device after device<br>configuration. |
| 17h | 1 | bProvisioningType | User conf. | Provisioning Type<br>00h: Thin Provisioning is disabled (default)<br>02h: Thin Provisioning is enabled and TPRZ = 0<br>03h: Thin Provisioning is enabled and TPRZ = 1<br>Others: Reserved |
| 18h:1Fh | 8 | qPhyMemResourceCount | 00h | Physical Memory Resource Count<br>Total physical memory resource available in the logical unit.<br>Value expressed in units of Logical Block Size. |
| 20h | 2 | wContextCapabilities | User conf. | Default 0000h<br>Bit [3:0]: MaxContextID is the maximum amount of contexts that the LU supports simultaneously. The sum of all MaXContextID must not exceed bMaxContexIDNumber.<br>Bit [6:4]: LARGE_UNIT_MAX_MULTIPLIER_M1 is the highest multiplier that can be configured for Large Unit contexts, minus one. Large Unit contexts may be configured to have a multiplier in the range:<br>1 ≤ multiplier ≤(LARGE_UNIT_MAX_MULTIPLIER_M1 + 1)<br>This field is read only.<br>Bit [15:7]: Reserved |
| 22h | 1 | bLargeUnitGranularity_M1 | 00h | Large Unit is not supported. |
| 23h | 2 | wLUMaxActiveHPB Regions | User conf. | Maximum Number of Active HPB Regions<br>Maximum number of HPB Active Regions that is supported by the logical unit.<br>Default value is 0000h |
| 25h | 2 | wHPBPinnedRegion StartIdx | User conf. | HPB Pinned Region Start Offset<br>Default value is 0000h |
| 27h | 2 | wNumHPBPinnedRegions | User conf. | Number of HPB Pinned Regions<br>Number of HPB pinned Regions assigned to the HPB logical unit.<br>Value "0" means that there is no pinned Region for this LU. |
| 29h | 4 | dLUNumWriteBoosterBufferAllocUnits | User Conf. | The WriteBooster Buffer size for the Logical Unit.<br>If this value is '0', then the WriteBooster is not Supported for this LU |

### 7.3.1. RPMB Unit Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 23h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 02h | RPMB Unit Descriptor Type Identifier |
| 02h | 1 | bUnitIndex | C4h | Unit Index |
| 03h | 1 | bLUEnable | 01h | 01h: Logical Unit enabled |
| 04h | 1 | bBootLunID | 00h | 00h: Not bootable |
| 05h | 1 | bLUWriteProtect | 00h | 00h: LU not write protected |
| 06h | 1 | bLUQueueDepth | 01h | Queue depth available in this LU. |
| 07h | 1 | bPSASensitive | 00h | |
| 08h | 1 | bMemoryType | 0Fh | 0Fh: RPMB Memory Type |
| 09h | 1 | Reserved | | Reserved |
| 0Ah | 1 | bLogicalBlockSize | 08h | The size of addressable logical blocks is equal the result of exponentiation with as base the number two and as exponent the bLogicalBlockSize value: 2bLogicalBlockSize (i.e., bLogicalBlockSize = 08h corresponds to 256 Byte Logical Block Size) |
| 0Bh | 8 | qLogicalBlockCount | 00010000h | Total number of addressable Logical Blocks of the RPMB LU in Logical Block Size unit. For RPMB, Logical Block Count shall be a multiple of 512 (i.e., 128 KByte) |
| 13h | 4 | dEraseBlockSize | 80000000h | In number of Logical Blocks. For RPMB, Erase Block Size is ignored. |
| 17h | 1 | bProvisioningType | 00h | 00h: Thin Provisioning is disabled. |
| 18h:1Fh | 8 | qPhyMemResourceCount | 00010000h | Total physical memory resource available in the logical unit.<br>Value expressed in units of bLogicalBlockSize.The dynamic device capacity feature does not apply to the RPMB well known logical unit. Therefore qPhyMemResourceCount value is always equal to qLogicalBlockCount value. |
| 20h:22h | 3 | Reserved | | Reserved |

## 7.4. Power Parameters Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 62h | Size of this descriptor |
| 01h | 1 | bDescriptorIDN | 08h | Power Parameters Descriptor Type Identifier |
| 02h | 2 | wActiveICCLevelsVCC(0) | 82BCh | 2 byte maximum VCC current value for each of the 16 active current consumption levels starting with level 0 |
| 04h | 2 | wActiveICCLevelsVCC(1) | | |
| 06h | 2 | wActiveICCLevelsVCC(2) | | |
| 08h | 2 | wActiveICCLevelsVCC(3) | | |
| 0Ah | 2 | wActiveICCLevelsVCC(4) | | |
| 0Ch | 2 | wActiveICCLevelsVCC(5) | | |
| 0Eh | 2 | wActiveICCLevelsVCC(6) | | |
| 10h | 2 | wActiveICCLevelsVCC(7) | | |
| 12h | 2 | wActiveICCLevelsVCC(8) | | |
| 14h | 2 | wActiveICCLevelsVCC(9) | | |
| 16h | 2 | wActiveICCLevelsVCC(10) | | |
| 18h | 2 | wActiveICCLevelsVCC(11) | | |
| 1Ah | 2 | wActiveICCLevelsVCC(12) | | |
| 1Ch | 2 | wActiveICCLevelsVCC(13) | | |
| 1Eh | 2 | wActiveICCLevelsVCC(14) | | |
| 20h | 2 | wActiveICCLevelsVCC(15) | | |
| 22h | 2 | wActiveICCLevelsVCCQ(0) | 00h | Not Used |
| 24h | 2 | wActiveICCLevelsVCCQ(1) | 00h | Not Used |
| 26h | 2 | wActiveICCLevelsVCCQ(2) | 00h | Not Used |
| 28h | 2 | wActiveICCLevelsVCCQ(3) | 00h | Not Used |
| 2Ah | 2 | wActiveICCLevelsVCCQ(4) | 00h | Not Used |
| 2Ch | 2 | wActiveICCLevelsVCCQ(5) | 00h | Not Used |
| 2Eh | 2 | wActiveICCLevelsVCCQ(6) | 00h | Not Used |
| 30h | 2 | wActiveICCLevelsVCCQ(7) | 00h | Not Used |
| 32h | 2 | wActiveICCLevelsVCCQ(8) | 00h | Not Used |
| 34h | 2 | wActiveICCLevelsVCCQ(9) | 00h | Not Used |
| 36h | 2 | wActiveICCLevelsVCCQ(10) | 00h | Not Used |
| 38h | 2 | wActiveICCLevelsVCCQ(11) | 00h | Not Used |
| 3Ah | 2 | wActiveICCLevelsVCCQ(12) | 00h | Not Used |
| 3Ch | 2 | wActiveICCLevelsVCCQ(13) | 00h | Not Used |
| 3Eh | 2 | wActiveICCLevelsVCCQ(14) | 00h | Not Used |
| 40h | 2 | wActiveICCLevelsVCCQ(15) | 00h | Not Used |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 42h | 2 | wActiveICCLevelsVCCQ2(0) | 82BCh | 2 byte maximum VCCQ2 current value for each of the 16 active current consumption levels starting with level 0 |
| 44h | 2 | wActiveICCLevelsVCCQ2(1) | | |
| 46h | 2 | wActiveICCLevelsVCCQ2(2) | | |
| 48h | 2 | wActiveICCLevelsVCCQ2(3) | | |
| 4Ah | 2 | wActiveICCLevelsVCCQ2(4) | | |
| 4Ch | 2 | wActiveICCLevelsVCCQ2(5) | | |
| 4Eh | 2 | wActiveICCLevelsVCCQ2(6) | | |
| 50h | 2 | wActiveICCLevelsVCCQ2(7) | | |
| 52h | 2 | wActiveICCLevelsVCCQ2(8) | | |
| 54h | 2 | wActiveICCLevelsVCCQ2(9) | | |
| 56h | 2 | wActiveICCLevelsVCCQ2(10) | | |
| 58h | 2 | wActiveICCLevelsVCCQ2(11) | | |
| 5Ah | 2 | wActiveICCLevelsVCCQ2(12) | | |
| 5Ch | 2 | wActiveICCLevelsVCCQ2(13) | | |
| 5Eh | 2 | wActiveICCLevelsVCCQ2(14) | | |
| 60h | 2 | wActiveICCLevelsVCCQ2(15) | | |

## 7.5. Interconnect Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 06h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 04h | Interconnect Description Type Identifier |
| 02h | 2 | bcdUniproVersion | 0161h | MIPI UniPro version number in BCD format<br>(i.e., version 1.61 = 0161h) |
| 04h | 2 | bcdMphyVersion | 0300h | MIPI M-PHY version number in BCD format<br>(i.e., version 3.00 = 0300h) |

## 7.6. Manufacturer Name String Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 12h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String Descriptor Type Identifier |
| 02h | 2 | UC[0] | 0053h | Unicode string character ("S") |
| 04h | 2 | UC[1] | 004Bh | Unicode string character ("K") |
| 06h | 2 | UC[2] | 0068h | Unicode string character ("h") |
| 08h | 2 | UC[3] | 0079h | Unicode string character ("y") |
| 0Ah | 2 | UC[4] | 006Eh | Unicode string character ("n") |
| 0Ch | 2 | UC[5] | 0069h | Unicode string character ("i") |
| 0Eh | 2 | UC[6] | 0078h | Unicode string character ("x") |
| 10h | 2 | UC[7] | 0000h | NULL |

## 7.7. OEM ID String Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 0Ah | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String Description Type Identifier |
| 02h | 2 | UC[0] | 0030h | |
| 04h | 2 | UC[1] | 0031h | |
| 06h | 2 | UC[2] | 0041h | |
| 08h | 2 | UC[3] | 0044h | |

## 7.8. Serial Number String Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 0Eh | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String Descriptor Type Identifier |
| 02h | 2 | UC[0] | - | Unique serial number hex code |
| 04h | 2 | UC[1] | - | Unique serial number hex code |
| 06h | 2 | UC[2] | - | Unique serial number hex code |
| 08h | 2 | UC[3] | 0000h | NULL |
| 0Ah | 2 | UC[4] | 0000h | NULL |
| 0Ch | 2 | UC[5] | 0000h | NULL |

SK hynix supports 6 Bytes serial Number which is assigned by unique hex-code at each device. If some part of them (less than 6 bytes) are used, it couldn't be guaranteed uniqueness.

## 7.9. Product Revision Level String Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 0Ah | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 05h | String Description Type Identifier |
| 02h | 2 | UC[0] | 0030h[1)] | "0" |
| 04h | 2 | UC[1] | 0030h[1)] | "0" |
| 06h | 2 | UC[2] | 0030h[1)] | "0" |
| 08h | 2 | UC[3] | 0031h[1)] | "1" |

Notes
1. The value in product revision level string descriptor composed of the revision count of controller and the revision count of F/W patch. Above value is an example.

## 7.10. Device Health Descriptor

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 25h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 09h | Device Health Descriptor Type Identifier |
| 02h | 1 | bPreEOLInfo | Device Specific | Pre End of Life Information<br>This field provides indication about device life time reflected by average reserved blocks.<br>00h: Not defined<br>01h: Normal<br>02h: Warning Consumed 80% of reserved blocks<br>03h: Critical Consumed 90% of reserved blocks<br>Others: Reserved |
| 03h | 1 | bDeviceLifeTimeEstA | Device Specific | This field provieds an indication of the device life time based on the amount of performed program/erase cycles. The caculation method is vendor specific and reffered as method A.<br>00h: information not available<br>01h: 0%~10% device life time used<br>02h: 10%~20% device life time used<br>03h: 20%~30% device life time used<br>04h: 30%~40% device life time used<br>05h: 40%~50% device life time used<br>06h: 50%~60% device life time used<br>07h: 60%~70% device life time used<br>08h: 70%~80% device life time used<br>09h: 80%~90% device life time used<br>0Ah: 90%~100% device life time used<br>0Bh: Exceeded its maximum estimated device life time<br>Others: Reserved |
| 04h | 1 | bDeviceLifeTimeEstB | Device Specific | This field provides an indication of the device life time based on the amount of performed program/erase cycles. The caculation method is vendor specific and reffered as method B.<br>00h: Information not available<br>01h: 0%~10% device life time used<br>02h: 10%~20% device life time used<br>03h: 20%~30% device life time used<br>04h: 30%~40% device life time used<br>05h: 40%~50% device life time used<br>06h: 50%~60% device life time used<br>07h: 60%~70% device life time used<br>08h: 70%~80% device life time used<br>09h: 80%~90% device life time used<br>0Ah: 90%~100% device life time used<br>0Bh: Exceeded its maximum estimated device life time<br>Others: Reserved |
| 05h | 2 | wFactoryBadBlockCount | Device Specific | Initial bad block count |
| 07h | 2 | wRuntimeBadBlockCount | Device Specific | Run Time bad block count |

| OFFSET | SIZE | NAME | VALUE | Description |
|---|---|---|---|---|
| 09h | 2 | wMaxBlockEraseCount | Device Specific | Maximum NAND block erase count |
| 0Bh | 2 | wMinBlockEraseCount | Device Specific | Minimum NAND block erase count |
| 0Dh | 2 | wAveBlockEraseCount | Device Specific | Average NAND block erase count |
| 0Fh | 2 | wReadReclaimCount | Device Specific | Count number of read reclaim operation |
| 11h | 4 | dSPOCount | Device Specific | Count number of Sudden power off.<br>If reach to 0xFFFFFFFF, it will not be increased further. |
| 15h | 4 | dTotalWriteSize100M | Device Specific | Total write size, unit is 100MB |
| 19h | 4 | dLVD count | Device Specific | Low Voltage Detection of VCC, VCCQ power supply.<br>Bit31~Bit16: LVD count of VCC(3.3V)<br>Bit15~Bit0: LVD count of VCCQ(1.8V) |
| 1Dh | 2 | bFFUCount | Device Specific | Success count of FFU to higher (not same) version firmware |
| 1Fh | 4 | dTotalReadSize100M | Device Specific | Total read size, unit is 100MB |
| 23h | 1 | bRemainReservedBlockCount | Device Specific | Count number of remain reserved block |
| 24h | 1 | Reserved | | |

## 7.11. UFS Flags

| IDN | NAME | TYPE | Default | Description |
|---|---|---|---|---|
| 00h | Reserved | | | Reserved |
| 01h | fDeviceInit | Read/<br>Set only | 0 | Device Initialization<br>Host sets fDeviceInit flag to initiate device initialization after boot process is completed.<br>Device resets flag when device initialization is completed.<br>0b: Device initialization completed or not started yet.<br>1b: Device initialization in progress. |
| 02h | fPermanentWPEn | Read/<br>Write Once | 0 | Permanent Write Protection Enable<br>fPermanentWPEn enables permanent write protection on all logical units configured as permanent protected;<br>it cannot be toggled or cleared once it is set.<br>00h: Permanent write protection disabled.<br>01h: Permanent write protection enabled. |
| 03h | fPowerOnWPEn | Read/<br>Power-on<br>Reset | 0 | Power On Write Protection Enable<br>fPowerOnWPEn enables the write protection on all logical units configured as power on write protected.<br>If fPowerOnWPEn is equal to one and the device receives a Query Request to clear or toggle this flag, the Query Request shall fail and Response field shall be set to "F8h"(Parameter already written).<br>The device shall set fPowerOnWPEn to zero in the event of power cycle or hardware reset.<br>0b: Power on write protection disabled.<br>1b: Power on write protection enabled. |
| 04h | fBackgroundOpsEn | Read/<br>Volatile | 1 | Background Operations Enable<br>0b: Device is not permitted to run background operations.<br>1b: Device is permitted to run background operations. |
| 05h | fDeviceLifeSpanModeEn | Read/<br>Volatile | 0 | Device Life Span Mode<br>0b: Device Life Span Mode is disabled.<br>1b: Device Life Span Mode is enabled. |
| 06h | fPurgeEnable | Write Only/<br>Volatile | 0 | Purge Enable<br>0b: Purge operation is disabled.<br>1b: Purge operation is enabled.<br><br>This flag shall only be set when the command queue of all logical units are empty and the bPurgeStatus is 00h (Idle).<br>fPurgeEnable is automatically cleared by the UFS device when the operation completes or an error condition occurs. fPurgeEnable can be cleared by the host to interrupt an ongoing purge operation. |
| 07h | Reserved | | | Reserved |

| IDN | NAME | TYPE | Default | Description |
|---|---|---|---|---|
| 08h | fPhyResourceRemoval | Read/ Persistent | 0 | Physical Resource Removal<br>The host sets this flag to one to indicate that the dynamic capacity operation shall commence upon device EndPointReset or hardware reset.<br>The device shall reset this flag to zero after completion of dynamic capacity operation.<br>The host cannot reset this flag. |
| 09h | fBusyRTC | Read Only | 0 | Busy Real Time Clock<br>0b: Device is not executing internal operation related to RTC.<br>1b: Device is executing internal operation related to RTC.<br>When this flag is set to one, it is recommended for the host to not send commands to the device. |
| 0Ah | Reserved | | | Reserved |
| 0Bh | fPermanentlyDisableFwUpdate | Read/ Write Once | 0 | Permanently Disable Firmware Update<br>0b: The UFS device firmware may be modified<br>1b: The UFS device shall permanently disallow future firmware updates to the UFS device |
| 0Ch | Reserved | - | - | |
| 0Dh | Reserved | - | - | |
| 0Eh | fWriteBoosterEn | Read/ Volatile | 0 | writebooster Enable<br>0b: writebooster is not enabled<br>1b: writebooster is enabled |
| 0Fh | fWriteBoosterBufferFlushEn | Read/ Volatile | 0 | Flush the data in writebooster Buffer to the user area of storage<br>0b: Flush operation is not performed<br>1b: Flush operation is performed |
| 10h | fWriteBoosterBufferFlushDuringHibernate | Read/ Volatile | 0 | Flush writebooster Buffer during Hibernation state<br>0b: Device is not allowed to flush the writebooster buffer during Hibernation state of the device<br>1b: Device is allowed to flush the writebooster Buffer during Hibernation state of the device |
| 11h | fHPBReset | Read / Set Only | 0 | HPB Reset<br>Host set this flag as”1”to inform the device that host reset its HPB tables. After this flag is set all regions are inactive. Device reset flag as “0” when device inactivated all region information.<br>0b: HPB reset completed or not started yet<br>1b: HPB reset in progress |

## 7.12. UFS Attributes

| IDN | NAME | TYPE | Size [Byte] | MDV | Description |
|---|---|---|---|---|---|
| 00h | bBootLunEn | Read/ Persistent | 1 | 00h | Boot LUN Enable<br>00h: Boot disabled<br>01h: Enabled boot from Boot LU A<br>02h: Enabled boot from Boot LU B<br>All others: Reserved<br><br>When bBootLunEn = 00h the boot feature is disabled, the device behaves as if bBootEnable would be equal to 0 |
| 01h | Reserved | | 1 | | Reserved |
| 02h | bCurrentPowerMode | Read Only | 1 | 11h | Current Power Mode<br>00h: Idle mode<br>10h: Pre-Active mode<br>11h: Active mode<br>20h: Pre-Sleep mode<br>22h: UFS-Sleep mode<br>30h: Pre-Power Down mode<br>33h: UFS-Power Down mode<br>Others: Reserved |
| 03h | bActiveICCLevel | Read/ Volatile | 1 | 00h | bActiveICCLevel defines the maximum current consumption allowed during Active Mode.<br>00h: Lowest Active ICC level<br>0Fh: Highest Active ICC level<br>Others: Reserved<br>Valid range from 00h to 0Fh. |
| 04h | bOutOfOrderDataEn | Read/ Write Once | 1 | 00h | Out of Order Data transfer Enable<br>00h: Out-of-order data transfer is disabled.<br>01h: Out-of-order data transfer is enabled.<br>Others: Reserved<br>This bit shall have effect only when bDataOrdering = 01h. |
| 05h | bBackgroundOpStatus | Read Only | 1 | 00h | Background Operations Status<br>Device health status for background operation<br><br>00h: Not required<br>01h: Required, not critical<br>02h: Required, performance impact<br>03h: Critical<br>Others: Reserved |

| IDN | NAME | TYPE | Size [Byte] | MDV | Description |
|---|---|---|---|---|---|
| 06h | bPurgeStatus | Read Only | 1 | 00h | Purge Operation Status<br>00h: Idle (purge operation disabled)<br>01h: Purge operation in progress<br>02h: Purge operation stopped prematurely<br>03h: Purge operation completed successfully<br>04h: Purge operation failed due to logical unit queue not empty<br>05h: Purge operation general failure<br><br>When the bPurgeStatus is equal to the values 02h, 03h, 04h or 05h, the bPurgeStatus is automatically cleared to 00h (Idle) the first time that it is read. |
| 07h | bMaxDataInSize | Read/ Persistent | 1 | 40h | Maximum Data In Size (32KB)<br>Maximum data size in a DATA IN UPIU.<br>Value expressed in number of 512 Byte units.<br>bMaxDataInSize shall not exceed the bMaxInBufferSize parameter.<br>bMaxDataInSize = bMaxInBufferSize when the UFS device is shipped. |
| 08h | bMaxDataOutSize | Read/ Persistent | 1 | 40h | Maximum Data-Out Size (32KB)<br>Maximum data-size in a DATA-OUT UPIU.<br>Value expressed in number of 512 Byte units.<br>bMaxDataOutSize shall not exceed the bMaxOutBufferSize parameter.<br>bMaxDataOutSize= bMaxOutBufferSize when the UFS device is shipped. |
| 09h | dDynCapNeeded | Read Only | 4 | 00h | Dynamic Capacity Needed<br>The amount of physical memory needed to be removed from the physical memory resource pool of the particular logical unit, in units of bOptimalWriteBlockSize. |
| 0Ah | bRefClkFreq | Read/ Persistent | 1 | 01h | Reference Clock Frequency Value<br>0h:19.2MHz<br>1h: 26MHz<br>2h: 38.4MHz<br>3h: 52MHz<br>Others: Reserved |
| 0Bh | bConfigDescrLock | Read/ Write Once | 1 | 00h | Configuration Descriptor Lock<br>0h: Configuration Descriptor not locked<br>1h: Configuration Descriptor locked<br>Others: Reserved |
| 0Ch | bMaxNumOfRTT | Read/ Persistent | 1 | 02h | Maximum current number of<br>outstanding RTTs in device that is allowed.<br>bMaxNumOfRTT shall not exceed the bDeviceRTTCap parameter.<br>This parameter can be written by the host only when all LU task queues are empty. |

| IDN | NAME | TYPE | Size [Byte] | MDV | Description |
|---|---|---|---|---|---|
| 0Dh | wExceptionEventControl | Read/ Volatile | 2 | 00h | Each bit, if set to '1' by the host, enables the assertion of the relevant exception event bit, allowing the device to raise the EVENT_ALERT bit in the Device Information field in the Response UPIU:<br>Bit 0: DYNCAP_EVENT_EN<br>Bit 1: SYSPOOL_EVENT_EN<br>Bit 2: URGENT_BKOPS_EN<br>Bit 3-4: Reserved<br>Bit 5: WRITEBOOSTER_EVENT_EN<br>Bit 6-15: Reserved |
| 0Eh | wExceptionEventStatus | Read Only | 2 | 00h | Each bit represents an exception event.<br>A bit will be set only if the relevant event has occurred (regardless of the wExceptionEventControl status).<br>Bit 0: DYNCAP_NEEDED<br>Bit 1: SYSPOOL_EXHAUSTED<br>Bit 2: URGENT_BKOPS<br>Bit 3-4: Reserved<br>Bit 5: WRITEBOOSTER_FLUSH_NEEDED<br>Bit 6-15: Reserved |
| 0Fh | dSecondsPassed | Write Only/ Volatile | 4 | 00h | Bit [31:0]: Seconds passed from TIME BASELINE (see wPeriodicRTCUpdate in Device Descriptor) |
| 10h | wContextConf | Read/ Volatile | 2 | 00h | INDEX specifies the LU number.<br>SELECTOR specifies the Context ID within the LU.<br>Valid range: 01h to 0Fh.<br>Bit [15:8]: RFU<br>Bit [7:6]: Reliability mode<br>00h: MODE0 (normal)<br>01h: MODE1 (non-Large Unit, reliable mode or Large Unit unit-by-unit mode)<br>02h: MODE2 (Large Unit, one-unit-tail mode)<br>03h: Reserved<br>Bit [5:3]: Large Unit multiplier.<br>If Large Unit context is set, this field defines the Large Unit size, else it is ignored<br>Bit [2]: Large Unit context<br>00b: Context is not following Large Unit rules<br>01b: Context follows Large Unit rules<br>Bit [1:0]: Activation and direction mode<br>00b: Context is closed and is no longer active.<br>01b: Context is configured and activated as a write-only context and according to the rest of the bits in this configuration register.<br>10b: Context is configured and activated as a read-only context and according to the rest of the bits in this configuration register.<br>11b: Context is configured and activated as a read/write context and according to the rest of the bits in this configuration register. |

| IDN | NAME | TYPE | Size [Byte] | MDV | Description |
|---|---|---|---|---|---|
| 11h | Obsoleted | Read Only | - | 00h | Obsoleted |
| 12h~13h | Reserved | | | | Reserved for Unified Memory Extension standard |
| 14h | bDeviceFFUStatus | Read Only | 1 | 00h | Device FFU Status<br>00h: No information<br>01h: Successful microcode update<br>02h: Microcode corruption error<br>03h: Internal error<br>04h: Microcode version mismatch<br>05h~FEh: Reserved<br>0FFh: General Error |
| 15h | bPSAState | Read/ Persistent | 1 | 00h | 00h: 'Off'. PSA feature is off.<br>01h: 'Pre-soldering'. PSA feature is on, device is in the pre-soldering state.<br>02h: 'Loading Complete' PSA feature is on.<br>The host will set to this value after the host finished writing data during pre-soldering state.<br>03h: 'Soldered'. PSA feature is no longer available.<br>Set by the Device to indicate it is in post soldering state.<br>This attributes unchangeable after it is in 'Soldered' state. |
| 16h | dPSADataSize | Read/ Persistent | 8 | 00 ...00 hh | The amount of data that the host plans to load to all logical units with bPSASensitive set to 1. |
| 1Ch | bWriteBoosterBufferFlushStatus | Read Only | 1 | 00h | Flush Operation status of writebooster Buffer<br>00h: IDLE. Device is not flushing the writebooster Buffer<br>01h: Flush Operation in progress<br>02h: Flush operation stopped prematurely by host's disabling flush enable flag or during hibernate flag<br>03h: Flush operation complete successfully<br>04h: Flush operation general failure<br>others: reserved |
| 1Dh | bAvailableWriteBoosterBufferSize | Read Only | 1 | 00h | Available writebooster Buffer size<br>this available buffer size is decreased by writebooster operation and increased by flush operation.<br>Value expressed in units of 10% granularity<br>00h: 0% buffer remains<br>01h~09h: 10%~90% buffer remains<br>0Ah: 100% buffer remains<br>Others: Reserved |

| IDN | NAME | TYPE | Size [Byte] | MDV | Description |
|---|---|---|---|---|---|
| 1Eh | bWriteBoosterBufferLifeTimeEst | Read Only | 1 | 00h | This field provides an indication of the writebooster Buffer lifetime based on the amount of performed program/erase cycle. In case of Preserve user space configuration for WriteBooster buffer, this lifetime will be reduced by writing on normal user level space, since Writebooster Buffer is shared with the user level space.<br>00h: Information not available<br>(writebooster Buffer is disabled)<br>01h: 0%~10% writebooster Buffer life time used<br>02h~09h 10%~90% writebooster Buffer life time used<br>0Ah: 90%~100% writebooster Buffer life time used<br>0Bh: Exceeded its maximum estimated WriteBooster Buffer life time<br>Others: Reserved |
| 1Fh | dCurrentWriteBoosterBufferSize | Read Only | 4 | 00h | The current WriteBooster Buffer size. in the case of preserve user space mode, depending on available user space remained, the storage block for the writebooster Buffer may be used for the user space. Therefore, the Writebooster Buffer size can be less than initially configured WriteBooster Buffer size. Host can check the current WriteBooster Buffer size by checking this attribute. Value expressed in unit of Allocation Units. If this value is 0, then the current WriteBooster Buffer size is 0, in the csae of user space reduction mode, this value shall be same to the value of dLUNumWriteBoosterBufferAllocUnits or dNumSharedWiteBoosterBufferAllocUnits depending on buffer configuration mode |

# 8. M-PHY & UniPro Attributes

## 8.1. M-TX Capability Attributes

MPHY capability attribute value in the table can be different from the value in the PACP_CAP_ind & PACP_CAP_EXT1_ind frame which is transmitted to the host during LinkStartUp. Some fields of PACP frame can be overwritten by FW.

| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ESC_PA | | | | | | | | EscParam_PA = PACP_BEGIN | | | | | | | |
| 0 | PACP_FunctionId = PACP_CAP_ind | | | | | | | | | | | | | | | |
| 0 | TSleepNoConfig | | | | Reserved | | | | | Flags | | MaxHS | | MaxPWM | | |
| 0 | TStallNoConfig | | | | | | | | TSaveConfig | | | | | | | |
| 0 | VersionInfo | | | | | | | | | | | | | | | |
| 0 | Reserved | | | | | | | | | | | | | | | |
| 0 | Reserved | | | | | | | | | | | | | | | |
| 0 | Reserved | | | | | | | | | | | | | | | |
| 0 | CCITT CRC-16 | | | | | | | | | | | | | | | |

**Figure 8 - PACP_CAP_ind**

| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ESC_PA | | | | | | | | EscParam_PA = PACP_BEGIN | | | | | | | |
| 0 | PACP_FunctionId = PACP_CAP_EXT1_ind | | | | | | | | | | | | | | | |
| 0 | THibern8 | | | | | | | | TMinActivate | | | | Status | | | |
| 0 | TAdvHibern8 | | | | | | | | TAdvMinActivate | | | | RxAdvGranularity | | | |
| 0 | MinRxTrailingClocks | | | | | | | | RxPwmBurstClosureLength | | | | | | | |
| 0 | RxLsPrepareLength | | | | | | | | RxPwmG6G7SyncLength | | | | | | | |
| 0 | RxHsG1PrepareLength | | | | | | | | RxHsG1SyncLength | | | | | | | |
| 0 | RxHsG2PrepareLength | | | | | | | | RxHsG2SyncLength | | | | | | | |
| 0 | RxHsG3PrepareLength | | | | | | | | RxHsG3SyncLength | | | | | | | |
| 0 | Reserved | | | | | | | | | | | | | | | |
| 0 | Reserved | | | | | | | | | | | | | | | |
| 0 | CCITT CRC-16 | | | | | | | | | | | | | | | |

**Figure 9 - PACP_CAP_EXT1_ind**

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_HSMODE_Capability | 0x01 | 01h | [0]: Specifies Support for HS-MODE.<br>0: False<br>1: True |
| TX_HSGEAR_Capability | 0x02 | 03h | [2:0]: Specifies supported HS-GEARS<br>00 – Reserved<br>01 – HS-GEAR1 Only<br>10 – HS-GEAR1 and HS-GEAR2<br>11 – HS-GEAR1, HS-GEAR2, and HS-GEAR3 |
| TX_PWMG0_Capability | 0x03 | 00h | PWM-G0 Capability<br>[0]: Specifies Support for PWM-G0<br>0 – NO<br>1 – YES |
| TX_PWMGEAR_Capability | 0x04 | 04h | [2:0]: Specifies supported PWM-GEARS other than PWM<br>000 – Reserved<br>001 – PWM-GEAR1 Only<br>010 – PWM-GEAR1 and PWM-GEAR2<br>011 – PWM-GEAR1 to PWM-GEAR3<br>100 – PWM-GEAR1 to PWM-GEAR4<br>101 – PWM-GEAR1 to PWM-GEAR5<br>110 – PWM-GEAR1 to PWM-GEAR6<br>111 – PWM-GEAR1 to PWM-GEAR7 |
| TX_Amplitude_Capability | 0x05 | 03h | [1:0]: Specifies supported signal amplitude levels<br>00 – Reserved<br>01 – SMALL AMPLITUDE Only<br>10 – LARGE AMPLITUDE Onlly<br>11 – LARGE and SMALL AMPLITUDE |
| TX_ExternalSYNC_Capability | 0x06 | 00h | [0]: Specifies support for external SYNC pattern.<br>0 – FALSE<br>1 – TRUE |
| TX_HS_Unterminated_ LINE_Drive_Capability | 0x07 | 01h | [0]: Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE.<br>0 – NO<br>1 – YES |
| TX_LS_Terminated_ LINE_Drive_Capability | 0x08 | 01h | Specifies whether or not M-TX supports driving an Terminated LINE in LS-MODE.<br>0 – NO<br>1 – YES |
| TX_Min_SLEEP_NoConfig_ Time_Capability | 0x09 | 0Fh | [3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.<br>Legal values are 0001 to 1111 (1 to 15) |
| TX_Min_STALL_NoConfig_Time _Capability | 0x0A | FFh | [7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.<br>Legal values are 8'h01 to 8'hFF (1 to 255) |
| TX_Min_SAVE_Config_ Time_Capability | 0x0B | FAh | [7:0] Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states<br>Legal values are 01h to FAh (1 to 250) which gives a Maximum time of 10000ns. |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_REF_CLOCK_ SHARED_Capability | 0x0C | 01h | [0]: Specifies support for shared reference clock.<br>0 – NO<br>1 – YES |
| TX_PHY_MajorMinor_ Release_Capability | 0x0D | 31h | Specifies the major and minor numbers of the M-PHY Version supported by the TX portion of M-PHY Version<br>[3:0]: Minor Version number. Fixed to 0x1<br>[7:4]: Major Version Number. Fixed to 0x3<br>The above values indicate that the M-PHY Version of the M-PHY Specification. |
| TX_PHY_Editorial_ Release_Capability | 0x0E | 01h | Specifies the sequence number of the M-Phy version<br>[7:0]: This value is fixed to 0x01. |
| TX_Hibern8Time_ Capability | 0x0F | 01h | [7:0]: Specifies the minimum time (in 100 us steps) in HIBERN8 State.<br>Legal values are 01h to 80h (1 to 128) which gives a range of 100us to 12.8ms. |
| TX_Advanced_ Granularity_Capability | 0x10 | 00h | Support and degree of fine granularity steps for a reduced time in HIBERN8 state. If a finer granularity is specified, all coarser granularities shall be supported.<br>[0]: supports fine granularity steps<br>0 – NO (100 µs step)<br>1 – YES<br>[2:1]: step size<br>00 – 4 µs<br>01 – 8 µs<br>10 – 16 µs<br>11 – 32 µs |
| TX_Advanced_ Hibern8time_Capability | 0x11 | 01h | Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Capability.<br>Existence depends on:<br>TX_Advanced_Granularity_Capability<br>[7:0] : 1 to 128 |
| TX_HS_Equalizer_ Setting_Capability | 0x12 | 03h | Support for transmit path de-emphasis for HS-MODE<br>Existence depends on: TX_HSMODE_Capability<br>[0] 0: De-emphasis of 3.5dB not supported,<br>1: De-emphasis of 3.5dB supported,<br>[1] 0: De-emphasis of 6dB not supported,<br>1: De-emphasis of 6dB supported |

## 8.2. M-RX Capability Attributes

| Attributes Name | Attribute ID | Default value | PACP_CAP value | Description |
|---|---|---|---|---|
| RX_HSMODE_Capability | 0x81 | 01h | 01h | [0]: Specifies Support for HS-MODE.<br>0: False<br>1: True |
| RX_HSGEAR_Capability | 0x82 | 03h | 03h | [2:0]: Specifies supported HS-GEARS<br>00 – Reserved<br>01 – HS-GEAR1 Only<br>10 – HS-GEAR1 and HS-GEAR2<br>11 – HS-GEAR1, HS-GEAR2, and HS-GEAR3 |
| RX_PWMG0_Capability | 0x83 | 00h | 00h | [0]: Specifies Support for PWM-G0<br>0 – NO<br>1 – YES |
| RX_PWMGEAR_Capability | 0x84 | 04h | 04h | [2:0]: Specifies supported PWM-GEARS other than PWM-G0<br>000 – Reserved<br>001 – PWM-GEAR1 Only<br>010 – PWM-GEAR1 to PWM-GEAR2<br>011 – PWM-GEAR1 to PWM-GEAR3<br>100 – PWM-GEAR1 to PWM-GEAR4<br>101 – PWM-GEAR1 to PWM-GEAR5<br>110 – PWM-GEAR1 to PWM-GEAR6<br>111 – PWM-GEAR1 to PWM-GEAR7 |
| RX_HS_Unterminated_Capability | 0x85 | 01h | 01h | [0]: Specifies support for disconnection of resistive termination in HS-MODE.<br>0 – NO<br>1 – YES |
| RX_LS_Terminated_Capability | 0x86 | 01h | 01h | [0]: Specifies support for enabling resistive termination in LSMode.<br>0 – NO<br>1 – YES |
| RX_Min_SLEEP_NoConfig_ Time_Capability | 0x87 | 0Fh | 0Fh | [3:0]: Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed. Legal values are 0x01 to 0x0F (1 to 15) |
| RX_Min_STALL_NoConfig_ Time_Capability | 0x88 | FFh | FFh | [7:0]: Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed. Legal values are 0x01 to 0xFF (1 to 255) |
| RX_Min_SAVE_Config_ Time_Capability | 0x89 | FAh | FAh | Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.<br>[7:0]: Specifies minimum reconfiguration time (in 40ns steps). This applies to SLEEP and STALL states Legal values are 01h to FAh (1 to 250)<br>which gives a maximum time of 10000ns. |

| Attributes Name | Attribute ID | Default value | PACP_CAP value | Description |
|---|---|---|---|---|
| RX_REF_CLOCK_ SHARED_Capability | 0x8A | 01h | 01h | [0]: Specifies support for shared reference clock<br>0 – NO<br>1 – YES |
| RX_HS_G1_SYNC_ LENGTH_Capability | 0x8B | 48h | 48h | HSG1 Synchronization pattern length in SI<br>[5:0]: Sync Length<br>1 to 15 for FINE<br>0 to 15 for COARSE<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE |
| RX_HS_G1_PREPARE_ LENGTH_Capability | 0x8C | 0Fh | 0Fh | [3:0]: HS GEAR1 PREPARE Length Multiplier for M-RX (0 to 15) |
| RX_LS_PREPARE_LENGTH_ Capability | 0x8D | 0Ah | 0Ah | [3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for M-RX (0 to 15) |
| RX_PWM_Burst_Closure_ Length_Capability | 0x8E | 1Fh | 1Fh | Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX |
| RX_Min_ActivateTime_ Capability | 0x8F | 01h | 03h | [3:0]: Specifies minimum activate time needed in 100us steps (1 to 9) |
| RX_PHY_MajorMinor_ Release_Capability | 0x90 | 31h | 31h | Specifies the major and minor numbers of the M-PHY<br>[3:0]: Minor Version Number. Fixed to 0x1<br>[7:4]: Major Version Number. Fixed to 0x3<br>Version of the M-PHY Specification. |
| RX_PHY_Editorial_ Release_Capability | 0x91 | 01h | 01h | Specifies the sequence number of the M-PHY version<br>[7:0]: This value is fixed to 0x01. |
| RX_Hibern8Time_ Capability | 0x92 | 01h | 01h | [7:0]: Specifies the minimum time (in 100us steps) in HIBERN8 State.<br>Legal values are 0x01 to 0x80 (1 to 128) which gives a range of 100us to 12.8ms.<br>Even though RX_Hibern8Time_Capability is 0x1, it sends THibern8 in PACP_CAP_EXT1_ind |
| RX_PWM_G6_G7_SYNC_ LENGTH_Capability | 0x93 | 00h | 00h | Synchronization pattern length, in SI, for PWM-G6 and PWM-G7 in LS-MODE .<br>Existence depends on: RX_PWMGEAR_Capability<br>[5:0]: Sync Length (0 to 15)<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE<br>Does not support PWMG6/G7 |
| RX_HS_G2_SYNC_ LENGTH_Capability | 0x94 | 48h | 48h | High Speed GEAR 2 Synchronization pattern length in SI.<br>Existence depends on: RX_HSGEAR_Capability<br>[5:0]: Sync Length (0 to 15)<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE |

| Attributes Name | Attribute ID | Default value | PACP_CAP value | Description |
|---|---|---|---|---|
| RX_HS_G3_SYNC_ LENGTH_Capability | 0x95 | 48h | 48h | High Speed GEAR 3 Synchronization pattern length in SI.<br>Existence depends on: RX_HSGEAR_Capability<br>[5:0]: Sync Length<br>1 to 15 for FINE<br>0 to 15 for COARSE<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE |
| RX_HS_G2_PREPARE_ LENGTH_Capability | 0x96 | 0Fh | 0Fh | HS-G2 PREPARE length multiplier for M-RX.<br>Existence depends on: RX_HSGEAR_Capability<br>[3:0]: 0 to 15<br>[7:4]: Reserved |
| RX_HS_G3_PREPARE_ LENGTH_Capability | 0x97 | 0Fh | 0Fh | HS-G3 PREPARE length multiplier for M-RX.<br>Existence depends on: RX_HSGEAR_Capability<br>[3:0]: 0 to 15<br>[7:4]: Reserved |
| RX_advanced_ granularity_capability | 0x98 | 00h | 00h | Support and degree of fine granularity steps for THIBERN8 and TACTIVATE.<br>[0] Supports fine granularity steps<br>0 : No (100 µs step)<br>1 : Yes<br>[2:1] Step size<br>00 : 4 µs<br>01 : 8 µs<br>10 : 16 µs<br>11 : 32 µs<br>Even though RX_Advanced_Granularity_Capability is 0x1, it sends RxAdvGranularity in PACP_CAP_EXT1 _ind |
| RX_advanced_ hibern8time_capability | 0x99 | 01h | 01h | Specifies minimum time in HIBERN8 state when advanced granularity is supported in steps defined by RX_advanced_Granularity_Capability.<br>Existence depends on:<br>RX_Advanced_Granularity_Capability<br>Range : 1 to 128<br>Even though RX_Advanced_Hibern8Time_Capability is 0x4, it sends TAdvHibern8 in PACP_CAP_EXT1_ind with 0x7 |
| RX_advanced_min_ activatetime_capability | 0x9A | 01h | 01h | Specifies minimum activate time when advanced granularity is supported in steps defined by RX_Advanced_Granularity_Capability.<br>Existence depends on:<br>RX_Advanced_Granularity_Capability<br>Range : 1 to 14<br>Even though<br>RX_Advanced_Min_ActivateTime_Capability is 0x7, it sends TAdvMinActivate in PACP_CAP_EXT1_ind with 0x7 |

## 8.3. M-TX Configuration Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_MODE | 0x21 | 01h | [1:0]: M-TX operating mode.<br>01: LS_MODE<br>10: HS_MODE<br>(default: LS_MODE) |
| TX_HSRATE_Series | 0x22 | 01h | [1:0]: HS mode RATE series value of M-TX.<br>01: RATE-A<br>10: RATE-B<br>(default: RATE-A) |
| TX_HSGEAR | 0x23 | 01h | [1:0]: HS-GEAR value of M-TX.<br>01: HS-GEAR1<br>10: HS-GEAR2<br>11: HS-GEAR3<br>(default: HS-GEAR1) |
| TX_PWMGEAR | 0x24 | 01h | [2:0]: PWM-GEAR value of M-TX.<br>000: PWM-GEAR0<br>001: PWM-GEAR1<br>010: PWM-GEAR2<br>011: PWM-GEAR3<br>100: PWM-GEAR4<br>101: PWM-GEAR5<br>110: PWM-GEAR6<br>111: PWM-GEAR7<br>(default: PWM-GEAR1) |
| TX_Amplitude | 0x25 | 02h | [0]: Controls the Drive Strength of the AFE Outputs on Transmit.<br>01: SMALL_AMPLITUDE<br>10: LARGE_AMPLITUDE<br>(default: LARGE_AMPLITUDE)<br>Other vendor specific MPHY attributes should be programmed to changed TX amplitude, Please contact SKH to change TX Amplitude. |
| TX_HS_SlewRate | 0x26 | 00h | HS Slew Rate [7:0]: Controls the Slew Rate of M-TX.<br>Does not support for this version.<br>Instead of Slew Rate control, limited slew rate adopted for EMI reduction. |
| TX_SYNC_Source | 0x27 | 00h | [0]: Source of Synchronization Pattern at M-TX.<br>0: INTERNAL_SYNC<br>1: EXTERNAL_SYNC |
| TX_HS_SYNC_LENGTH | 0x28 | 4Fh | HS mode Synchronization Pattern Length.<br>[5:0]: Sync Length (0 to 15)<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE<br>(default: COARSE, 15) |
| TX_HS_PREPARE_LENGTH | 0x29 | 0Fh | [3:0]: HS PREPARE Length Multiplier for M-TX. (0 to 15)<br>(default: 15) |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_LS_PREPARE_LENGTH | 0x2A | 0Ah | [3:0]: PWM-Burst or SYS-Burst PREPARE Length Multiplier for M-TX. (0 to 15)<br>(default: 10) |
| TX_HIBERN8_Control | 0x2B | 01h | [0]: M-TX HIBERN8 state control.<br>0: EXIT<br>1: ENTER<br>Note: After LINE-RESET condition, the value is reset to EXIT state.<br>(default: ENTER) |
| TX_LCC_Enable | 0x2C | 00h | [0]: Enables the Transmission of LCC at the end of Burst.<br>0: NO<br>1: YES<br>[7:1]: Reserved<br>(default: YES) |
| TX_PWM_BURST_Closure_ Extension | 0x2D | 20h | [7:0]: BURST CLOSURE sequence duration in SI. (0 to 255)<br>(default: 32) |
| TX_BYPASS_8B10B_Enable | 0x2E | 00h | [0]: Bypass 8b10b Encoding operation at M-TX.<br>0: FALSE<br>1: TRUE<br>[7:1]: Reserved<br>(default: FALSE) |
| TX_DRIVER_POLARITY | 0x2F | 00h | Output Driver Polarity<br>[0]: Output Driver Polarity<br>0: NORMAL<br>1: INVERTED<br>[7:1]: Reserved<br>(default: NORMAL) |
| TX_HS_Unterminated_ LINE_Drive_Enable | 0x30 | 00h | [0]: Enables/Disables the unterminated LINE in HS-MODE.<br>0: NO<br>1: YES<br>[7:1]: Reserved<br>(default: NO) |
| TX_LS_Terminated_ LINE_Drive_Enable | 0x31 | 00h | [0]: Enables/Disables the terminated LINE in LS-MODE.<br>0: NO<br>1: YES<br>[7:1]: Reserved<br>(default: NO) |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_LCC_Sequencer | 0x32 | 00h | LCC Sequencer bits<br>[0]: LCC READ-CAPABILITY<br>0: Not Requested<br>1: Requested<br>[1]: LCC READ-MFG-INFO<br>0: Not Requested<br>1: Requested<br>[2]: LCC READ-VEND-INFO<br>0: Not Requested<br>1: Requested<br>[6:3]: Reserved<br>[7]: LCC WRITE-ATTRIBUTE<br>0: Not Requested<br>1: Requested<br>(default: No READ or WRITE operation Requested) |
| TX_Min_ActivateTime | 0x33 | 0Fh | [3:0]: Specifies minimum activate time needed in 100us steps (1 to 15)<br>[7:4]: Reserved<br>(default: 15) |
| TX_PWM_G6_G7_SYNC_ LENGTH | 0x34 | 4Fh | PWM G6/G7 mode Synchronization Pattern Length.<br>[5:0]: Sync Length (0 to 15)<br>[7:6]: SYNC Range<br>00: FINE<br>01: COARSE<br>(default: COARSE, 15)<br>Does not support PWMG6/G7. |
| TX_Advanced_ Granularity_Step | 0x35 | 00h | Support and degree of fine granularity steps for TACTIVATE<br>Reset Value: 0<br>[0]: Supports advanced granularity<br>0: NO<br>1: YES<br>[2:1] step size<br>00 = 4 µs<br>01 = 8 µs<br>10 = 16 µs<br>11 = 32 µs<br>Others : Reserved |
| TX_Advanced_Granularity | 0x36 | 01h | Specifies minimum activate time when advanced granularity is supported in steps defined by TX_Advanced_Granularity_Step.<br>[3:0]: 1 to 15<br>Others: Reserved<br>Advanced granularity is not supported |
| TX_HS_Equalizer_Setting | 0x37 | 00h | HS Transmit path de-emphasis value selection.<br>Existence depends on: TX_HSMODE_Capability AND TX_HS_Equalizer_Setting_Capability<br>Value depends on: TX_HS_Equalizer_Setting_Capability<br>Required Values: Support for de-emphasis of 3.5 dB or 6 dB<br>Reset Value: 0 for local RESET.<br>LINE-RESET shall not reset the value of this attribute. |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_MIN_SLEEP_NOCONFIG_ TIME | 0x38 | 0Fh | This amount of time(in SI) ensures remote MRX has transitioned to termination disable entering SLEEP.<br>Set greater than or equal to remote RX_MIN_SLEEP_NOCONFIG_TIME_CAPABILITY.<br>This attribute newly added at v3.1<br>Default value is 0Fh, but this value is overwritten '00h' by FW. |
| TX_MIN_STALL_NOCONFIG_ TIME | 0x39 | FFh | This amount of time(in SI) ensures remote MRX has transitioned to termination disable entering STALL.<br>Set greater than or equal to remote RX_MIN_STALL_NOCONFIG_TIME_CAPABILITY.<br>This attribute newly added at v3.1 |

## 8.4. M-RX Configuration Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| RX_MODE | 0xA1 | 01h | [1:0]: Operating mode.<br>01: LS_MODE<br>10: HS_MODE<br>(default: LS_MODE) |
| RX_HSRATE_Series | 0xA2 | 01h | [1:0]: HS mode rate series value.<br>01: RATE-A<br>10: RATE-B<br>(default: RATE-A) |
| RX_HSGEAR | 0xA3 | 01h | [1:0]: Current HS-Gear.<br>01: HS-GEAR1<br>10: HS-GEAR2<br>11: HS-GEAR3<br>(default: HS-GEAR1) |
| RX_PWMGEAR | 0xA4 | 01h | [2:0]: Current PWM-GEAR.<br>000: PWM-GEAR0<br>001: PWM-GEAR1<br>010: PWM-GEAR2<br>011: PWM-GEAR3<br>100: PWM-GEAR4<br>101: PWM-GEAR5<br>110: PWM-GEAR6<br>111: PWM-GEAR7<br>(default: PWM-GEAR1) |
| RX_LS_Terminated_Enable | 0xA5 | 00h | [0]: Enables/Disables the resistive termination of Receive in LS-MODE.<br>0: OFF<br>1: ON<br>(default: OFF) |
| RX_HS_Unerminated_Enable | 0xA6 | 00h | [0]: Enables/Disables the resistive termination of Receive in HS-MODE.<br>0: OFF<br>1: ON<br>(default: OFF) |
| RX_Enter_HIBERN8 | 0xA7 | 01h | [0]: M-RX Entry to HIBERN8 State control.<br>0: NO<br>1: YES<br>Note: After LINE-RESET condition, the value is reset to NO state.<br>(default: YES) |
| RX_BYPASS_8B10B_Enable | 0xA8 | 00h | [0]: Bypass 8b10b decoding at the M-RX.<br>0: FALSE<br>1: TRUE<br>(default: FALSE) |
| RX_Termination_Force_Enable | 0xA9 | 00h | Force connection of differential termination resistance, RDIF_RX, to enabled state, for RX S-Parameter test purposes.<br>0: NO<br>1: YES |

## 8.5. M-TX & M-RX Status Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| TX_FSM_State | 0x41 | 01h | [3:0]: Current State of M-TX<br>000: DISABLED<br>001: HIBERN8<br>010: SLEEP<br>011: STALL<br>100: LS-BUSRT<br>101: HS-BURST<br>110: LINE-CFG<br>111: LINE-RESET |
| RX_FSM_State | 0xC1 | 01h | [3:0]: Current State of M-RX.<br>000: DISABLED<br>001: HIBERN8<br>010: SLEEP<br>011: STALL<br>100: LS-BUSRT<br>101: HS-BURST<br>110: LINE-CFG<br>111: LINE-RESET |

## 8.6. UniPro L1.5 Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| PA_PHY_Type | 0x1500 | 01h | PHY Type |
| PA_AvailTxDataLanes | 0x1520 | 02h | Available TX Data Lanes |
| PA_AvailRxDataLanes | 0x1540 | 02h | Available RX Data Lanes |
| PA_MinRxTrailingClocks | 0x1543 | 84h | Minimum number of PHY byte clock cycles without data to receive before a mode change from FAST_STATE or SLOW_STATE to SLEEP_STATE, or before a pause in data transmission while in FAST_STATE or SLOW_STATE. |
| PA_TxHsG1SyncLength | 0x1552 | 4Fh | Start of Burst: High Speed Synchronization pattern Length in HS-G1, follows MPHY 3.1 Spec definition for TX_HS_SYNC_LENGTH |
| PA_TxHsG1PrepareLength | 0x1553 | 0Fh | Start of Burst: Minimum Prepare time in HS-G1, follows MPHY 3.1 Spec definition for TX_HS_PREPARE_LENGTH |
| PA_TxHsG2SyncLength | 0x1554 | 4Fh | Start of Burst: High Speed Synchronization pattern Length in HS-G2, follows MPHY 3.1 Spec definition for TX_HS_SYNC_LENGTH |
| PA_TxHsG2PrepareLength | 0x1555 | 0Fh | Start of Burst: Minimum Prepare time in HS-G2, follows MPHY 3.1 Spec definition for TX_HS_PREPARE_LENGTH |
| PA_TxHsG3SyncLength | 0x1556 | 4Fh | Start of Burst: High Speed Synchronization pattern Length in HS-G3, follows MPHY 3.1 Spec definition for TX_HS_SYNC_LENGTH |
| PA_TxHsG3PrepareLength | 0x1557 | 0Fh | Start of Burst: Minimum Prepare time in HS-G3, follows MPHY 3.1 Spec definition for TX_HS_PREPARE_LENGTH |
| PA_TxMk2Extension | 0x155A | 0h | Peer supports MK2 signaling (inbound direction) |
| PA_PeerScrambling | 0x155B | 0h | Peer supports scrambling |
| PA_TxSkip | 0x155C | 0h | Peer indicates requirement for skip symbol insertion (Set during link startup) |
| PA_TxSkipPeriod | 0x155D | FAh | A skip symbol <MK4,MK4> shall be inserted at least every interval with a number of PA_PDUs equal to PA_TxSkipPeriod. The value 250 should correspond to +/-2000ppm difference between local and remote. |
| PA_LocalTxLccEnable | 0x155E | 00h | Local MPHY Line Configuration Enable. |
| PA_PeerTxLccEnable | 0x155F | 00h | Peer M-PHY Line Configuration Enable, updated on reception of PACP_CAP_EXT1_ind frame. |
| PA_ActiveTxDataLanes | 0x1560 | 01h | Active TX Data Lanes |
| PA_ConnectedTxDataLanes | 0x1561 | 00h | Number of TX Data Lanes connected Shall be updated after LinkStartUp |
| PA_TxTrailingClocks | 0x1564 | FFh | Number of PHY byte clock cycles forced without data before a mode change from FAST_STATE or SLOW_STATE to SLEEP_STATE. |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| PA_TxPWRStatus | 0x1567 | 3h | TX power state status<br>000 : Off state<br>001 : Fast state<br>010 : Slow state<br>011 : Hibernate state<br>100 : Sleep state |
| PA_TxGear | 0x1568 | 1h | TX Gear in PWM or HS Mode<br>001 : PWM_G1 or HS_G1<br>010 : PWM_G2 or HS_G2<br>011 : PWM_G3 or HS_G3<br>100 : PWM_G4<br>101 : PWM_G5<br>110 : PWM_G6<br>111 : PWM_G7 |
| PA_TxTermination | 0x1569 | 0h | FALSE - 0<br>TRUE - 1 |
| PA_HSSeries | 0x156A | 1h | TX and RX Frequency Series in High Speed Mode<br>A-1<br>B-2 |
| PA_PWRMode | 0x1571 | 55h | TX/RX power mode<br>TX[b3:b0]<br>RX[b7:b4]<br>0000 : Off mode<br>0001 : Fast mode<br>0010 : Slow mode<br>0100 : Fast auto mode<br>0101 : Slow auto mode<br>1111 : UNCHANGED. |
| PA_ActiveRxDataLanes | 0x1580 | 01h | Active RX Data Lanes<br>1 - one lane active<br>2 - two lanes active<br>3 - three lanes active<br>4 - four lanes active |
| PA_ConnectedRxDataLanes | 0x1581 | 00h | Number of RX Data Lanes connected<br>0 - not connected<br>1 - 1 lane<br>2 - 2 lanes<br>3 - 3 lanes<br>4 - 4 lanes<br>Shall be updated after LinkStartUp |
| PA_RxPWRStatus | 0x1582 | 3h | RX power state status<br>000 : Off state<br>001 : Fast state<br>010 : Slow state<br>011 : Hibernate state<br>100 : Sleep state |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| PA_RxGear | 0x1583 | 1h | RX Gear in PWM or HS Mode<br>001 : PWM_G1 or HS_G1<br>010 : PWM_G2 or HS_G2<br>011 : PWM_G3 or HS_G3<br>100 : PWM_G4<br>101 : PWM_G5<br>110 : PWM_G6<br>111 : PWM_G7 |
| PA_RxTermination | 0x1584 | 0h | RX Termination |
| PA_Scrambling | 0x1585 | 0h | Scrambling Request. |
| PA_MaxRxPWMGear | 0x1586 | 01h | Maximum RX Low Speed Gears (PWM)<br>001 : PWM_G1<br>010 : PWM_G2<br>011 : PWM_G3<br>100 : PWM_G4<br>101 : PWM_G5<br>110 : PWM_G6<br>111 : PWM_G7<br>Shall be updated to 04h after Controller Initialization |
| PA_MaxRxHSGear | 0x1587 | 00h | Maximum RX High Speed Gears (HS), 0 means no HS available<br>00 : NO_HS<br>01 : HS_G1<br>10 : HS_G2<br>11 : HS_G3<br>Shall be updated to 03h after Controller Initialization |
| PA_PACPReqTimeout | 0x1590 | 3Fh | Expiration value of the PACP_REQUEST_TIMER when the PA Layer is waiting for a cnf Message The actual duration of the timeout period shall be the value set in the Attribute ±10% |
| PA_PACPReqEoBTimeout | 0x1591 | 0Fh | Expiration value of the PACP_REQUEST_TIMER when the PA Layer is waiting for the end of burst.<br>The actual duration of the timeout period shall be the value set in the Attribute ±10% |
| PA_RemoteVerInfo | 0x15A0 | 00h | Peer Device version information. Available after a successful Link StartUp Sequence. |
| PA_LogicalLaneMap | 0x15A1 | 00h | Logical to Physical Lane mapping.<br>Shall be updated after LinkStartUp |
| PA_SleepNoConfigTime | 0x15A2 | 0Fh | Minimum time to wait between bursts in PWM mode when no new configuration was performed. |
| PA_StallNoConfigTime | 0x15A3 | FFh | Minimum time to wait between bursts in HS mode when no new configuration was performed. |
| PA_SaveConfigTime | 0x15A4 | FAh | Minimum time to wait between bursts when a new Configuration was performed. |
| PA_<br>RxHSUnterminationCapability | 0x15A5 | 00h | Specifies whether or not the inbound Link supports unterminated line in HS mode<br>0 - FALSE<br>1 - TRUE |

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| PA_ RxLSTerminationCapability | 0x15A6 | 0h | Specifies whether or not the inbound Link supports terminated line in PWM mode. |
| PA_Hibern8Time | 0x15A7 | 80h | Minimum time to wait in HIBERN8 before allowing a M-TX to exit HIBERN8. |
| PA_TActivate | 0x15A8 | 10h | Time to wait in SAVE before activating a burst in order to wake up OMC and remote M-RX. |
| PA_LocalVerInfo | 0x15A9 | 05h | Local version info. Delivered during Link Startup Sequence to the peer Device and stored in PA_RemoteVerInfo in the peer Device. |
| PA_Granularity | 0x15AA | 06h | Granularity for PA_TActivate and PA_Hibern8Time |
| PA_MK2ExtensionGuardBand | 0x15AB | 00h | MK2 extension time. The unit is PA_Granularity. |
| PA_PWRModeUserData [0 to 11] | 0x15B0 to 0x15BB | 00h | Data to be sent within PACP_PWR_req and delivered to the remote DME. |
| PA_PACPFrameCount | 0x15C0 | 00h | Number of valid PACP frames received. |
| PA_PACPErrorCount | 0x15C1 | 00h | Number of erroneous PACP frames received. |
| PA_PHYTestControl | 0x15C2 | 00h | PHY Test Feature control register.<br>b0: ContBurst<br>b1: CfgReady<br>b2: LineReset<br>b3: TestPattern Transmit<br>b4: TestPattern Select |

## 8.7. UniPro L2 Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| DL_TxPreemptionCap | 0x2000 | 1b | Preemption capability on transmit side for both Traffic Classes. |
| DL_TC0TxMaxSDUSize | 0x2001 | 90h | TC0 Transmitter Maximum SDU Size |
| DL_TC0RxInitCreditVal | 0x2002 | 7Ch | TC0 Receiver Initial Credit Value (initial register A value) |
| DL_TC1TxMaxSDUSize | 0x2003 | 90h | TC1 Transmitter Maximum SDU Size |
| DL_TC1RxInitCreditVal | 0x2004 | 0h | TC1 Receiver Initial Credit Value (initial register A value) |
| DL_TC0TxBufferSize | 0x2005 | 76h | TC0 Transmitter Buffer Size |
| DL_TC1TxBufferSize | 0x2006 | 0h | TC1 Transmitter Buffer Size |
| DL_TC0TXFCThreshold | 0x2040 | 09h | Threshold for triggering an AFC0 Frame with CReq bit set to '1' to request flow control update from remote end.<br>This Attribute is retained during hibernate. |
| DL_FC0ProtectionTimeOutVal | 0x2041 | 1FFFh | Expiration value of the FC0_PROTECTION_TIMER<br>The actual duration of the timeout period shall<br>be the value set in the Attribute ±10%.<br>A value of zero means "OFF"<br>This Attribute is retained during hibernate. |
| DL_TC0ReplayTimeOutVal | 0x2042 | FFFFh | Expiration value of the TC0_REPLAY_TIMER<br>The actual duration of the timeout period shall be the value set in the Attribute ±10%. A value of zero means "OFF" This Attribute is retained during hibernate. |
| DL_AFC0ReqTimeOutVal | 0x2043 | 7FFFh | Expiration value of the AFC0_REQUEST_TIMER<br>The actual duration of the timeout period shall be the<br>value set in the Attribute ±10%. A value of zero means "OFF"<br>This Attribute is retained during hibernate. |
| DL_AFC0CreditThreshold | 0x2044 | 00h | Threshold for AFC0 triggering based on available TC0 credits at receiver. This Attribute is retained during hibernate. |
| DL_TC0OutAckThreshold | 0x2045 | 00h | Number of outstanding acknowledgments for TC0 |
| DL_PeerTC0Present | 0x2046 | 00h | Peer Device supports TC0 |
| DL_PeerTC0RxInitCreditVal | 0x2047 | 00h | Peer TC0 Receiver Initial Credit Value<br>(initial register A value) |
| DL_PeerTC1Present | 0x2066 | 00h | Peer Device supports TC1 |
| DL_PeerTC1RxInitCreditVal | 0x2067 | 00h | Peer TC1 Receiver Initial Credit Value<br>(initial register A value) |

## 8.8. UniPro L3 Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| N_DeviceID | 0x3000 | 01h | Local Device ID. UFS Device is 01h |
| N_DevieID_valid | 0x3001 | 1b | N_Device ID attribute is valid.<br>1 - True<br>0 - False |
| N_TC0TxMaxSDUSize | 0x3020 | 111h | Maximum Transmit payload size per packet for TC0 |
| N_TC1TxMaxSDUSize | 0x3021 | 111h | Maximum Transmit payload size per packet for TC1 |

## 8.9. UniPro L4 Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| T_NumCports | 0x4000 | 01h | No. of available cports |
| T_NumTestFeatures | 0x4001 | 01h | No. of available Test Feature instances |
| T_ConnectionState | 0x4020 | 01h | State of the connection |
| T_PeerDeviceID | 0x4021 | 00h | Device id of the peer cport |
| T_PeerCportID | 0x4022 | 00h | CPortID of the peer cport |
| T_TrafficClass | 0x4023 | 00h | Traffic Class of current connection |
| T_CPortFlags | 0x4025 | 6h | E2E_FC off, CSD off, CSV off |
| T_TxTokenValue | 0x4026 | 20h | Value of E2E FC Token transmitted |
| T_RxTokenValue | 0x4027 | 20h | Value of E2E FC Token received |
| T_LocalBufferSpace | 0x4028 | 00h | Amount of local buffer space |
| T_PeerBufferSpace | 0x4029 | 00h | Conservative value of amount of buffer space at the peer cport |
| T_CreditsToSend | 0x402A | 00h | Amount of space in the local buffer that has not been communicated to remote destination port yet |
| T_CportMode | 0x402B | 01h | Cport mode ..<br>1 - Application<br>2 - Test mode |
| T_TC0TxMaxSDUSize | 0x4060 | 110h | Maximum Transmit payload size per segment for TC0 |

## 8.10. UniPro DME DDB L1 Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| DME_DDBL1_Revision | 0x5000 | 10h | The revision of the DDB Specification supported by this Device encoded as major-version * 0x10 + minor-version. The value shall be 0x10. (DDB v1.0). |
| DME_DDBL1_Level | 0x5001 | 01h | Eight bit field indicating the DDB support:<br>b0: DDB Level 1 support. Shall be 0b1.<br>b1: DDB Level 2 get support. Shall be 0b1 if, and only if, the GET-DDB-LEVEL2 Service is supported. If b1 is set to '1', then b0 shall also be set to '1'.<br>b2: DDB Level 2 set support. Shall be 0b1 if, and only if, the SET-DDB-LEVEL2 Service is supported. If b2 is set to '1', both b0 and b1 shall also be set to '1'.<br>b[7:3]: Reserved. Shall be 0b00000. |
| DME_DDBL1_DeviceClass | 0x5002 | 02h | The Device Class ID of the DME User as specified by the MIPI Alliance. If the Device does not conform to a specified device class, the value shall be zero |
| DME_DDBL1_ManufacturerID | 0x5003 | 24Ah | Manufacturer ID of the DME User as specified by the MIPI Alliance. |
| DME_DDBL1_ProductID | 0x5004 | A00h | The Manufacturer's internal product ID of the DME User. |
| DME_DDBL1_Length | 0x5005 | 00h | The length of any DDB Level 2 data.<br>For Devices supporting only DDB Level 1, the value shall be zero. |

## 8.11. UniPro TstSrc/TstDst Attributes

| Attributes Name | Attribute ID | Default value | Description |
|---|---|---|---|
| T_TstCPortID | 0x4080 | 00h | The ID of the CPort-under-test |
| T_TstSrcOn | 0x4081 | 00h | Message generation state |
| T_TstSrcPattern | 0x4082 | 00h | Pattern used for Message generation |
| T_TstSrcIncrement | 0x4083 | 01h | The increment value between two consecutive bytes |
| T_TstSrcMessageSize | 0x4084 | 100h | The size of each generated Message |
| T_TstSrcMessageCount | 0x4085 | 100h | The number of Messages generated<br>(Nonzero: finite Message stream,<br>zero: infinite Message stream). |
| T_TstSrcInterMessageGap | 0x4086 | 00h | If non-zero, the gap time between two Messages<br>The actual duration of the timeout period shall be the value set in the attribute ±10%.<br>This value multiplied by SYS1CLK 1us Register (0x0FC) gives the no. of clocks Required |
| T_TstDstOn | 0x40A1 | 00h | The state of TstDst |
| T_TstDstErrorDetectionEnable | 0x40A2 | 00h | Enable analyzing incoming Messages |
| T_TstDstPattern | 0x40A3 | 00h | The expected pattern in the incoming Messages |
| T_TstDstIncrement | 0x40A4 | 01h | The expected increment value between two consecutive bytes |
| T_TstDstMessageCount | 0x40A5 | 00h | Number of received Messages |
| T_TstDstMessageOffset | 0x40A6 | 00h | Offset of error from start of Message |
| T_TstDstMessageSize | 0x40A7 | 100h | The expected size of incoming Message |
| T_TstDstFCCredits | 0x40A8 | 100h | The amount of credits passed to the flow control Service Primitive |
| T_TstDstInterFCTokenGap | 0x40A9 | 00h | The interval in microseconds for<br>which requesting T_CO_FLOWCONTROL. req is skipped.<br>The actual duration of the timeout period shall be the value set in the attribute ±10%.<br>This value multiplied bySYS1CLK 1us<br>Register(0x0FC) gives the no. of clocks required |
| T_TstDstInitialFCCredits | 0x40AA | 100h | The initial number of credits passed by the TstDst to T_CO_FLOWCONTROL.req after enabling the TstDst |
| T_TstDstErrorCode | 0x40AB | 00h | Error code that generated the TstDst disconnection<br>0 - NO_ERROR<br>1 - FRAGMENT_CORRUPT<br>2 - INVALID_MSG_SIZE<br>3 - UNEXPECTED_BYTE_VALUE |

## 8.12. Product Name String Descriptor

| OFFSET | SIZE | NAME | 64GB | Description |
|---|---|---|---|---|
| 00h | 1 | bLength | 22h | Size of this Descriptor |
| 01h | 1 | bDescriptorIDN | 05h | Type Identifier |
| 02h | 2 | UC[0] | 0048h | "H" |
| 04h | 2 | UC[1] | 0039h | "9" |
| 06h | 2 | UC[2] | 0048h | "H" |
| 08h | 2 | UC[3] | 0051h | "Q" |
| 0Ah | 2 | UC[4] | 0035h | "5" |
| 0Ch | 2 | UC[5] | 0034h | "4" |
| 0Eh | 2 | UC[6] | 0041h | "A" |
| 10h | 2 | UC[7] | 0043h | "C" |
| 12h | 2 | UC[8] | 0050h | "P" |
| 14h | 2 | UC[9] | 004Dh | "M" |
| 16h | 2 | UC[10] | 004Dh | "M" |
| 18h | 2 | UC[11] | 0044h | "D" |
| 1Ah | 2 | UC[12] | 0041h | "A" |
| 1Ch | 2 | UC[13] | 0052h | "R" |
| 1Eh | 2 | UC[14] | 0000h | NULL |
| 20h | 2 | UC[15] | 0000h | NULL |

# LPDDR4x Specification
# (x16)

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## Revision History

| Version | Description | Date | Remark |
|---|---|---|---|
| 1.0 | Updates<br>- Notes in 1.2. "Simplified State Diagram"<br>- Data patterns in 7.1. "IDD Measurement Conditions"<br>- Timing diagram in 2.50. "Post Package Repair - PPR"<br>- Notes in 4.1. "Recommended DC Operating Conditions"<br><br>Added in this version<br>- PPRP, SREF abort and Thermal offset information in 1.4. "Mode Register Definition"<br>- 2.5. "Read Preamble and Postamble"<br>- 2.7.1. "tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation"<br>- 2.9. "Write Preamble and Postamble"<br>- 2.11. "Write Timing"<br>- 2.14. "Postamble and Preamble merging behavior"<br>- 2.22. "MRR, MRW, MPC Command during tXSR, tRFC"<br>- tWLWPRE definition in 2.30. "Mode Register Write-WR Leveling Mode"<br>- tMPCWR definition in 2.32. "DQS-DQ Training"<br>- 2.36. "Thermal offset"<br>- 4.2. "Input Leakage Current"<br>- 4.3. "Input/Output Leakage Current"<br>- 5.2.1. "Differential Input Voltage for CK"<br>- 5.2.6. "Differential Input Voltage for DQS"<br><br>- Other editorial changes | Jun 2015 | |
| 1.7 | Updates<br>- Address table, functional description, command truth table<br>- MR17<br>- MR8<br>- IDD4R/W pattern update<br>- ODT input level | Sep 2017 | |
| 1.8 | Updates<br>- JEDEC C version | Aug 2020 | |
| 1.9 | Updated JEDEC D version<br>- 1.4. "Mode Register Definition"<br>- 1.4.1. "MR0 Register Information (MA[5:0] = 00H)"<br>- 1.4.2. "MR1 Register Information (MA[5:0] = 01H)"<br>- 1.4.25. "MR24 Register Information (MA[5:0] = 18H)"<br>- 1.4.27. "MR26 Register Information (MA[7:0] = 1AH)"<br>- 1.4.31. "MR36 Register Information (MA[7:0] = 1BH)"<br>- 2.17.3. "Scaling Parameters"<br>- 2.47. "Truth Tables"<br>- 3. "Absolute Maximum DC Ratings" | Jun 2021 | |

## Features

[LPDDR4x]

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2 = 1.1V (1.06V to 1.17V)
- VDDQ = 0.6V (0.57V to 0.65V)
- Programmable CA ODT and DQ ODT with VSSQ termination
- VOH compensated output driver
- Single data rate command and address entry
- Double data rate architecture for data Bus;
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
- DMI pin support for write data masking and DBIdc functionality
- Programmable RL (Read Latency) and WL (Write Latency)
- Burst length: 16 (default), 32 and On-the-fly
  - On the fly mode is enabled by MRS
- Auto refresh and self refresh supported
- All bank auto refresh and directed per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- Background ZQ Calibration

## Pin Description

| Symbol | Type | Description |
|---|---|---|
| CK_t_A, CK_c_A<br>CK_t_B, CK_c_B | Input | **Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair. |
| CKE_A<br>CKE_B | Input | **Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions.<br>CKE is part of the command code. Each channel (A & B) has its own CKE signal. |
| CS_A<br>CS_B | Input | **Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal. |
| CA[5:0]_A,<br>CA[5:0]_B | Input | **Command/Address Inputs:** Provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals. |
| ODT_CA_A<br>ODT_CA_B | Input | **CA ODT Control:** The ODT_CA pin is ignored by LPDDR4x devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS. |
| DQ[15:0]_A,<br>DQ[15:0]_B | I/O | **Data Input/Output** : Bi-direction data bus. |
| DQS[1:0]_t_A,<br>DQS[1:0]_c_A,<br>DQS[1:0]_t_B,<br>DQS[1:0]_c_B | I/O | **Read Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and is center aligned with Data. Each byte of data has a Data Strobe signal pair.<br>Each channel (A & B) has its own DQS strobes. |
| DMI[1:0]_A, DMI[1:0]_B | I/O | **Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals.This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data Mask - depends on Mode Register Setting. |
| ZQ | Reference | **Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240-Ω ± 1% resistor. |
| VDD1, VDD2, VDDQ | Supply | **Power Supplies:** Isolated on the die for improved noise immunity. |
| VSS | GND | **Ground Reference:** Power supply ground reference. |
| RESET_n | Input | **RESET:** When asserted LOW, the RESET pin resets both channels of the die. |

Notes
1. "_A" and "_B" indicate DRAM channel. "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only

# 1. Functional Description

LPDDR4-SDRAM is a high-speed synchronous DRAM device internally configured with either 1 or 2 channels. Single-channel is comprised of 8-banks with from 1 Gb to 16 Gb per channel density. Dual channel is comprised of 8-banks with from 2 Gb to 32 Gb total die density.

Single-channel SDRAM devices contain the following number of bits:

- 1Gb has 1,073,741,824 bits
- 2Gb has 2,147,483,648 bits
- 3Gb has 3,221,225,472 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits

Dual-channel SDRAM devices contain the following number of bits:

- 2Gb has 2,147,483,648 bits
- 4Gb has 4,294,967,296 bits
- 6Gb has 6,442,450,944 bits
- 8Gb has 8,589,934,592 bits
- 12Gb has 12,884,901,888 bits
- 16Gb has 17,179,869,184 bits
- 24Gb has 25,769,803,776 bits
- 32Gb has 34,359,738,368 bits

LPDDR4 devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details.

These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

## 1.1. LPDDR4 SDRAM Addressing

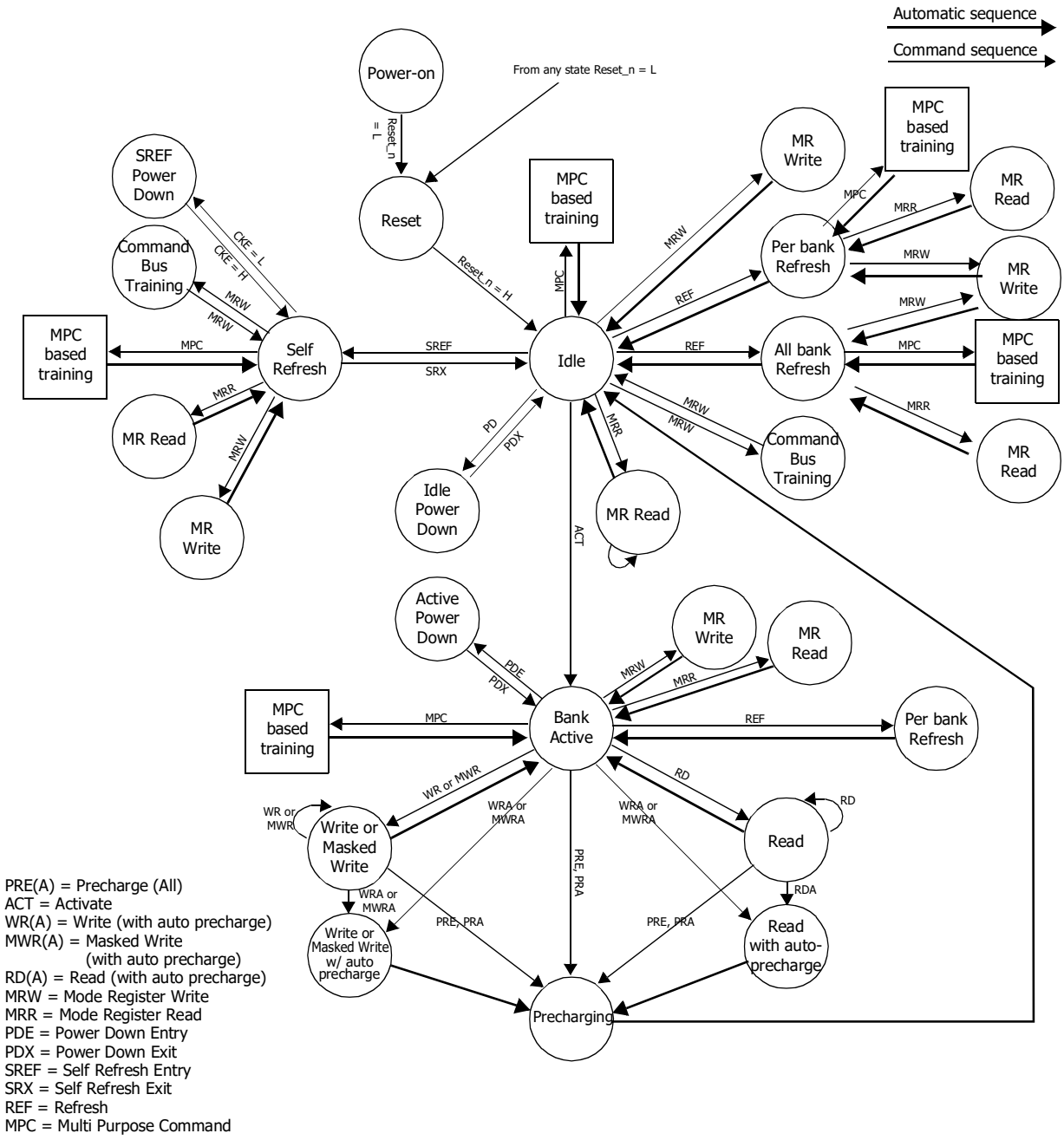
**Table 1 - LPDDR4 SDRAM x16 mode Addressing for Dual Channel SDRAM Die**

| Memory Density (per Die) | | 2Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | 24Gb | 32Gb |
|---|---|---|---|---|---|---|---|---|---|
| Memory Density (per channel) | | 1Gb | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb |
| Configuration | | 8 Mb x 16 DQ x 8 banks x 2 channels | 16 Mb x 16 DQ x 8 banks x 2 channels | 24 Mb x 16 DQ x 8 banks x 2 channels | 32 Mb x 16 DQ x 8 banks x 2 channels | 48Mb x 16DQ x 8 banks x 2 channels | 64 Mb x 16 DQ x 8 banks x 2 channels | 96 Mb x 16DQ x 8 banks x 2 channel | 128Mb x 16DQ x 8 banks x 2 channels |
| Number of Channels per die | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Number of Banks per Channel | | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Array Pre-fetch (bits, per channel) | | 256 | 256 | 256 | 256 | 256 | 256 | 256 | 256 |
| Number of Rows per Channel | | 8,192 | 16,384 | 24,576 | 32,768 | 49,152 | 65,536 | 98,304 | 131,072 |
| Number of Columns (fetch boundaries) | | 64 | 64 | 64 | 64 | 64 | 64 | 64 | 64 |
| Page Size (Bytes) | | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 |
| Channel Density (Bits per channel) | | 1,073,741,824 | 2,147,483,648 | 3,221,225,472 | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 |
| Total Density (Bits per die) | | 2,147,483,648 | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 | 25,769,803,776 | 34,359,738,368 |
| Bank Address | | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 | BA0 - BA2 |
| x16 | Row Addresses | R0 - R12 | R0 - R13 | R0 – R14 (R13=0 when R14=1) | R0 - R14 | R0 – R15 (R14=0 when R15=1) | R0 - R15 | R0 – R16 (R15=0 when R16=1) | R0 - R16 |
| | Column Addresses | C0 - C9 | C0 - C9 | C0 - C9 | C0 - C9 | C0 - C9 | C0 - C9 | C0 - C9 | C0 - C9 |
| Burst Starting Address Boundary | | 64-bit | 64-bit | 64-bit | 64-bit | 64-bit | 64-bit | 64-bit | 64-bit |

Notes
1. The lower two column addresses (C0-C1) are assumed to be "zero" and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density is required to at valid logic levels.
3. For non-binary memory densities, only half of the row address space is valid. When the MSB address bit is "HIGH", then the MSB-1 address bit must be "LOW".
4. The row address input which violates restriction described in note 3 in this table may result in undefined or vendor specific behavior. Consult memory vendor for more information.

## 1.2. Simplified State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the section 2. "Command Definitions and Timing Diagrams".




PRE(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with auto precharge)
MWR(A) = Masked Write (with auto precharge)
RD(A) = Read (with auto precharge)
MRW = Mode Register Write
MRR = Mode Register Read
PDE = Power Down Entry
PDX = Power Down Exit
SREF = Self Refresh Entry
SRX = Self Refresh Exit
REF = Refresh
MPC = Multi Purpose Command

**Figure 1 - Simplified State Diagram**

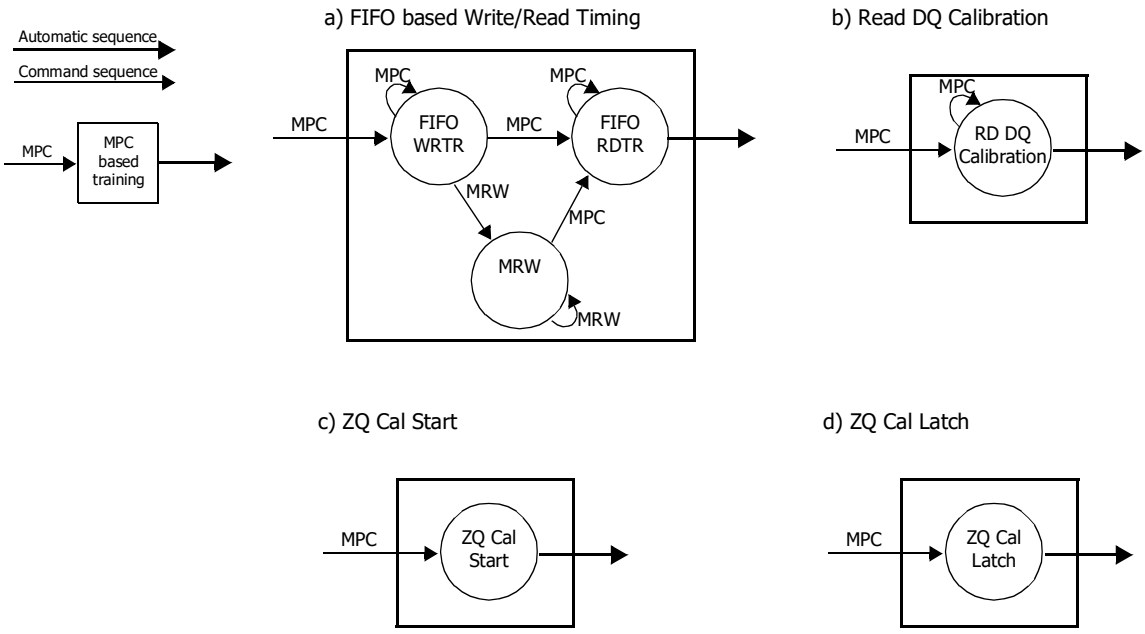



**Figure 2 - Simplified Bus Interface State Diagram**

Notes

1. From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2. In IDLE state, all banks are pre-charged.
3. In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4. In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5. This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7. The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

## 1.3. Power-up and Initialization

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as following table.

**Table 2 - MRS defaults settings**

| Item | MRS | Default setting | Description |
|---|---|---|---|
| FSP-OP/WR | MR13 OP[7:6] | 00B | FS-OP/WR[0] are enabled |
| WLS | MR2 OP[6] | 0B | Write Latency Set 0 is selected |
| WL | MR2 OP[5:3] | 000B | WL = 4 |
| RL | MR2 OP[2:0] | 000B | RL = 6, nRTP = 8 |
| nWR | MR1 OP[6:4] | 000B | nWR = 6 |
| DBI-WR/RD | MR3 OP[7:6] | 00B | Write & Read DBI are disabled |
| CA ODT | MR11 OP[6:4] | 000B | CA ODT is disabled |
| DQ ODT | MR11 OP[2:0] | 000B | DQ ODT is disabled |
| VREF(CA) Setting | MR12 OP[6] | 1B | VREF(CA) Range[1] enabled |
| VREF(CA) value | MR12 OP[5:0] | 011101B | Range1: 50.3% of VDDQ |
| VREF(DQ) Setting | MR14 OP[6] | 1B | VREF(DQ) Range[1] enabled |
| VREF(DQ) Value | MR14 OP[5:0] | 011101B | Range1: 50.3% of VDDQ |

### 1.3.1. Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table "Voltage Ramp Conditions". VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

**Table 3 - Voltage Ramp Conditions**

| After | Applicable Conditions |
|---|---|
| Ta is reached | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

Notes
1. Ta is the point when any power supply first reaches 300mV.
2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. The voltage difference between any of VSS and VSSQ pins must not excess 100mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before Reset_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

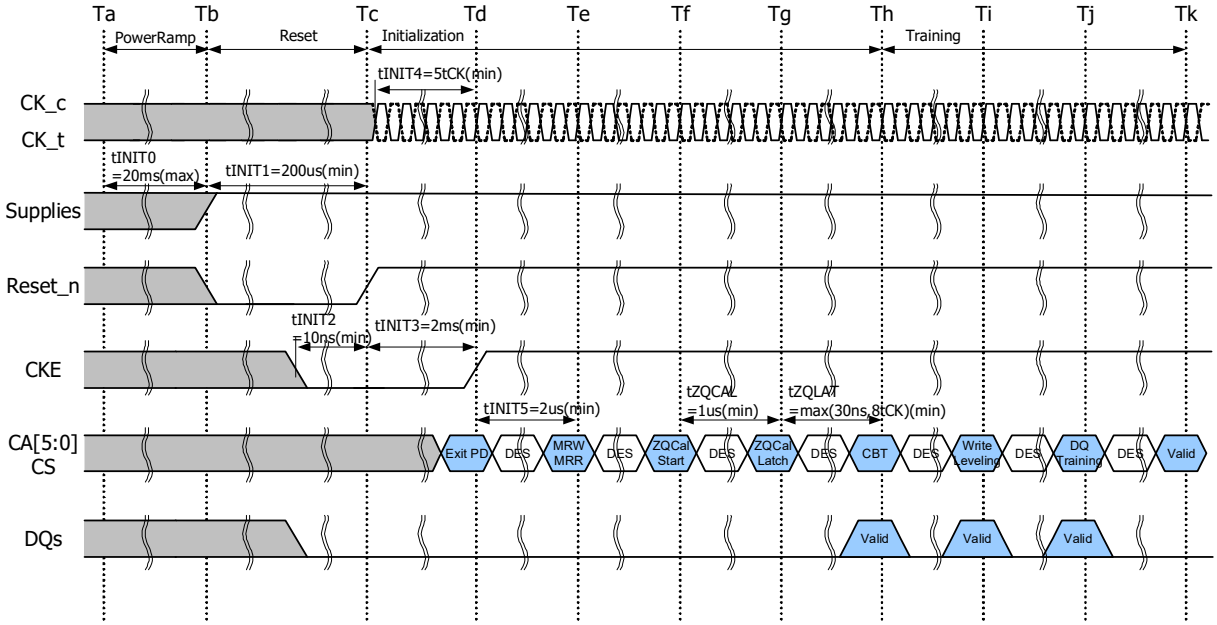



**Figure 3 - Power Ramp and Initialization Sequence**

Notes

1. Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in the above figure, is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed

operations, and VREF(CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high(Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(DQ)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

**Table 4 - Initialization Timing Parameters**

| Parameter | Value | | Unit | Comment |
|---|---|---|---|---|
| | Min | Max | | |
| tINIT0 | | 20 | ms | Maximum Voltage Ramp Time |
| tINIT1 | 200 | | us | Minimum RESET_n LOW time after completion of voltage ramp |
| tINIT2 | 10 | | ns | Minimum CKE LOW time before RESET_n goes HIGH |
| tINIT3 | 2 | | ms | Minimum CKE LOW time after RESET_n goes HIGH |
| tINIT4 | 5 | | tCK | Minimum stable clock before first CKE HIGH |
| tINIT5 | 2 | | us | Minimum idle time before first MRW/MRR command |
| tZQCAL | 1 | | us | ZQ Calibration time |
| tZQLAT | Max(30ns.8tCK) | | ns | ZQCAL latch quite time |
| tCKb | Note 1, 2 | Note 1, 2 | ns | Clock cycle time during boot |

Notes
1. Min tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

### 1.3.2. Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.

2. Repeat steps 4 to 10 in 1.3.1. "Voltage Ramp and Device Initialization".

**Table 5 - Reset Timing Parameter**

| Parameter | Value | | Unit | Comment |
|---|---|---|---|---|
| | Min | Max | | |
| tPW_RESET | 100 | - | ns | Minimum RESET_n low time for Reset Initialization with stable power |

### 1.3.3. Power-off Sequence

The following procedure is required to power off the device.
While powering off, CKE must be held LOW (≤0.2 X VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300mV. After TZ, the device is powered off.

**Table 6 - Power Supply Conditions for Power-off**

| Between | Applicable Conditions |
|---|---|
| TX and TZ | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

Notes
1. The voltage difference between any of VSS, VSSQ pins must not exceed 100mV

### 1.3.4. Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5V/µs between Tx and Tz.
An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

**Table 7 - Timing Parameters for Power-off**

| Symbol | Value | | Unit | Comment |
|---|---|---|---|---|
| | Min | Max | | |
| tPOFF | - | 2 | s | Maximum Power-off ramp time |

## 1.4. Mode Register Definition

Table below shows the mode registers for LPDDR4 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

**Table 8 - Mode Register Assignment**

| MR# | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| 0 | Reserved | RFU | RFU | RZQI | | RFU | RFU | Refresh Mode |
| 1 | RPST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | |
| 2 | WR Lev | WLS | WL | | | RL | | |
| 3 | DBI-WR | DBI-RD | PDDS | | | PPRP | WR-PST | PU-CAL |
| 4 | TUF | Thermal Offset | | PPRE | SR Abort | Refresh Rate | | |
| 5 | LPDDR4 Manufacturer ID | | | | | | | |
| 6 | Revision ID-1 | | | | | | | |
| 7 | Revision ID-2 | | | | | | | |
| 8 | IO Width | | Density | | | | Type | |
| 9 | Vendor Specific Test Mode | | | | | | | |
| 10 | RFU | | | | | | | ZQ Reset |
| 11 | RFU | CA ODT | | | RFU | DQ ODT | | |
| 12 | CBT Mode | VR-CA | VREF(CA) | | | | | |
| 13 | FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPT | CBT |
| 14 | RFU | VR(dq) | VREF(DQ) | | | | | |
| 15 | Lower Byte Invert for DQ Calibration | | | | | | | |
| 16 | PASR Bank Mask | | | | | | | |
| 17 | PASR Segment Mask | | | | | | | |
| 18 | DQS Oscillator Count - LSB | | | | | | | |
| 19 | DQS Oscillator Count - MSB | | | | | | | |
| 20 | Upper Byte Invert for DQ Calibration | | | | | | | |
| 21 | RFU | | | | | | | |
| 22 | RFU | | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT | | |
| 23 | DQS Oscillator Interval Timer Run Time Setting | | | | | | | |
| 24 | TRR Mode | TRR Mode BAn | | | Unlimited MAC | MAC value | | |
| 25 | Post Package Repair Resources | | | | | | | |
| 26 | Reserved for Future Use | | | | | | | |
| 27 | Reserved for Future Use | | | | | | | |
| 28 | Reserved for Future Use | | | | | | | |
| 29 | Reserved for Future Use | | | | | | | |

| MR# | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|---|---|---|---|---|---|---|---|
| 30 | Reserved for testing - SDRAM will ignore | | | | | | | |
| 31 | Reserved for Future Use | | | | | | | |
| 32 | DQ Calibration Pattern "A" (default = 5AH) | | | | | | | |
| 33 | Reserved for Future Use | | | | | | | |
| 34 | Reserved for Future Use | | | | | | | |
| 35 | Reserved for Future Use | | | | | | | |
| 36 | Reserved for Future Use | | | | | | | |
| 37 | Reserved for Future Use | | | | | | | |
| 38 | Reserved for Future Use | | | | | | | |
| 39 | Reserved for testing - SDRAM will ignore | | | | | | | |
| 40 | DQ Calibration Pattern "B" (default = 3CH) | | | | | | | |

### 1.4.1. MR0 Register Information (MA[5:0] = 00H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| CATR | RFU | Single-Ended Mode | RZQI | | RFU | Latency Mode | Refresh Mode |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Refresh Mode | Read-only | OP[0] | 0B: Both legacy & modified refresh mode supported<br>1B: Only modified refresh mode supported | |
| Latency Mode | | OP[1] | 0B: Device supports normal latency<br>1B: Device supports byte mode latency | 5,6 |
| RZQI<br>(Built-in Self-Test for RZQ) | | OP[4:3] | 00B: RZQ Self-Test Not Supported<br>01B: ZQ pin may connect to VSSQ or float<br>10B: ZQ-pin may short to VDDQ<br>11B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ) | 1,2,3,4 |
| Single-Ended Mode | | OP[5] | 0B: No support for Single-Ended Mode<br>1B: Support for Single-Ended Mode | 7 |
| CATR<br>(CA Terminating Rank) | | OP[7] | 0B: CA for this rank is not terminated<br>1B: Vendor Specific | 5 |

Notes
1. RZQI MR value, if supported, will be valid after the following sequence:
   a. Completion of MPC ZQCAL Start command to either channel.
   b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied. RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ω ± 1%).
5. CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.
7. Support for Single Ended Mode is optional. If supported, Single Ended Write DQS, Read DQS and CK can be enabled in MR51.

### 1.4.2. MR1 Register Information (MA[5:0] = 01H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RPST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| BL<br>(Burst Length) | Write-only | OP[1:0] | 00B: BL=16 Sequential (default)<br>01B: BL=32 Sequential<br>10B: BL=16 or 32 Sequential (on-the-fly)<br>All Others: Reserved | 1,7 |
| WR-PRE<br>(WR Pre-amble Length) | | OP[2] | 0B: Reserved<br>1B: WR Pre-amble = 2tCK (default) | 5,6 |
| RD-PRE<br>(RD Pre-amble Type) | | OP[3] | 0B: RD Pre-amble = Static (default)<br>1B: RD Pre-amble = Toggle | 3,5,6 |
| nWR<br>(Write-Recovery for Auto Precharge commands) | | OP[6:4] | For x16 mode MR26 OP[1:0]= 00B<br>000B: nWR = 6 (default)<br>001B: nWR = 10<br>010B: nWR = 16<br>011B: nWR = 20<br>100B: nWR = 24<br>101B: nWR = 30<br>110B: nWR = 34<br>111B: nWR = 40<br><br>For x16 mode MR26 OP[1:0]= 01B<br>000B: nWR = 11 (default)<br>001B: nWR = 19<br>010B: nWR = 29<br>011B: nWR = 38<br>100B: nWR = 46<br>101B: nWR = 56<br>110B: nWR = 64<br>111B: nWR = 75 | 2,5,6 |
| RPST<br>(RD Post-amble Length) | | OP[7] | 0B: RD Post-amble = 0.5*tCK (default)<br>1B: RD Post-amble = 1.5*tCK | 4,5,6 |

Notes

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the "BL" bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled.
3. For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be read from with an MRR command to this MR address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
7. Supporting the two physical registers for Burst Length: MR1 OP[1:0] as optional feature. Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.

### 1.4.2.1. Burst Sequence

**Table 9 - Burst Sequence for Read**

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | Co | Burst Cycle Number and Burst Address Sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16 | SEQ | V | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | | | | | | | | | | | | | | | | |
| | | V | 0 | 1 | 0 | 0 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | | | | | | | | | | | | | | | | | | |
| | | V | 1 | 0 | 0 | 0 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | | | | | | | | | | | |
| | | V | 1 | 1 | 0 | 0 | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | | | | | | | | | | | | | | | | | | |
| 32 | SEQ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |
| | | 0 | 0 | 1 | 0 | 0 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 |
| | | 0 | 1 | 0 | 0 | 0 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| | | 0 | 1 | 1 | 0 | 0 | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B |
| | | 1 | 0 | 0 | 0 | 0 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| | | 1 | 0 | 1 | 0 | 0 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 |
| | | 1 | 1 | 0 | 0 | 0 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | | 1 | 1 | 1 | 0 | 0 | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B |

Notes
1. C0-C1 are assumed to be '0' , and are not transmitted on the command bus
2. The starting address is on 64-bit (4n) boundaries.

**Table 10 - Burst Sequence for Write**

| Burst Length | Burst Type | C4 | C3 | C2 | C1 | Co | Burst Cycle Number and Burst Address Sequence | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 16 | SEQ | V | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | | | | | | | | | | | | | | | | |
| 32 | SEQ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |

Notes
1. C0-C1 are assumed to be '0' , and are not transmitted on the command bus
2. The starting address is on 256-bit (16n) boundaries for Burst length 16.
3. The starting address is on 512-bit (32n) boundaries for Burst length 32.
4. C2-C3 shall be set to '0' for all Write operations.
5. C4=1 for Write is supported in SK hynix device.

### 1.4.3. MR2 Register Information (MA[5:0] = 02H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| WR Lev | WLS | WL | | | RL | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| RL<br>(Read latency) | Write only | OP[2:0] | For x16 mode<br>RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0B)<br>000B: RL=6, nRTP = 8 (Default)<br>001B: RL=10, nRTP = 8<br>010B: RL=14, nRTP = 8<br>011B: RL=20, nRTP = 8<br>100B: RL=24, nRTP = 10<br>101B: RL=28, nRTP = 12<br>110B: RL=32, nRTP = 14<br>111B: RL=36, nRTP = 16<br>RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1B)<br>000B: RL=6, nRTP = 8<br>001B: RL=12, nRTP = 8<br>010B: RL=16, nRTP = 8<br>011B: RL=22, nRTP = 8<br>100B: RL=28, nRTP = 10<br>101B: RL=32, nRTP = 12<br>110B: RL=36, nRTP = 14<br>111B: RL=40, nRTP = 16 | 1,3,4 |
| WL<br>(Write latency) | | OP[5:3] | For x16 mode<br>WL Set "A" (MR2 OP[6]=0B)<br>000B: WL=4 (Default)<br>001B: WL=6<br>010B: WL=8<br>011B: WL=10<br>100B: WL=12<br>101B: WL=14<br>110B: WL=16<br>111B: WL=18<br>WL Set "B" (MR2 OP[6]=1B)<br>000B: WL=4<br>001B: WL=8<br>010B: WL=12<br>011B: WL=18<br>100B: WL=22<br>101B: WL=26<br>110B: WL=30<br>111B: WL=34 | 1,3,4 |
| WLS<br>(Write Latency Set) | | OP[6] | 0B: WL Set "A" (default)<br>1B: WL Set "B" | 1,3,4 |
| WR LEV<br>(Write Leveling) | | OP[7] | 0B: Disabled (default)<br>1B: Enabled | 2 |

Notes
1. See Section 4.12 Read and Write Latencies for detail.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

### 1.4.4. MR3 Register Information (MA[5:0] = 03H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DBI-WR | DBI-RD | PDDS | | | PPRP | WR-PST | PU-CAL |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| PU-CAL<br>(Pull-up Calibration Point) | Write-only | OP[0] | 0B: VDDQ*0.6<br>1B: VDDQ*0.5 (default) | 1,4 |
| WR-PST<br>(Write Post-amble length) | | OP[1] | 0B: WR Post-amble = 0.5*tCK (default)<br>1B: WR Post-amble = 1.5*tCK (Vendor Specific) | 2,3,5 |
| Post Package Repair Protection | | OP[2] | 0B: PPR Protection Disabled (Default)<br>1B: PPR Protection Enabled | 6 |
| PDDS<br>(Pull-down Drive Strength) | | OP[5:3] | 000B: RFU<br>001B: RZQ/1<br>010B: RZQ/2<br>011B: RZQ/3<br>100B: RZQ/4<br>101B: RZQ/5<br>110B: RZQ/6 (default)<br>111B: Reserved | 1,2,3 |
| DBI-RD<br>(DBI-Read Enable) | | OP[6] | 0B: Disabled (default)<br>1B: Enabled | 2,3 |
| DBI-WR<br>(DBI-WR Enable) | | OP[7] | 0B: Disabled (default)<br>1B: Enabled | 2,3 |

Notes
1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. Refer to the supplier data sheet for vendor specific function. 1.5*tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

### 1.4.5. MR4 Register Information (MA[5:0] = 04H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| TUF | Thermal Offset | | PPRE | SR Abort | Refresh Rate | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Refresh Rate | Read | OP[2:0] | 000B: SDRAM Low temperature operating limit exceeded<br>001B: 4x refresh<br>010B: 2x refresh<br>011B: 1x refresh (default)<br>100B: 0.5x refresh<br>101B: 0.25x refresh, no de-rating<br>110B: 0.25x refresh, with de-rating<br>111B: SDRAM High temperature operating limit exceeded | 1,2,3,4, 7,8,9 |
| Self Refresh Abort | Write | OP[3] | 0B: Disabled (default)<br>1B: Enabled | 9,11 |
| PPRE<br>(Post-package repair entry/exit) | Write | OP[4] | 0B: Exit PPR mode (default)<br>1B: Enter PPR mode | 5,9 |
| Thermal Offset | Write | OP[6:5] | 00B: No offset, 0-5°C gradient (default)<br>01B: 5°C offset, 5-10°C gradient<br>10B: 10°C offset, 10-15°C gradient<br>11B: Reserved | 10 |
| TUF<br>(Temperature Update Flag) | Read | OP[7] | 0B: No change in OP[2:0] since last MR4 read (default)<br>1B: Change in OP[2:0] since last MR4 read | 6,7,8 |

Notes
1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. If OP[2]=0B, the device temperature is less or equal to 85'C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1, the device temperature is greater than 85'C.
2. At higher temperatures (>85'C), AC timing de-rating may be required. If de-rating is required the LPDDR4-SDRAM will set OP[2:0]=110B. See de-rating timing requirements in the AC Timing section.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000B or 111B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7]=0 at power-up. OP[2:0] bits are undefined at power-up.
8. See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
9. OP[6:3] bits are that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register
10. Refer to the supplier data sheet for vender specific function.
11. Self Refresh abort feature is available for higher density devices starting with 12Gb device.

### 1.4.6. MR5 Register Information (MA[5:0] = 05H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| LPDDR4 Manufacturer ID | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| LPDDR4 Manufacturer ID | Read-only | OP[7:0] | 00000110B : SK hynix | |

### 1.4.7. MR6 Register Information (MA[5:0] = 06H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Revision ID-1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| LPDDR4 Revision ID-1 | Read-only | OP[7:0] | 00000000B: A-version<br>00000001B: B-version | 1 |

Notes
1. Please contact SK hynix office for MR6 code for this device.

### 1.4.8. MR7 Register Information (MA[5:0] = 07H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Revision ID-2 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| LPDDR4 Revision ID-1 | Read-only | OP[7:0] | 00000000B: A-version<br>00000001B: B-version | 1 |

Notes
1. Please contact SK hynix office for MR7 code for this device.

### 1.4.9. MR8 Register Information (MA[5:0] = 08H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| IO Width | | Density | | | | Type | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Type | Read-only | OP[1:0] | 00B: S16 SDRAM (16n pre-fetch)<br>All Others: Reserved | |
| Density | | OP[5:2] | 0000B: 4Gb dual channel die / 2Gb single channel die<br>0001B: 6Gb dual channel die / 3Gb single channel die<br>0010B: 8Gb dual channel die / 4Gb single channel die<br>0011B: 12Gb dual channel die / 6Gb single channel die<br>0100B: 16Gb dual channel die / 8Gb single channel die<br>0101B: 24Gb dual channel die / 12Gb single channel die<br>0110B: 32Gb dual channel die / 16Gb single channel die<br>1100B: 2Gb dual channel die / 1Gb single channel die<br>All Others: Reserved | |
| IO Width | | OP[7:6] | 00B: x16 (per channel)<br>All Others: Reserved | |

### 1.4.10. MR9 Register Information (MA[5:0] = 09H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Vendor Specific Test Register | | | | | | | |

Notes
1. Only 00H should be written to this register.

### 1.4.11. MR10 Register Information (MA[5:0] = 0AH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | | | | | | ZQ Reset |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| ZQ Reset | Write-only | OP[0] | OB: Normal Operation (Default)<br>1B: ZQ Reset | 1,2 |

Notes
1. See the AC Timing tables for calibration latency and timing
2. If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

### 1.4.12. MR11 Register Information (MA[5:0] = 0BH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | CA ODT | | | RFU | DQ ODT | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| DQ ODT<br>(DQ Bus Receiver On-Die-Termination) | Write-only | OP[2:0] | 000B: Disable (Default)<br>001B: RZQ/1<br>010B: RZQ/2<br>011B: RZQ/3<br>100B: RZQ/4<br>101B: RZQ/5<br>110B: RZQ/6<br>111B: RFU | 1,2,3 |
| CA ODT<br>(CA Bus Receiver On-Die-Termination) | | OP[6:4] | 0000B: Disable (Default)<br>0001B: RZQ/1<br>0010B: RZQ/2<br>0011B: RZQ/3<br>0100B: RZQ/4<br>0101B: RZQ/5<br>0110B: RZQ/6<br>0111B: RFU | 1,2,3 |

Notes
1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

### 1.4.13. MR12 Register Information (MA[5:0] = 0CH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| CBT Mode | VR-CA | VREF(CA) | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| VREF(CA)<br>(VREF(CA) Setting) | Read/Write | OP[5:0] | 000000B:<br>-- Thru –<br>110010B: See table below<br>All Others: Reserved | 1,2,3,5,6 |
| VREF(CA) Range | | OP[6] | 0B: VREF(CA) Range[0] enabled<br>1B: VREF(CA) Range[1] enabled (default) | 1,2,4,5,6 |
| CBT Mode | Write | OP[7] | 0B: Mode1 (Default)<br>1B: Mode2 | 7 |

Notes

1. This register controls the VREF(CA) levels. Refer to Table 3 for actual voltage of VREF(CA).
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(CA) level for FSP[0] when MR13 OP[6] = 0B, or sets FSP[1] when MR13 OP[6] = 1B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(CA) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
7. This field can be activated in only Byte Mode: x8. Device.

**Table 11 - VREF Settings for Range[0] and Range[1]**

| Function | Operand | Range[0] Values (% of VDDQ) | | Range[1] Values (% of VDDQ) | | Notes |
|---|---|---|---|---|---|---|
| VREF Settings for MR12 | OP[5:0] | 000000B: 15.0%<br>000001B: 15.6%<br>000010B: 16.2%<br>000011B: 16.8%<br>000100B: 17.4%<br>000101B: 18.0%<br>000110B: 18.6%<br>000111B: 19.2%<br>001000B: 19.8%<br>001001B: 20.4%<br>001010B: 21.0%<br>001011B: 21.6%<br>001100B: 22.2%<br>001101B: 22.8%<br>001110B: 23.4%<br>001111B: 24.0%<br>010000B: 24.6%<br>010001B: 25.1%<br>010010B: 25.7%<br>010011B: 26.3%<br>010100B: 26.9%<br>010101B: 27.5%<br>010110B: 28.1%<br>010111B: 28.7%<br>011000B: 29.3%<br>011001B: 29.9% | 011010B: 30.5%<br>011011B: 31.1%<br>011100B: 31.7%<br>011101B: 32.3%<br>011110B: 32.9%<br>011111B: 33.5%<br>100000B: 34.1%<br>100001B: 34.7%<br>100010B: 35.3%<br>100011B: 35.9%<br>100100B: 36.5%<br>100101B: 37.1%<br>100110B: 37.7%<br>100111B: 38.3%<br>101000B: 38.9%<br>101001B: 39.5%<br>101010B: 40.1%<br>101011B: 40.7%<br>101100B: 41.3%<br>101101B: 41.9%<br>101110B: 42.5%<br>101111B: 43.1%<br>110000B: 43.7%<br>110001B: 44.3%<br>110010B: 44.9%<br>All Others: Reserved | 000000B: 32.9%<br>000001B: 33.5%<br>000010B: 34.1%<br>000011B: 34.7%<br>000100B: 35.3%<br>000101B: 35.9%<br>000110B: 36.5%<br>000111B: 37.1%<br>001000B: 37.7%<br>001001B: 38.3%<br>001010B: 38.9%<br>001011B: 39.5%<br>001100B: 40.1%<br>001101B: 40.7%<br>001110B: 41.3%<br>001111B: 41.9%<br>010000B: 42.5%<br>010001B: 43.1%<br>010010B: 43.7%<br>010011B: 44.3%<br>010100B: 44.9%<br>010101B: 45.5%<br>010110B: 46.1%<br>010111B: 46.7%<br>011000B: 47.3%<br>011001B: 47.9% | 011010B: 48.5%<br>011011B: 49.1%<br>011100B: 49.7%<br>011101B: 50.3%<br>011110B: 50.9%<br>011111B: 51.5%<br>100000B: 52.1%<br>100001B: 52.7%<br>100010B: 53.3%<br>100011B: 53.9%<br>100100B: 54.5%<br>100101B: 55.1%<br>100110B: 55.7%<br>100111B: 56.3%<br>101000B: 56.9%<br>101001B: 57.5%<br>101010B: 58.1%<br>101011B: 58.7%<br>101100B: 59.3%<br>101101B: 59.9%<br>101110B: 60.5%<br>101111B: 61.1%<br>110000B: 61.7%<br>110001B: 62.3%<br>110010B: 62.9%<br>All Others: Reserved | 1,2,3 |

Notes

1. These values may be used for MR12 OP[5:0] to set the VREF(CA) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

### 1.4.14. MR13 Register Information (MA[5:0] = 0DH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPRE-TR | CBT |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| CBT<br>(Command Bus Training) | Write-Only | OP[0] | 0B: Normal Operation (default)<br>1B: Command Bus Training mode enabled | 1 |
| RPT<br>(Read Preamble Training) | | OP[1] | 0B: Normal Operation (default)<br>1B: Read Preamble Training mode enabled | |
| VRO<br>(Vref Output) | | OP[2] | 0B: Normal Operation (default)<br>1B: Output the VREF(CA) value on DQ[0] and the VREF(DQ) value on DQ[1] | 2 |
| VRCG<br>(VREF Current Generator) | | OP[3] | 0B: Normal Operation (default)<br>1B: VREF Fast Response (high current) mode | 3 |
| RRO<br>(Refresh Rate Option) | | OP[4] | 0B: Disable codes 001 and 010 in MR4 OP[2:0]<br>1B: Enable MR4 OP[2:0] | 4,5 |
| DMD<br>(Data Mask Disable) | | OP[5] | 0B: Data Mask Operation Enabled (default)<br>1B: Data Mask Operation Disabled | 6 |
| FSP-WR<br>(Frequency Set Point Write Enable) | | OP[6] | 0B: Frequency-Set-Point[0] (default)<br>1B: Frequency-Set-Point[1] | 7 |
| FSP-OP<br>(Frequency Set Point Operation Mode) | | OP[7] | 0B: Frequency-Set-Point[0] (default)<br>1B: Frequency-Set-Point[1] | 8 |

Notes

1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the Command bus training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the VREF(CA) training section for more information.
2. When set, the LPDDR4-SDRAM will output the VREF(CA) voltage on DQ[0] and the VREF(DQ) voltage on DQ[1]. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), Masked Write Command is not allowed and it is illegal. See the Data Mask section for more information.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions: VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions: VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range, CA ODT Enable, CA ODT value, DQ ODT Enable, DQ ODT value, DQ Calibration Point, WL, RL, nWR, Read and Write Preamble, Read postamble, and DBI Enables.

### 1.4.15. MR14 Register Information (MA[5:0] = 0EH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | VR(DQ) | VREF(DQ) | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| VREF(DQ)<br>(VREF(DQ) Setting | Read / Write | OP[5:0] | 000000B:<br>-- Thru –<br>110010B: See table below<br>All Others: Reserved | 1,2,3,5,<br>6 |
| VREF(DQ) Range | | OP[6] | 0B: VREF(DQ) Range[0] enabled<br>1B: VREF(DQ) Range[1] enabled (default) | 1,2,4,5,<br>6 |

Notes

1. This register controls the VREF(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(dq)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(DQ) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal VREF(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

**Table 12 - VREF Settings for Range[0] and Range[1]**

| Function | Operand | Range[0] Values (% of VDDQ) | | Range[1] Values (% of VDDQ) | | Notes |
|---|---|---|---|---|---|---|
| VREF Settings for MR14 | OP[5:0] | 000000B: 15.0%<br>000001B: 15.6%<br>000010B: 16.2%<br>000011B: 16.8%<br>000100B: 17.4%<br>000101B: 18.0%<br>000110B: 18.6%<br>000111B: 19.2%<br>001000B: 19.8%<br>001001B: 20.4%<br>001010B: 21.0%<br>001011B: 21.6%<br>001100B: 22.2%<br>001101B: 22.8%<br>001110B: 23.4%<br>001111B: 24.0%<br>010000B: 24.6%<br>010001B: 25.1%<br>010010B: 25.7%<br>010011B: 26.3%<br>010100B: 26.9%<br>010101B: 27.5%<br>010110B: 28.1%<br>010111B: 28.7%<br>011000B: 29.3%<br>011001B: 29.9% | 011010B: 30.5%<br>011011B: 31.1%<br>011100B: 31.7%<br>011101B: 32.3%<br>011110B: 32.9%<br>011111B: 33.5%<br>100000B: 34.1%<br>100001B: 34.7%<br>100010B: 35.3%<br>100011B: 35.9%<br>100100B: 36.5%<br>100101B: 37.1%<br>100110B: 37.7%<br>100111B: 38.3%<br>101000B: 38.9%<br>101001B: 39.5%<br>101010B: 40.1%<br>101011B: 40.7%<br>101100B: 41.3%<br>101101B: 41.9%<br>101110B: 42.5%<br>101111B: 43.1%<br>110000B: 43.7%<br>110001B: 44.3%<br>110010B: 44.9%<br>All Others: Reserved | 000000B: 32.9%<br>000001B: 33.5%<br>000010B: 34.1%<br>000011B: 34.7%<br>000100B: 35.3%<br>000101B: 35.9%<br>000110B: 36.5%<br>000111B: 37.1%<br>001000B: 37.7%<br>001001B: 38.3%<br>001010B: 38.9%<br>001011B: 39.5%<br>001100B: 40.1%<br>001101B: 40.7%<br>001110B: 41.3%<br>001111B: 41.9%<br>010000B: 42.5%<br>010001B: 43.1%<br>010010B: 43.7%<br>010011B: 44.3%<br>010100B: 44.9%<br>010101B: 45.5%<br>010110B: 46.1%<br>010111B: 46.7%<br>011000B: 47.3%<br>011001B: 47.9% | 011010B: 48.5%<br>011011B: 49.1%<br>011100B: 49.7%<br>011101B: 50.3%<br>011110B: 50.9%<br>011111B: 51.5%<br>100000B: 52.1%<br>100001B: 52.7%<br>100010B: 53.3%<br>100011B: 53.9%<br>100100B: 54.5%<br>100101B: 55.1%<br>100110B: 55.7%<br>100111B: 56.3%<br>101000B: 56.9%<br>101001B: 57.5%<br>101010B: 58.1%<br>101011B: 58.7%<br>101100B: 59.3%<br>101101B: 59.9%<br>101110B: 60.5%<br>101111B: 61.1%<br>110000B: 61.7%<br>110001B: 62.3%<br>110010B: 62.9%<br>All Others: Reserved | 1,2,3 |

Notes

1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency settings which may use different terminations values.

### 1.4.16. MR15 Register Information (MA[5:0] = 0FH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Lower Byte Invert Register for DQ Calibration | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Lower Byte Invert for DQ Calibration | Write-Only | OP[7:0] | The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane:<br><br>0B: Do not invert<br>1B: Invert the DQ Calibration patterns in MR32 and MR40<br><br>Default value for OP[7:0]=55H | 1,2,3 |

Notes

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table 13 - MR15 Invert Register Pin Mapping**

| Pin | DQ0 | DQ1 | DQ2 | DQ3 | DMI0 | DQ4 | DQ5 | DQ6 | DQ7 |
|---|---|---|---|---|---|---|---|---|---|
| MR15 | OP0 | OP1 | OP2 | OP3 | No-invert | OP4 | OP5 | OP6 | OP7 |

### 1.4.17. MR16 Register Information (MA[5:0] = 10H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| PASR Bank Mask | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Bank[7:0] Mask | Write-only | OP[7:0] | 0B: Bank Refresh enabled (default) : Unmasked<br>1B: Bank Refresh disabled : Masked | 1 |

| OP[n] | Bank Mask | 8-Bank SDRAM |
|---|---|---|
| 0 | xxxxxxx1 | Bank 0 |
| 1 | xxxxxx1x | Bank 1 |
| 2 | xxxxx1xx | Bank 2 |
| 3 | xxxx1xxx | Bank 3 |
| 4 | xxx1xxxx | Bank 4 |
| 5 | xx1xxxxx | Bank 5 |
| 6 | x1xxxxxx | Bank 6 |
| 7 | 1xxxxxxx | Bank 7 |

Notes
1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank masking is on a per channel basis. The two channels on the die may have different bank masking.

### 1.4.18. MR17 Register Information (MA[5:0] = 11H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| PASR Segment Mask | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| PASR Segment Mask | Write-only | OP[7:0] | 0B: Segment Refresh enabled (default)<br>1B: Segment Refresh disabled | 1 |

**Table 14 - MR17 Register Segment Mask for x16 mode**

| Segment | OP[n] | Segment Mask | 2Gb per channel | 3Gb per channel | 4Gb per channel | 6Gb per channel | 8Gb per channel | 12Gb per channel | 16Gb per channel |
|---|---|---|---|---|---|---|---|---|---|
| | | | R13:R11 | R14:R12 | R14:R12 | R15:R13 | R15:R13 | R16:R14 | R16:R14 |
| 0 | 0 | xxxxxxx1 | 000B | | | | | | |
| 1 | 1 | xxxxxx1x | 001B | | | | | | |
| 2 | 2 | xxxxx1xx | 010B | | | | | | |
| 3 | 3 | xxxx1xxx | 011B | | | | | | |
| 4 | 4 | xxx1xxxx | 100B | | | | | | |
| 5 | 5 | xx1xxxxx | 101B | | | | | | |
| 6 | 6 | x1xxxxxx | $110_B$ | Not Allowed | $110_B$ | Not Allowed | $110_B$ | Not Allowed | $110_B$ |
| 7 | 7 | 1xxxxxxx | $111_B$ | | $111_B$ | | $111_B$ | | $111_B$ |

Notes
1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
3. For 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00B).

### 1.4.19. MR18 Register Information (MA[5:0] = 12H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DQS Oscillator Count - LSB | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only | OP[7:0] | 0:255 LSB DRAM DQS Oscillator Count | 1,2,3 |

Notes
1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 1.4.20. MR19 Register Information (MA[5:0] = 13H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DQS Oscillator Count - MSB | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| DQS Oscillator<br>(WR Training DQS Oscillator) | Read-only | OP[7:0] | 0:255 MSB DRAM DQS Oscillator Count | 1,2,3 |

Notes
1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

### 1.4.21. MR20 Register Information (MA[5:0] = 14H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Upper Byte Invert Register for DQ Calibration | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Upper Byte Invert for DQ Calibration | Write-Only | OP[7:0] | The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane:<br><br>0B: Do not invert<br>1B: Invert the DQ Calibration patterns in MR32 and MR40<br><br>Default value for OP[7:0]=55H | 1,2 |

Notes

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

**Table 15 - MR20 Invert Register Pin Mapping**

| Pin | DQ8 | DQ9 | DQ10 | DQ11 | DMI1 | DQ12 | DQ13 | DQ14 | DQ15 |
|---|---|---|---|---|---|---|---|---|---|
| MR20 | OP0 | OP1 | OP2 | OP3 | No-invert | OP4 | OP5 | OP6 | OP7 |

### 1.4.22. MR21 Register Information (MA[5:0] = 15H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | Low Speed CA buffer | RFU | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Low Speed CA Buffer | Write-only | OP[1] | 0B : Normal CA Buffer (Default)<br>1B : Low Speed CA Buffer | 1,2,3,4, 5,6,7 |

Notes

1. Support for the Low Speed CA Buffer feature enabled by MR21 OP[5] is optional. Refer to manufacturer data sheet for availability.
2. Low speed CA buffer. Low Speed CA Buffer feature can enable lower power for some manufacturers' designs. The maximum clock speed for this mode is vendor-specific, but is not above 800 MHz. Refer to manufacturer data sheet for details.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
5. After completing all other MRW commands to set the values besides MR21 OP[5] setting, MR21 OP[5] can be enabled to "high". Low Power CA Buffer cannot be enabled prior to full device initialization (completion of Step 9 in power up sequence).
6. Low speed CA buffer is allowed to be enabled only when CA ODT is disabled.
7. Devices not supporting Low Speed CA Buffer will ignore MR21 OP[5] setting.

### 1.4.23. MR22 Register Information (MA[5:0] = 16H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| SoC ODT<br>(Controller ODT Value for VOH calibration | Write | OP[2:0] | 000B: Disable (Default)<br>001B: RZQ/1(illegal if MR3 OP[0]=0B)<br>010B: RZQ/2<br>011B: RZQ/3(illegal if MR3 OP[0]=0B)<br>100B: RZQ/4<br>101B: RZQ/5(illegal if MR3 OP[0]=0B)<br>110B: RZQ/6(illegal if MR3 OP[0]=0B)<br>111B: RFU | 1,2,3 |
| ODTE-CK<br>(CK ODT enabled for non-terminating rank) | | OP[3] | ODT bond PAD is ignored<br>0B: ODT-CK Enable (Default)<br>1B: ODT-CK Disable | 2,3,4 |
| ODTE-CS<br>(CS ODT enable for non-terminating rank) | | OP[4] | ODT bond PAD is ignored<br>0B: ODT-CS Enable (Default)<br>1B: ODT-CS Disable | 2,3,4 |
| ODTD-CA<br>(CA ODT termination disable) | | OP[5] | ODT bond PAD is ignored<br>0B: ODT-CA Enable (Default)<br>1B: ODT-CA Disable | 2,3,4 |

Notes
1. All values are "typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. The ODT_CA pin is ignored by LPDDR4X devices. The ODT_CA pin shall be connected to either VDD2 or VSS. CA/ CS/ CK ODT is fully controlled through MR11 and MR22. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed.

### 1.4.24. MR23 Register Information (MA[5:0] = 17H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DQS interval timer run time setting | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| DQS interval timer run time | Write-Only | OP[7:0] | 00000000B: DQS timer stops via MPC Command (Default)<br>00000001B: DQS timer stops automatically at 16th clocks after timer start<br>00000010B: DQS timer stops automatically at 32nd clocks after timer start<br>00000011B: DQS timer stops automatically at 48th clocks after timer start<br>00000100B: DQS timer stops automatically at 64th clocks after timer start<br>---------- Thru ----------<br>00111111B: DQS timer stops automatically at (63X16)th clocks after timer start<br>01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start<br>10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start<br>11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start | 1, 2 |

Notes
1. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

### 1.4.25. MR24 Register Information (MA[5:0] = 18H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RAAMMT | | RAMMT | | | | | RFM |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| RFM(RFM Required) | Read-Only | OP[0] | 0B: RFM not required<br>1B: RFM required | 1 |
| RAAIMT (Rolling Accumulated ACT Initial Management Threshold) | | OP[5:1] | 00000B: Invalid<br>00001B: 8<br>00010B: 16<br>....<br>11110B: 240<br>11111B: 248 | 1 |
| RAAMMT (Rolling Accumulated ACT Maximum Management Threshold) | Write-Only | OP[6:4] | 00B: 2X<br>01B: 4X<br>10B: 6X<br>11B: 8X | 1 |

Notes
1. Vendor programmed.

### 1.4.26. MR25 Register Information (MA[5:0] = 19H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| PPR Resource | Read-Only | OP[7:0] | 0B: PPR Resource is not available<br>1B: PPR Resource is available | |

### 1.4.27. MR26 Register Information (MA[7:0] = 1AH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | | | | | SCL | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| SCL<br>(Scaling Level) | Read-Only | OP[1:0] | 00B: Level 0<br>01B: Level 1<br>10B: Level 2<br>11B: Level 3 | 1 |

Notes
1. Vendor programmed, OP[1:0] Scaling Parameter bits are valid only when MR0 OP[6] (Scaling Parameter support) = 1.

### 1.4.28. MR30 Register Information (MA[5:0] = 1EH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Valid 0 or 1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| SDRAM will ignore | Write-Only | OP[7:0] | Don't care | 1 |

Notes
1 This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

### 1.4.29. MR31 Register Information (MA[5:0] = 1FH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Bytemode Vref Selection | | RFU | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Bytemode Vref Selection-Lower Byte | Write-only | OP[6] | 0B : x16 device and no Byte mode selection(Default)<br>1B : Disable to update MR12/MR14 for lowerbyte | 1,2,3 |
| Bytemode Vref Selection-Upper Byte | | OP[7] | 0B : x16 device and no Byte mode selection(Default)<br>1B : Disable to update MR12/MR14 for upper byte | 1,2,3 |

Notes

1. The byte mode Vref selecion is optional. Please consult with vendors for the availability to support feature.
2. When Byte mode Vref selection is applied, the non-targeted byte is required to disable to update VrefCA and VrefDQ setting, assigned in MR12 and MR14 OP[6:0], for the other targeted byte.
   - In order to update MR12/MR14 setting only for upper byte, it is required to disable byte mode selection on lower byte, as applying MR31 OP[7:6] = 01B.
   - n order to update MR12/MR14 setting only for lower byte, it is required to disable byte mode selection on upper byte, as applying MR31 OP[7:6] = 10B.
   - When OP[7:6] = 00B is applied, both lower byte and upper byte will be updated.
3. When the configuration is not composed of byte mode device, MR31 OP[7:6] shall be the default value, 00B.

### 1.4.30. MR32 Register Information (MA[5:0] = 20H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DQ Calibration Pattern "A" (default = 5AH) | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Return DQ Calibration Pattern MR32 + MR40 | Write | OP[7:0] | XB: An MPC command with OP[6:0]=1000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5AH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information) | |

### 1.4.31. MR36 Register Information (MA[7:0] = 1BH)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | | | | | RAADEC | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| RAADEC (RAA Count Multiplier per RFM Command) | Read-Only | OP[1:0] | 00B: x1<br>01B: x1.5<br>10B: x2<br>11B: RFU | 1 |

Notes
1. OP[1:0] RAADEC bits are valid only when MR0 OP[2] (RFM support) = 1B.

### 1.4.32. MR39 Register Information (MA[5:0] = 27H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| Valid 0 or 1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| SDRAM will ignore | Write-only | OP[7:0] | Don't care | 1 |

Notes
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

### 1.4.33. MR40 Register Information (MA[5:0] = 28H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| DQ Calibration Pattern "B" (default = 3CH) | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Return DQ Calibration Pattern MR32 + MR40 | Write-Only | OP[7:0] | XB: A default pattern "3CH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register.<br>See MR32 for more information. | 1,2,3 |

Notes

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

### 1.4.34. MR51 Register Information (MA[7:0] = 33H)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|---|---|---|---|---|---|---|
| RFU | | | | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | RFU |

| Function | Register Type | Operand | Data | Notes |
|---|---|---|---|---|
| Single Ended RDQS | Write-Only | OP[1] | 0B : Differential Read DQS (Default)<br>1B : Single Ended Read DQS | 1,2,3,4,5 |
| Single Ended WDQS | | OP[2] | 0B : Differential Write DQS (Default)<br>1B : Single Ended Write DQS | 1,2,3,4,6 |
| Single Ended Clock | | OP[3] | 0B : Differential Clock (Default), CK_t/CK_c<br>1B : Single Ended Clock, Only CK_t | 1,2,3,4,7 |

Notes
1. The features described in MR51 are optional. Please check the vendor for the availability.
2. Device support for single ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5]
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
5. When single ended RDQS mode is enabled (MR51 OP[1] =1b), DRAM drives Read DQSB low or Hi-Z.
6. When single ended WDQS mode is enabled (MR51 OP[2] =1b), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
7. When single ended Clock mode is enabled (MR51 OP[3] =1b), CK_c is required to be at a valid logic level. A valid CK_c signal will meet this requirement.

# 2. Command Definitions and Timing Diagrams

## 2.1. Activate Command

The ACTIVATE command is composed of two consecutive commands, Activate-1 command and Activate-2. Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at $t_{RCD}$ after the ACTIVATE command is issed. After a bank has been activated it must be precharged before another ACTIVATE commnand can be applied to the same bank. The bank active and precharge times are defined as $t_{RAS}$ and $t_{RP}$ respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the device($t_{RC}$). The minimum time interval between ACTIVATE commands to different banks is $t_{RRD}$.

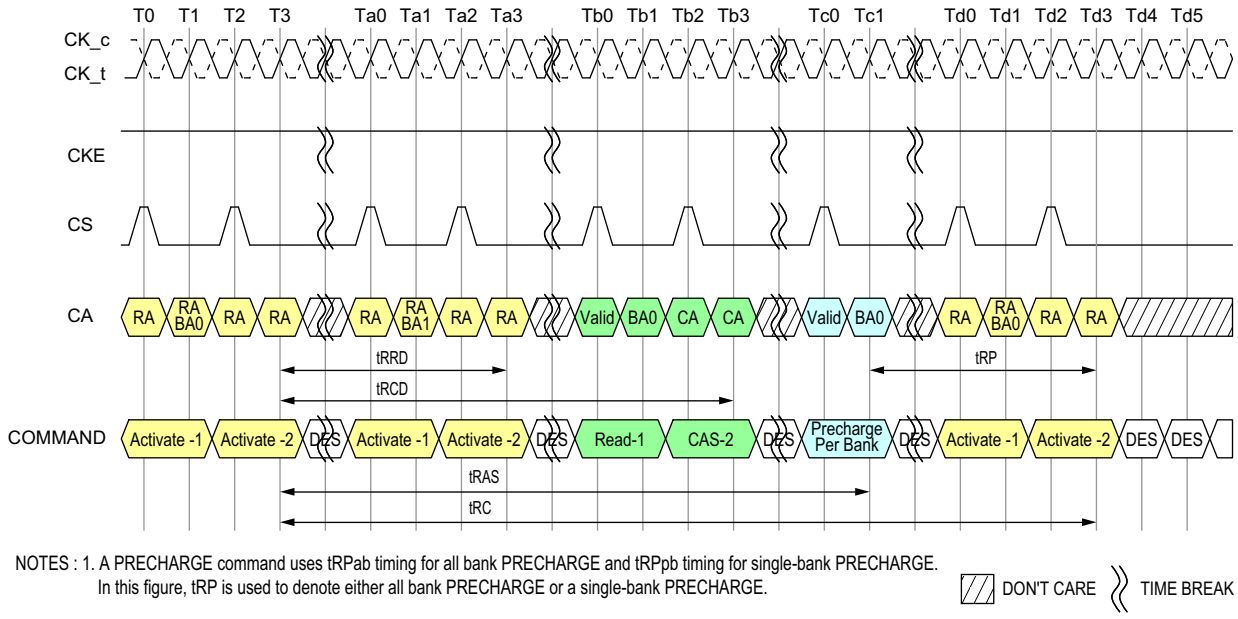



**Figure 4 - Activate Command**

## 2.2. 8-Bank Device Operation

Certain restrictions on operation of the 8-bank LPDDR4 devices must be observed. There are two rules: One rule restricts the number of sequential ACTIVATE commands that can be issued; the other provides more time for RAS precharge for a PRECHARGE ALL command. The rules are as follows:

**8 bank device Sequential Bank Activation Restriction:** No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW/tCK) is 10 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued at or between clock n + 1 and n + 9. REFpb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceeds the tFAW time.

**The 8-Bank Device Precharge-All Allowance:** tRP for a PRECHRGE ALL command must equal tRPab, which is greater than tRPpb.

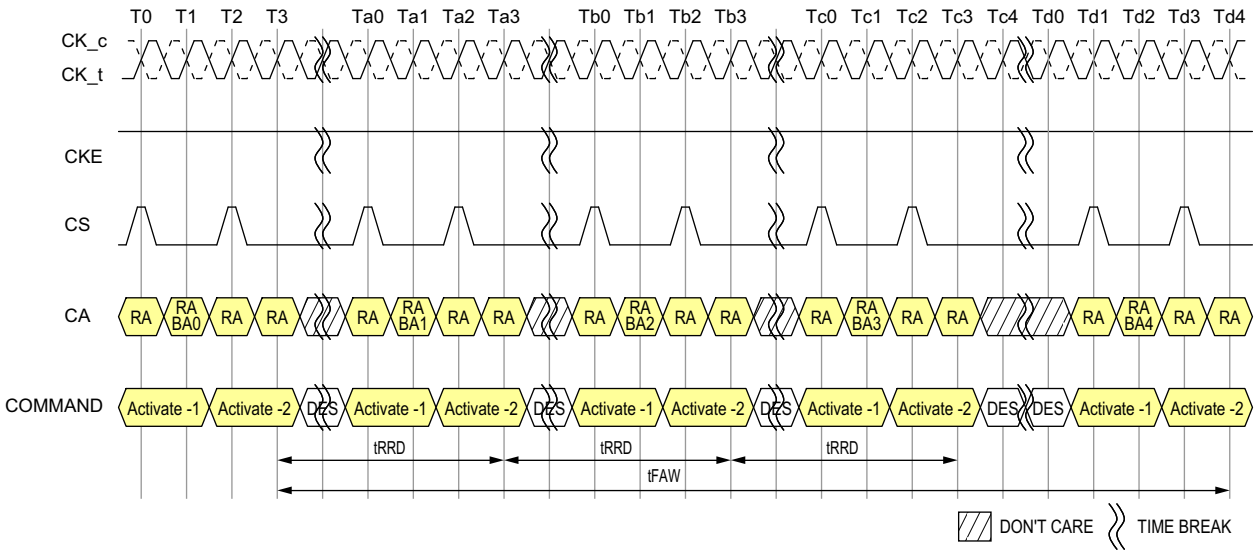



**Figure 5 - tFAW Timing**

## 2.3. Core Timing

**Table 16 - Core AC timing for x16 mode**

| Parameter | Symbol | min max | Data Rate | | | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | | |
| ACTIVATE-to-ACTIVATE command period (same bank) | tRC | min | tRAS + tRPab (with all bank precharge)<br>tRAS + tRPpb (with per bank precharge) | | | | | | | | ns | |
| Minimum Self Refresh Time (Entry to Exit) | tSR | min | max(15ns, 3nCK) | | | | | | | | ns | |
| Self Refresh exit to next valid command delay | tXSR | min | max(tRFCab + 7.5ns, 2nCK) | | | | | | | | ns | |
| Exit Power-Down to next valid command delay | tXP | min | max(7.5ns, 5nCK) | | | | | | | | ns | |
| CAS-to-CAS delay | tCCD | min | 8 | | | | | | | | tCK (avg) | 3 |
| Internal READ to PRECHARGE command delay | tRTP | min | max(7.5ns, 8nCK) | | | | | | | | ns | |
| RAS-to-CAS delay | tRCD | min | max(18ns, 4nCK) | | | | | | | | ns | |
| Row precharge time (single bank) | tRPpb | min | max(18ns, 4nCK) | | | | | | | | ns | |
| Row precharge time (all banks) | tRPab | min | max(21ns, 4nCK) | | | | | | | | ns | |
| Row active time | tRAS | min | max(42ns, 3nCK) | | | | | | | | ns | |
| | | mas | min(9 * tREFI * Refresh Rate, 70.2us) | | | | | | | | us | 4 |
| WRITE recovery time | tWR | min | max(18ns, 6nCK) | | | | | | | | ns | |
| WRITE-to-READ delay | tWTR | min | max(10ns, 8nCK) | | | | | | | | ns | |
| Active bank-A to active bank-B[1] | tRRD | min | max(10ns, 4nCK) | | | | | | | max (7.5ns, 4nCK)[2] | ns | |
| Precharge to Precharge Delay | tPPD | min | 4 | | | | | | | | tCK (avg) | 1 |
| Four-bank ACTIVATE window | tFAW | min | 40 | | | | | | | 30[2] | ns | |

Notes
1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. Device supporting 4266 Mbps specification shall support these timing at lower data rates.
3. The value is based on BL16. For BL32 need additional 8 tCK (avg) delay.
4. Refresh Rate is specified by MR4 OP[2:0].

## 2.4. Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see 2.47.1. "Command Truth Table") at a rising edge of CK.

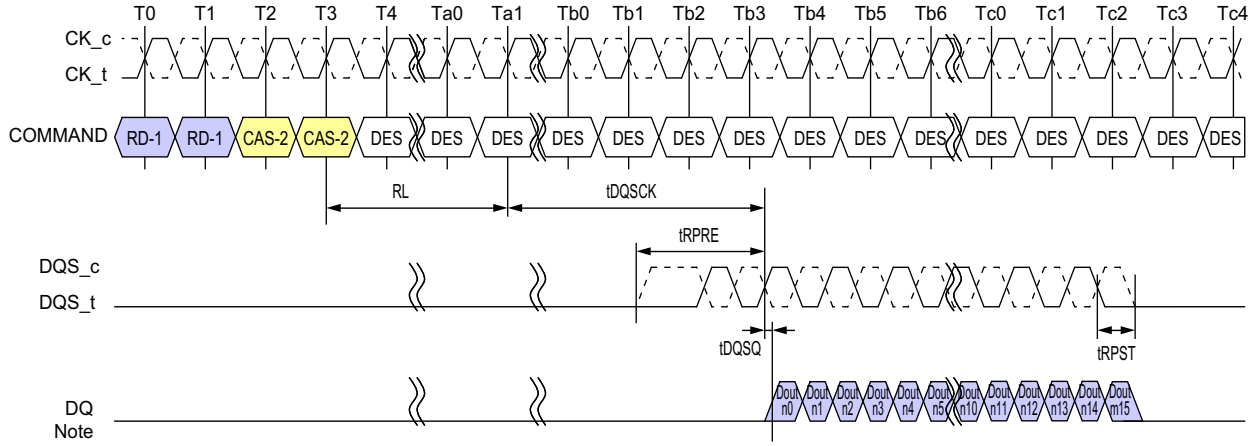
The LPDDR4-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see 2.47.1. "Command Truth Table").

## 2.5. Read Preamble and Postamble

The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS_t with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

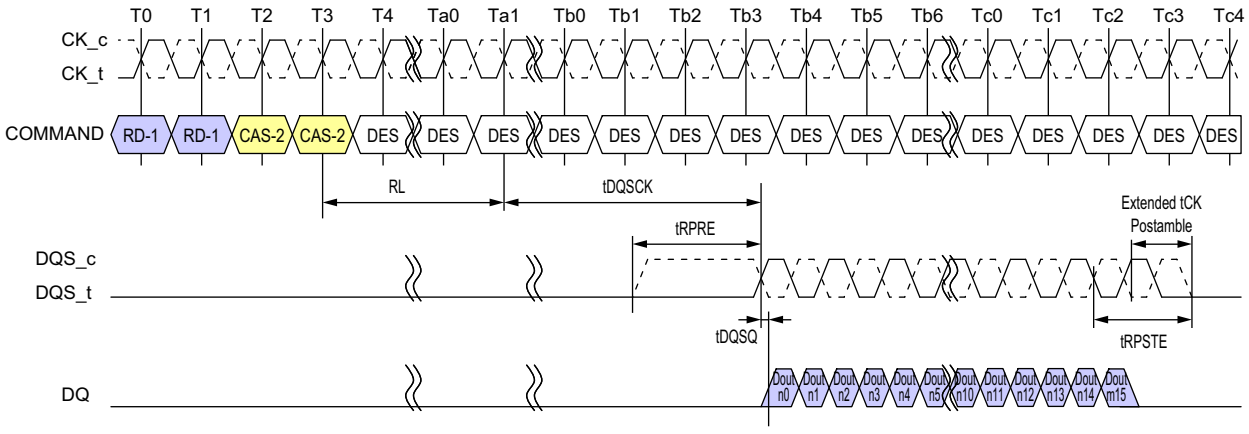
For READ operations the pre-amble is 2*tCK, but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4 will have a DQS Read post-amble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS postamble will be 0.5*tCK driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. The drawings below show examples of DQS Read post-amble for both standard (tRPST) and extended (tRPSTE ) post-amble operation.




Note
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ.
3. DQS_t/DQS_c is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

**Figure 6 - DQS Read Preamble and Postamble: Toggling Preamble and 0.5nCK Postamble**




Note
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (Extended)
2. DQS and DQ terminated VSSQ.
3. DQS_t/DQS_c is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

**Figure 7 - DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble**

## 2.6. Burst Read Operation

A burst Read command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be "0", so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e. post-preamble) rising edge of the data strobe. Each subsequent dataout appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c.

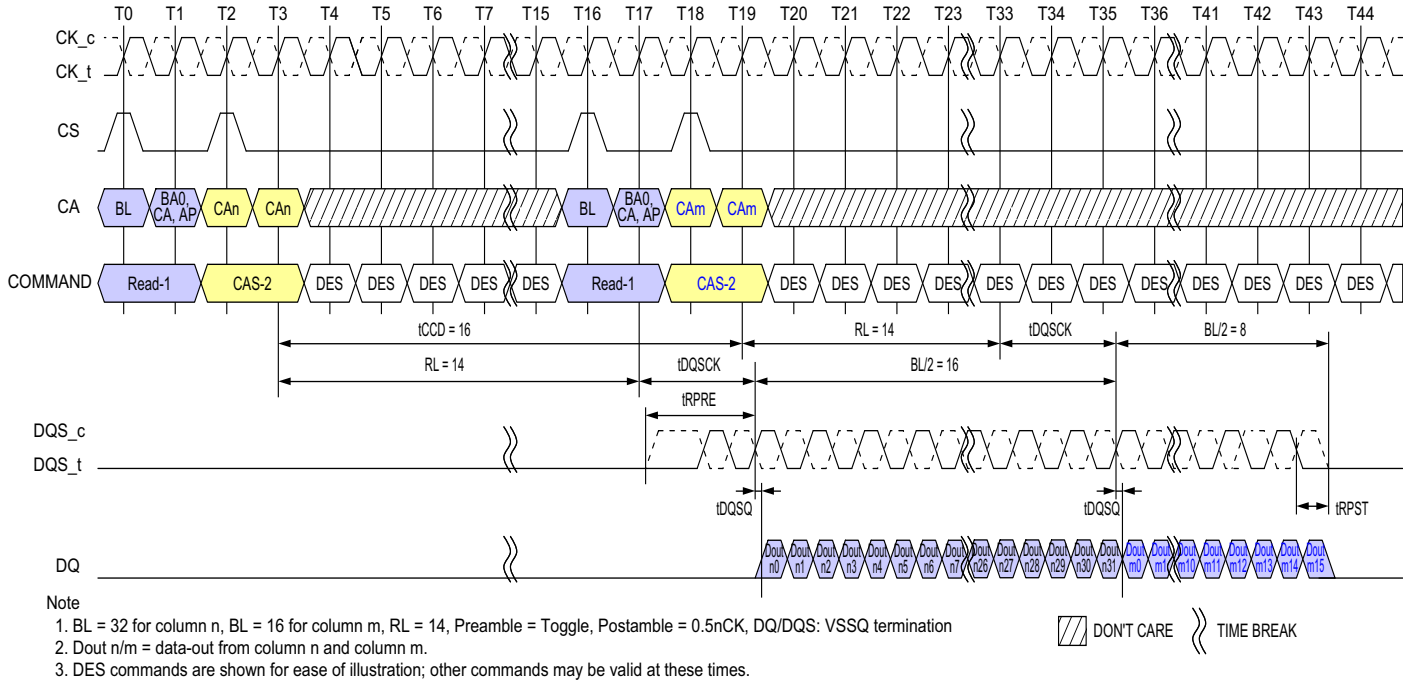
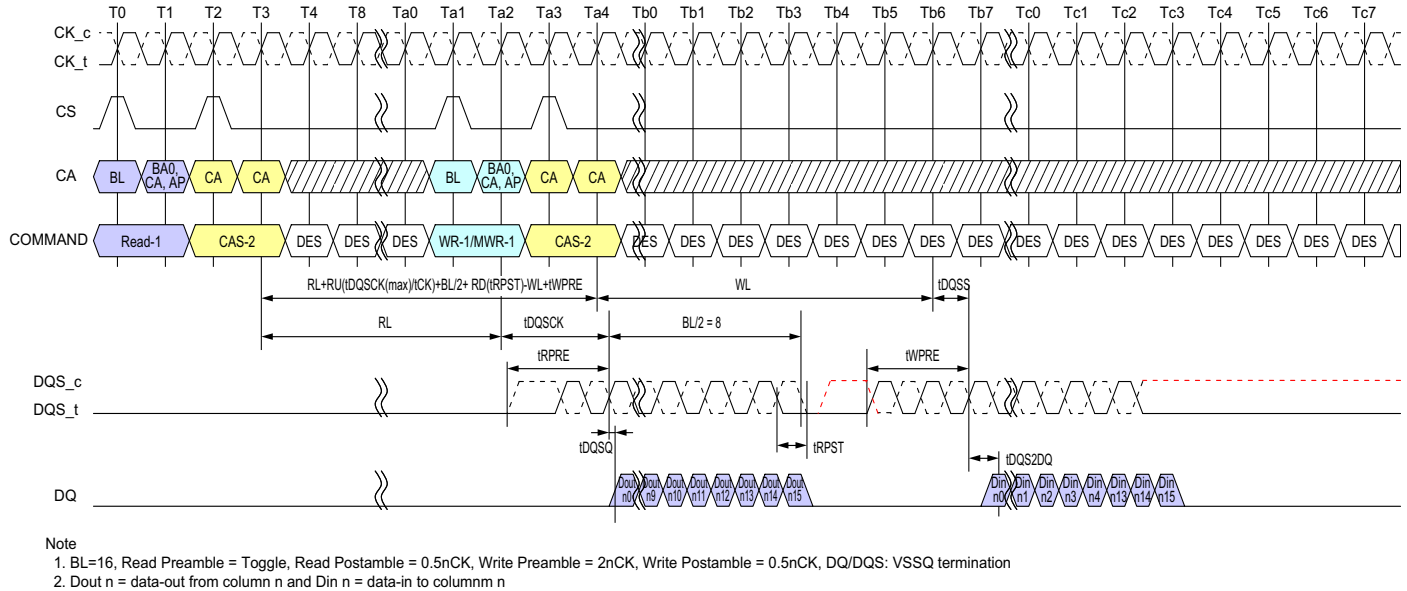


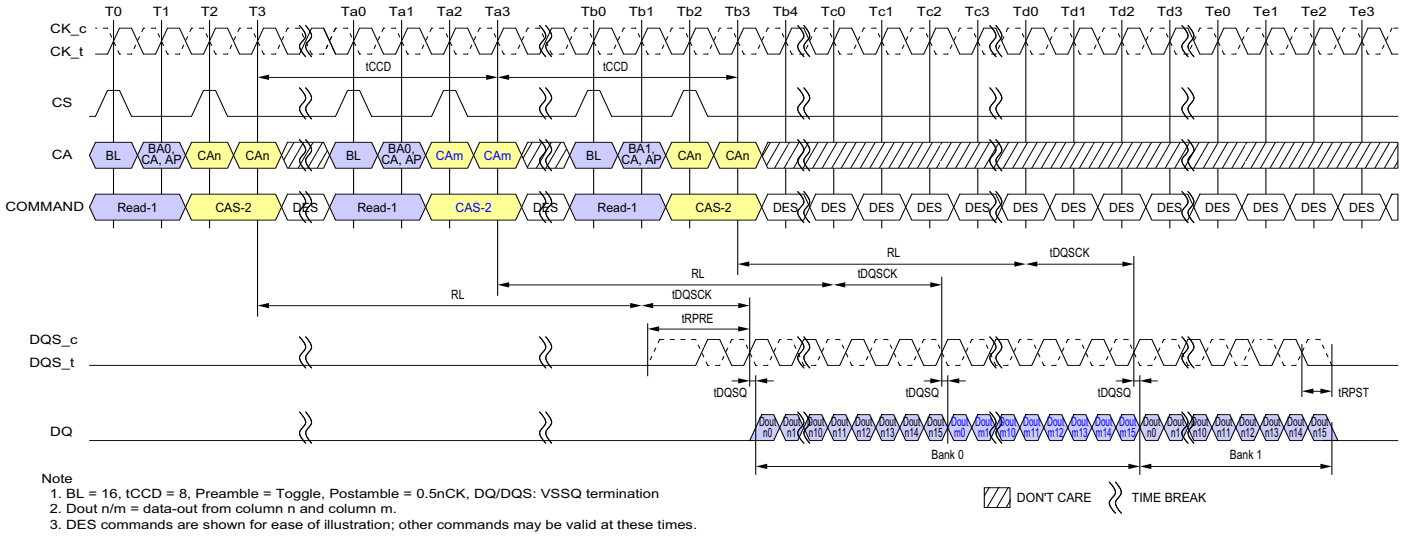

**Figure 8 - Burst Read Timing**




Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to columnn n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 9 - Burst Read followed by Burst Write or Burst Mask Write**

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL). Minimum READ-to-WRITE or MASK WRITE latency is RL+RU(tDQSCK(max)/tCK)+BL/2+ RD(tRPST)-WL+tWPRE.



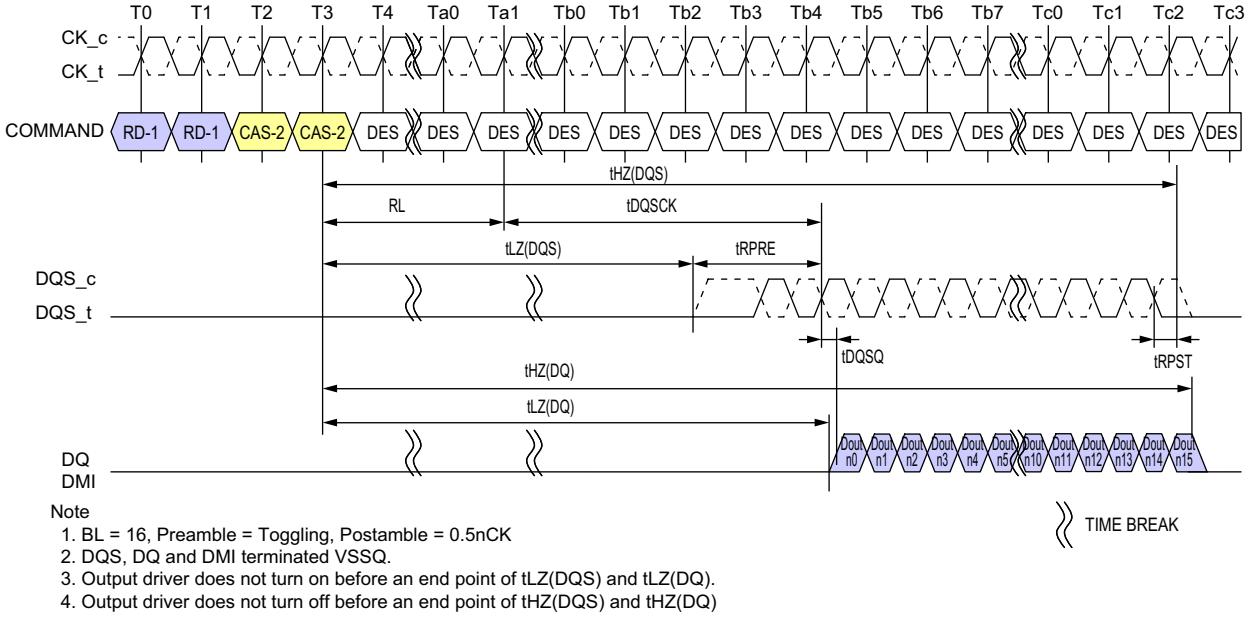

Note
1. BL = 16, tCCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 10 - Seamless Burst Read**

The seamless Burst READ operation is supported by placing a READ command at every tCCD(min) interval for BL16 (or every 2 x tCCD for BL32). The seamless Burst READ can access any open bank.

## 2.7. Read Timing

The read timing is shown in following figure.




Note
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS, DQ and DMI terminated VSSQ.
3. Output driver does not turn on before an end point of tLZ(DQS) and tLZ(DQ).
4. Output driver does not turn off before an end point of tHZ(DQS) and tHZ(DQ)

**Figure 11 - Read Timing**

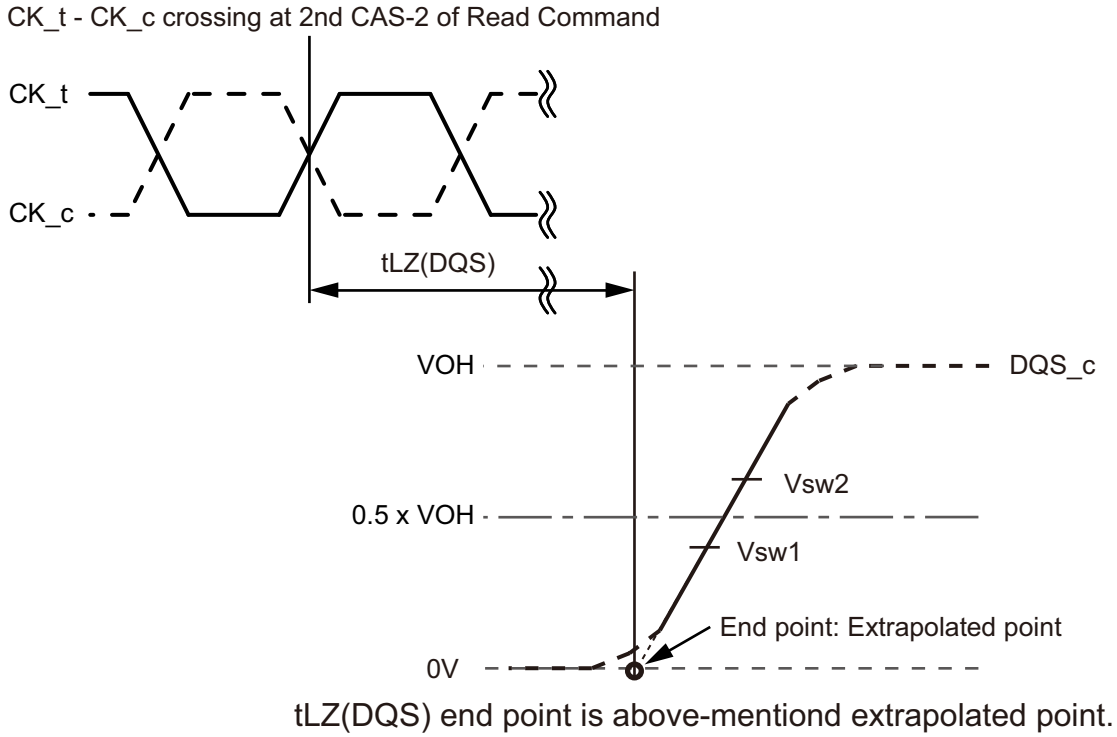
### 2.7.1. tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

This section shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

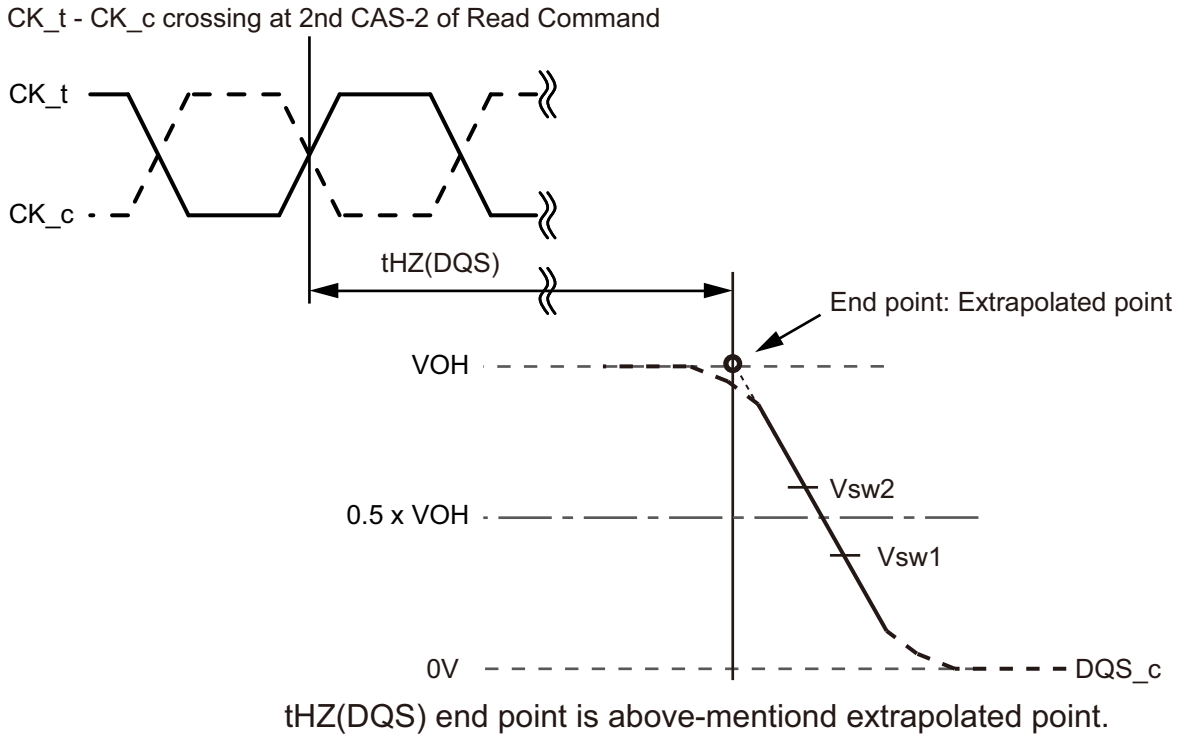
### 2.7.2. tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment)

The calculation method is shown in Figure 12 and Figure 13, and Table 17




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQS_t and DQS_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

**Figure 12 - tLZ(DQS) method for calculating transitions and end point**




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQS_t and DQS_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

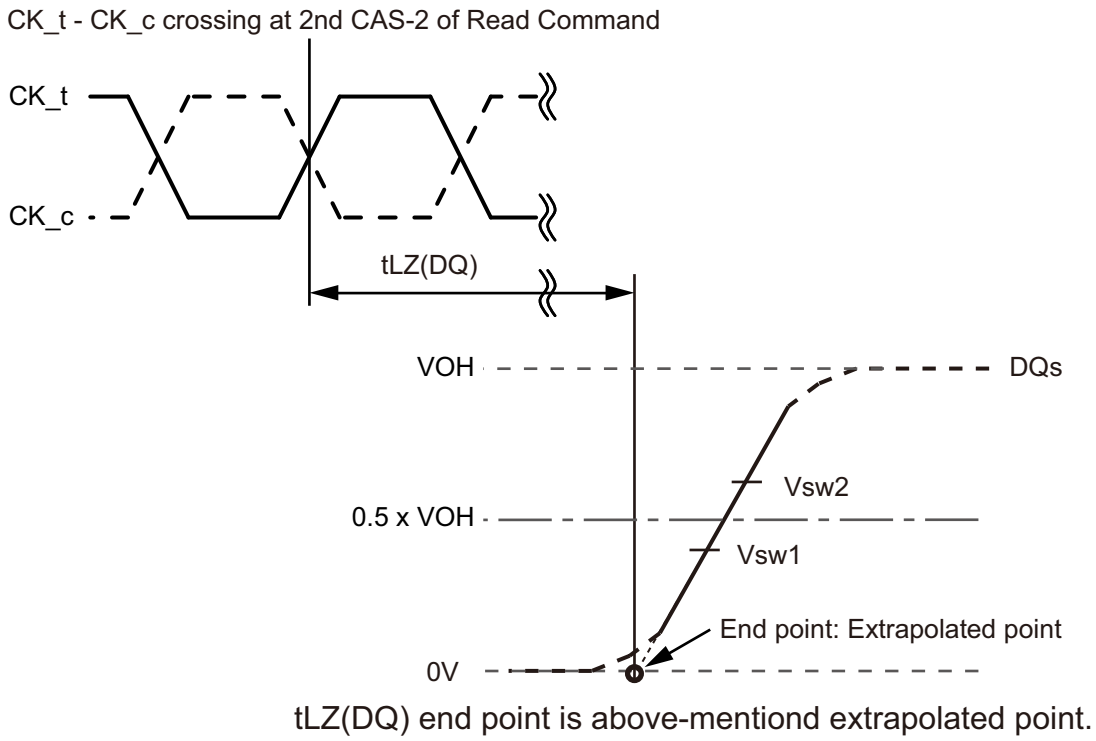
**Figure 13 - tHZ(DQS) method for calculating transitions and end point**

**Table 17 - Reference voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

| Measured Parameter | Symbol | Vsw1 [V] | Vsw2 [V] |
|---|---|---|---|
| DQS_c low-impedance time from CK_t, CK_c | tLZ(DQS) | 0.4 x VOH | 0.6 x VOH |
| DQS_c high impedance time from CK_t, CK_c | tHZ(DQS) | 0.4 x VOH | 0.6 x VOH |

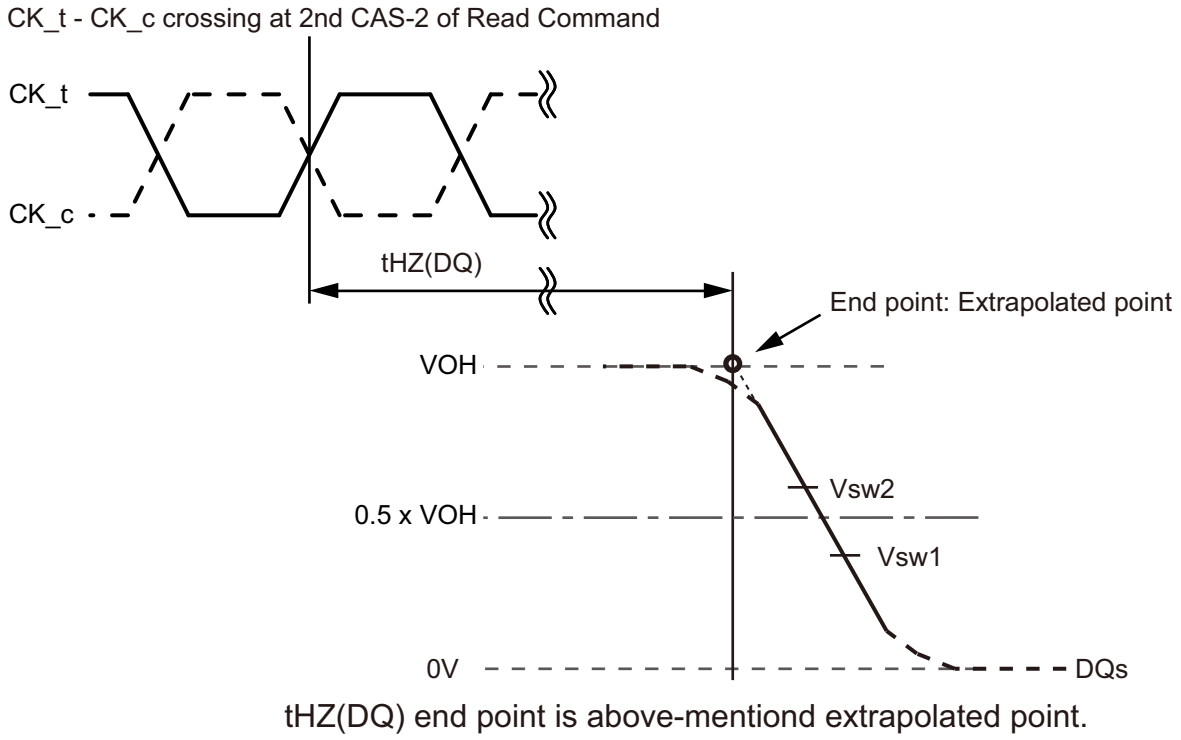
### 2.7.3. tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)

The calculation method is shown in Figure 14 and Figure 15 and Table 18.




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

**Figure 14 - tLZ(DQ) method for calculating transitions and end point**




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

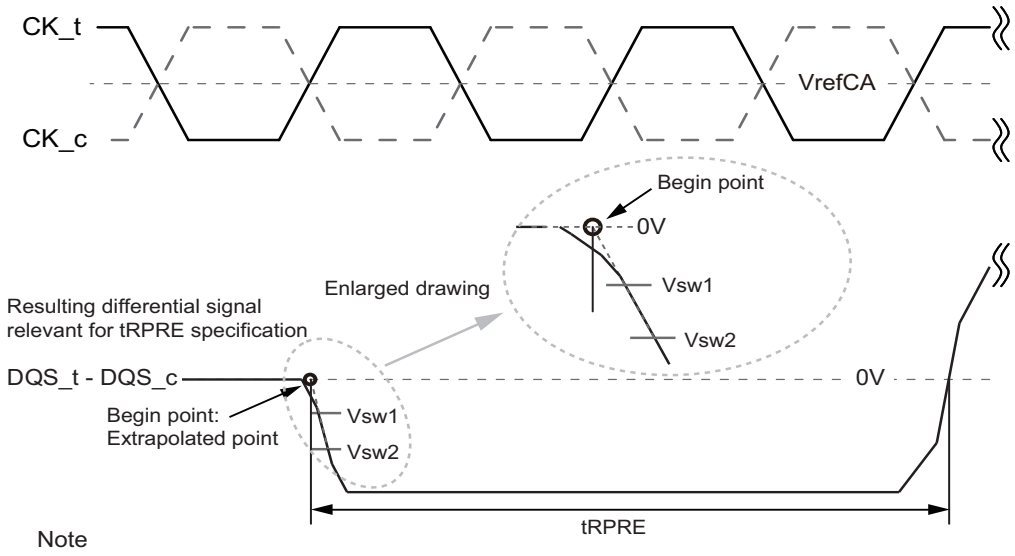
**Figure 15 - tHZ(DQ) method for calculating transitions and end point**

**Table 18 - Reference voltage for tLZ(DQS), tHZ(DQS) Timing Measurements**

| Measured Parameter | Symbol | Vsw1 [V] | Vsw2 [V] |
|---|---|---|---|
| DQ low-impedance time from CK_t, CK_c | tLZ(DQ) | 0.4 x VOH | 0.6 x VOH |
| DQ high impedance time from CK_t, CK_c | tHZ(DQ) | 0.4 x VOH | 0.6 x VOH |

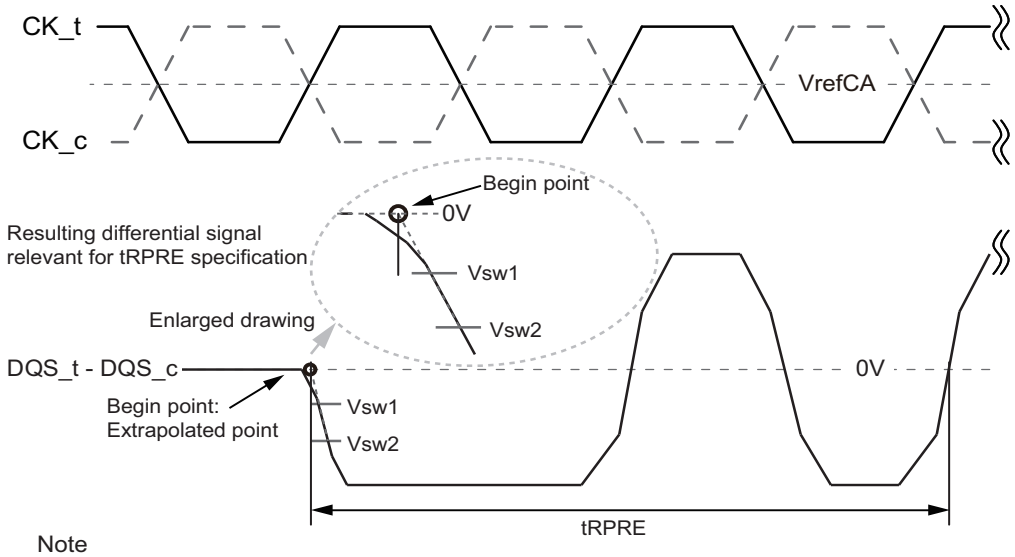
### 2.7.4. tRPRE Calculation for ATE(Automatic Test Equipment)

The method for calculating differential pulse widths for tRPRE is shown in Figure below.




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Static

**Figure 16 - 18 Method for calculating tRPRE transitions and endpoints**




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Toggle

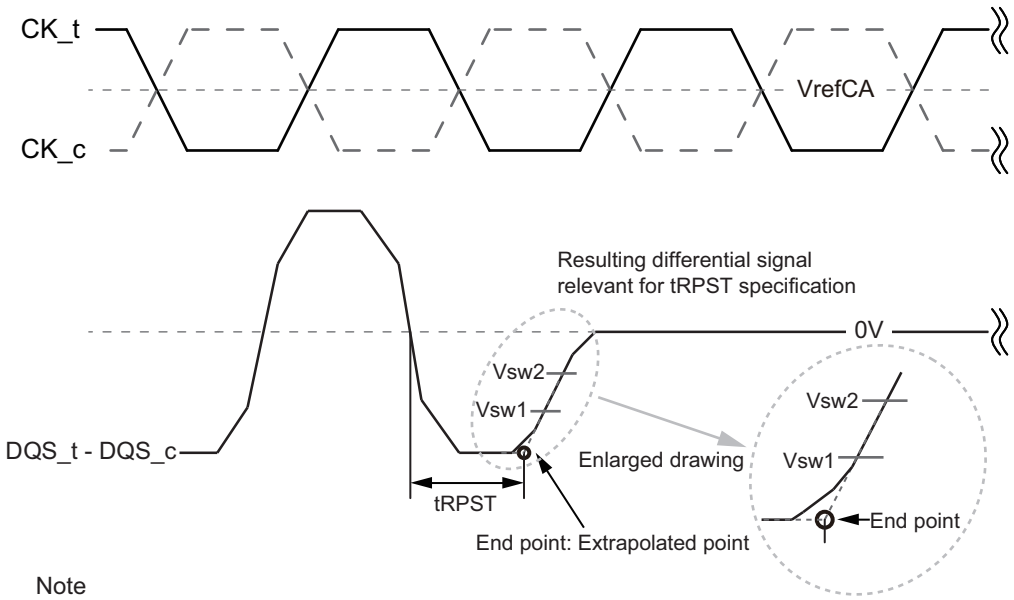
**Figure 17 - Method for calculating tRPRE transitions and endpoints**

**Table 19 - Reference Voltage for tRPRE Timing Measurements**

| Measured Parameter | Symbol | Vsw1[V] | Vsw2[V] | Note |
|---|---|---|---|---|
| DQS_t, DQS_c differential Read Preamble | tRPRE | -(0.3 x VOH) | -(0.7 x VOH) | |

### 2.7.5. tRPST Calculation for ATE(Automatic Test Equipment)

The method for calculating differential pulse widths for tRPST is shown in Figure below.




Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ/3.
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Read Postamble: 0.5tCK
4. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure 18 - 20 Method for calculating tRPST transitions and endpoints**

**Table 20 - Reference Voltage for tRPST Timing Measurements**

| Measured Parameter | Symbol | Vsw1[V] | Vsw2[V] | Note |
|---|---|---|---|---|
| DQS_t, DQS_c differential Read Postamble | tRPST | -(0.7 x VOH) | -(0.3 x VOH) | |

**Table 21 - Read AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read preamble | tRPRE | min | 1.8 | | | | | | | | tCK (avg) | |
| Read postamble | tRPST | min | 0.4 | | | | | | | | tCK (avg) | |
| Extended Read postamble | tRPSTE | min | 1.4 | | | | | | | | tCK (avg) | |
| DQ low-impedance time from CK_t, CK_c | tLZ(DQ) | Min | (RL x tCK) + tDQSCK(Min) - 200ps | | | | | | | | ps | |
| DQ high impedance time from CK_t, CK_c | tHZ(DQ) | Max | (RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100ps | | | | | | | | ps | |
| DQS_c low-impedance time from CK_t, CK_c | tLZ(DQS) | Min | (RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200ps | | | | | | | | ps | |
| DQS_c high impedance time from CK_t, CK_c | tHZ(DQS) | Max | (RL x tCK) + tDQSCK(Max) +(BL/2 x tCK) + (RPST(Max) x tCK) - 100ps | | | | | | | | ps | |
| DQS-DQ skew | tDQSQ | max | 0.18 | | | | | | | | UI | |

## 2.8. tDQSCK Timing Table

**Table 22 - tDQSCK AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQS Output Access Time from CK_t/CK_c | tDQSCK | min | 1.5 | | | | | | | | ns | 1 |
| | | max | 3.5 | | | | | | | | | |
| DQS Output Access Time from CK_t/CK_c - Temperature Variation | tDQSCK_temp | max | 4 | | | | | | | | ps/°C | 2 |
| DQS Output Access Time from CK_t/CK_c - Voltage Variation | tDQSCK_volt | max | 7 | | | | | | | | ps/mV | 3 |

Notes

1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
2. tDQSCK_temp max delay variation as a function of Temperature.
3. tDQSCK_volt max delay variation as a function of DC voltage variation for $V_{DDQ}$ and $V_{DD2}$. tDQSCK_volt should be used to calculate timing variation due to $V_{DDQ}$ and $V_{DD2}$ noise < 20 MHz. Host controller do not need to account for any variation due to $V_{DDQ}$ and $V_{DD2}$ noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement $V_{DDQ}$ = $V_{DD2}$ is assumed.

### 2.8.1. CK to DQS Rank to Rank Variation

**Table 23 - tDQSCK_rank2rank AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CK to DQS rank to Rank Variation | tDQSCK_rank2rank | max | 1.0 | | | | | | | | ns | 1,2 |

Notes

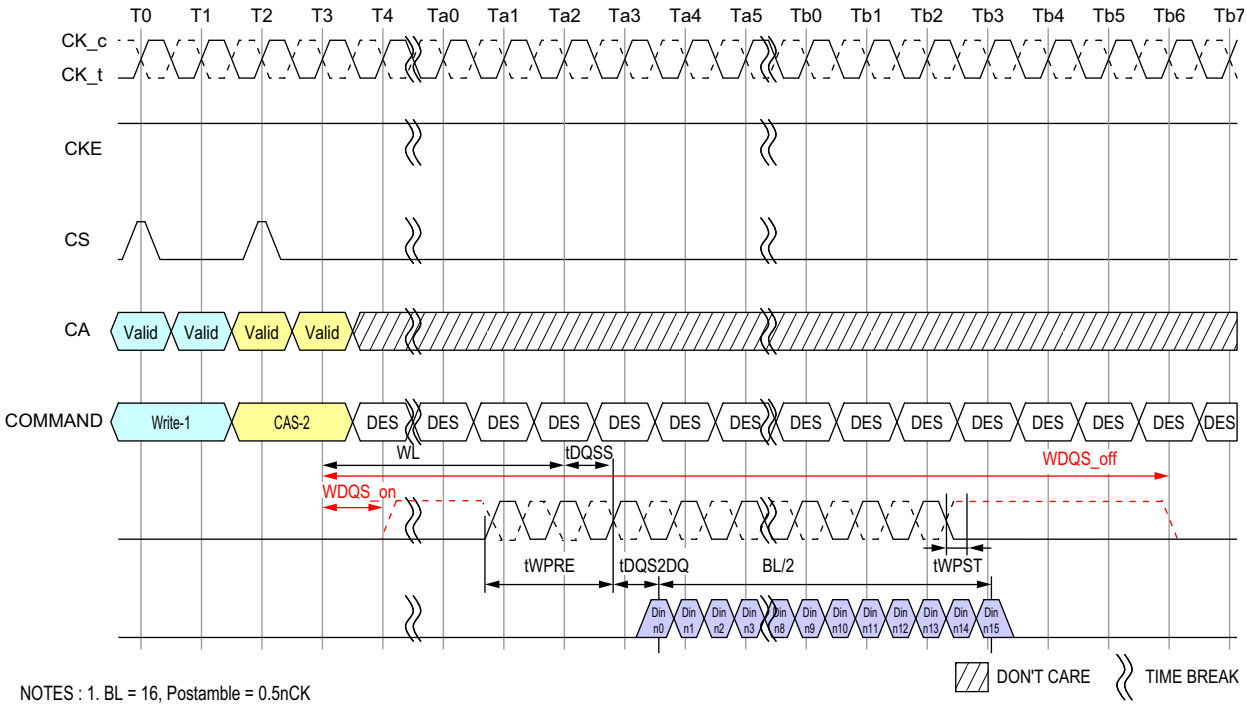
1. The same voltage and temperature are applied to tDQS2CK_rank2rank.
2. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

## 2.9. Write Preamble and Postamble

The DQS strobe for the LPDDR4-SDRAM requires a pre-amble prior to the first latching edge (the rising edge of DQS_t with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

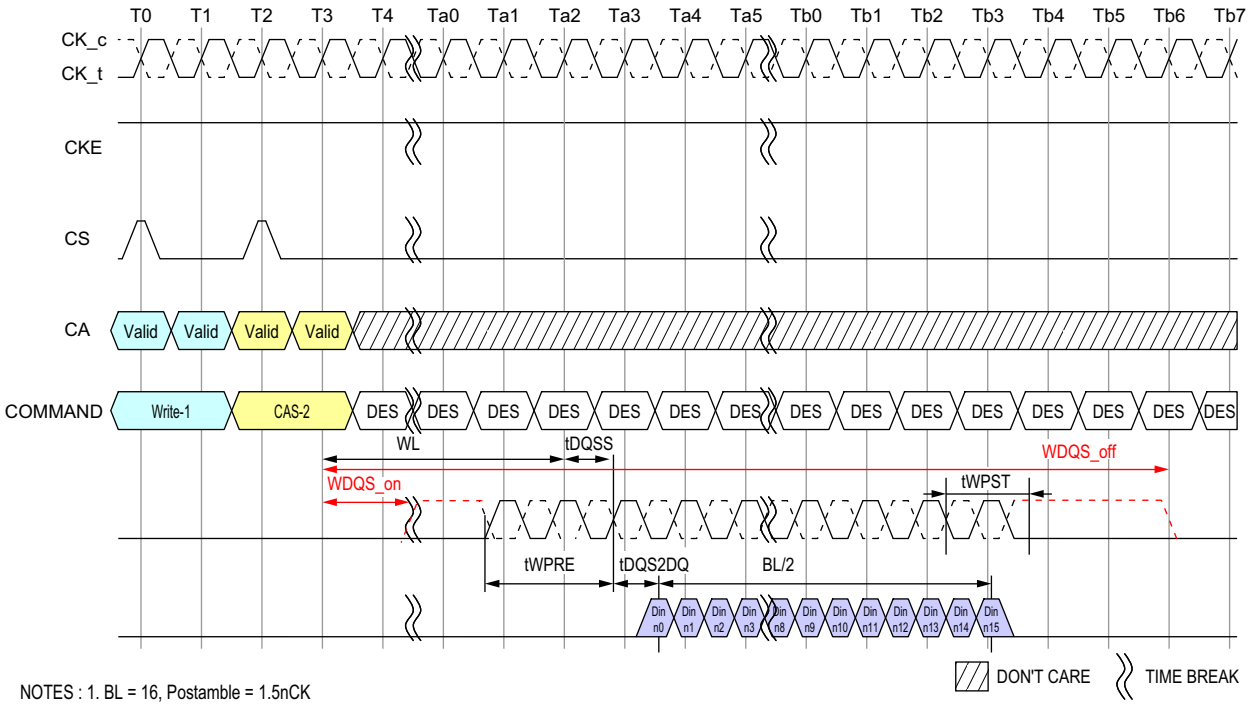
For WRITE operations, a 2*tCK pre-amble is required at all operating frequencies.

LPDDR4 will have a DQS Write post-amble of 0.5*tCK or extended to 1.5*tCK. Standard DQS post-amble will be 0.5*tCK driven by the memory controller for Writes. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Write post-amble. The drawings below show examples of DQS Write post-amble for both standard (tWPST) and extended (tWPSTE ) post-amble operation.




NOTES : 1. BL = 16, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ
3. DQS_t/DQS_c is "don't care" prior to the start of tWPRE.
No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tWPRE.

**Figure 19 - DQS Write Preamble and Postamble; 0.5nCK Postamble**



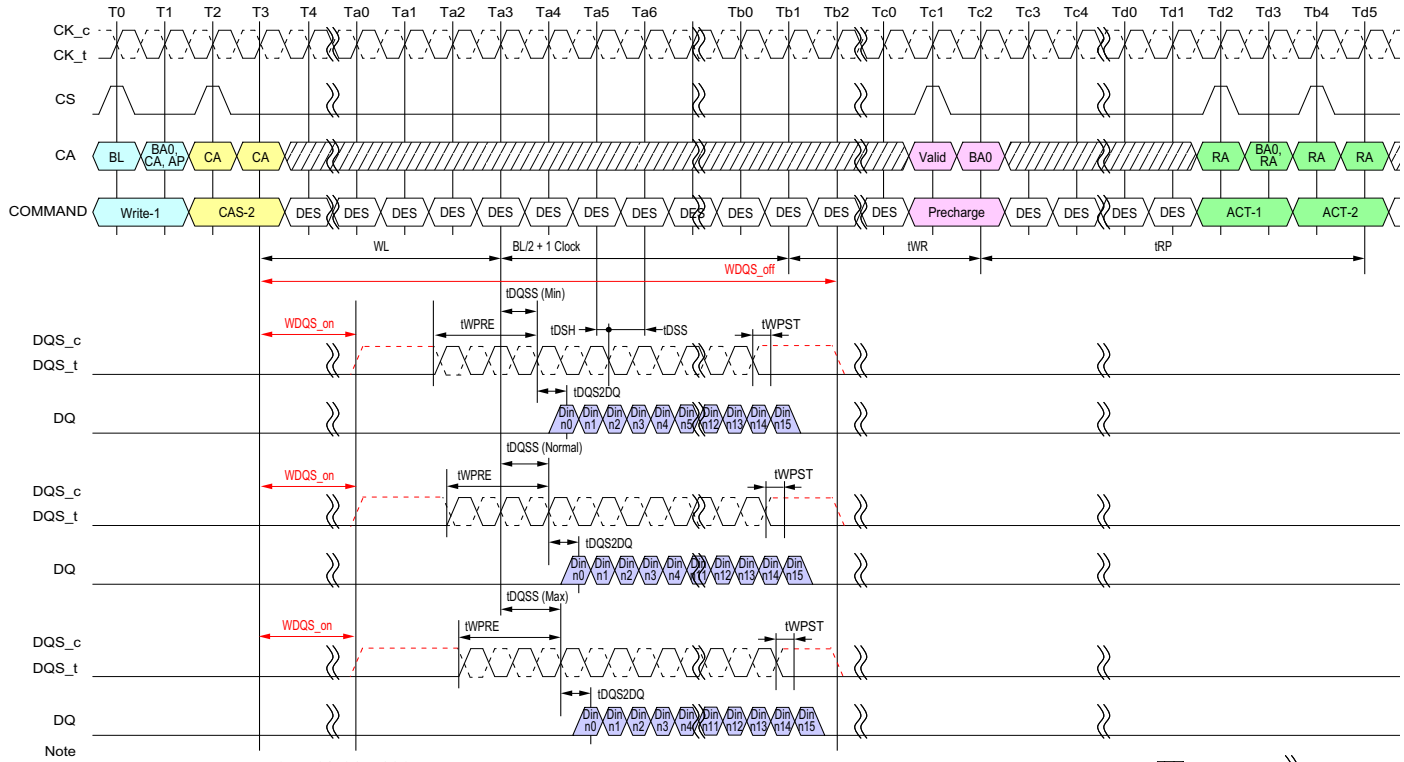

NOTES : 1. BL = 16, Postamble = 1.5nCK
2. DQS and DQ terminated VSSQ
3. DQS_t/DQS_c is "don't care" prior to the start of tWPRE.
No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tWPRE.

**Figure 20 - DQS Write Preamble and Postamble: 1.5nCK Postamble**

## 2.10. Burst Write Operation

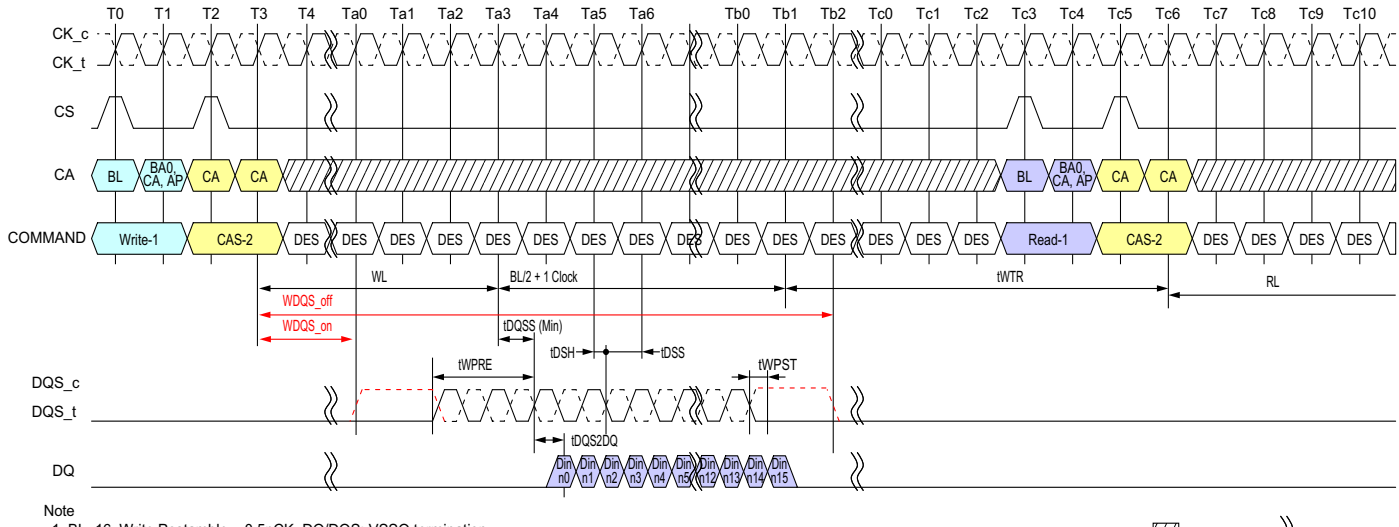
A burst WRITE command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid "latching" edge of DQS must be driven WL * tCK + tDQSS after the rising edge of Clock that completes a write command.

The LPDDR4-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE pre-amble is required to be 2 x tCK. The DQS strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (WRITE post-amble) after the completion of the burst WRITE. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the cross point of DQS_t and DQS_c.




Note
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnn n
3. The minimum number of clock cycles from the burst write command to the precharge command for same bank is [WL + 1 + BL/2 + RU(tWR/tCK)].
4. tWR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 21 - Burst Write Operation**

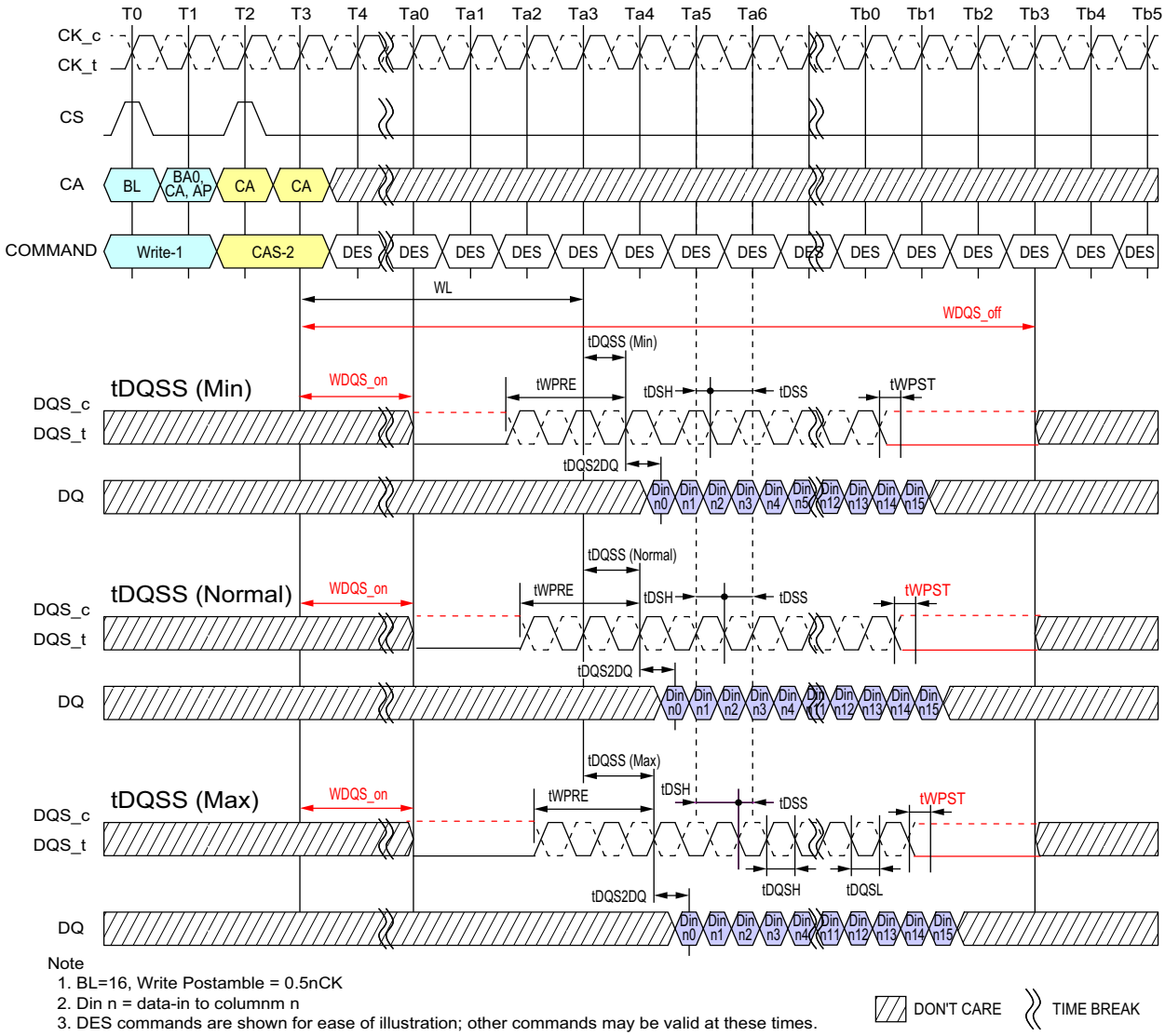



Note
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnn n
3. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 22 - Burst Write Followed by Burst Read**

## 2.11. Write Timing

The write timing is shown in the following figure.



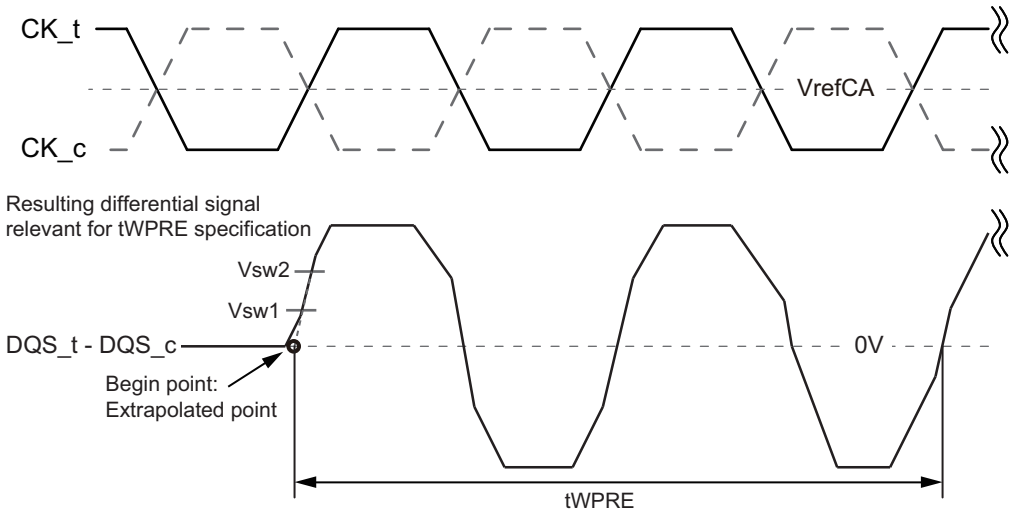

Note
1. BL=16, Write Postamble = 0.5nCK
2. Din n = data-in to columnm n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

DON'T CARE TIME BREAK

**Figure 23 - Write Timing**

### 2.11.1. tWPRE Calculation for ATE (Automated Test Equipment)

The method for calculating differential pulse widths for tWPRE is shown in the following figure.




Note
1. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.

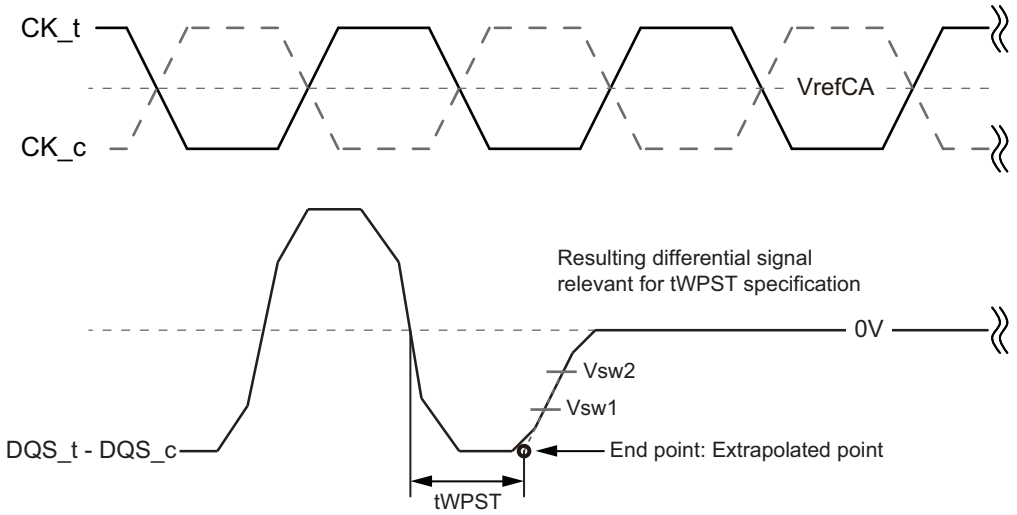
**Figure 24 - Method for calculating tWPRE transitions and endpoints**

**Table 24 - Reference Voltage for tWPRE Timing Measurements**

| Measured Parameter | Symbol | Vsw1 [V] | Vsw2 [V] |
|---|---|---|---|
| DQS_t, DQS_c differential Write Preamble | tWPRE | VIHL_AC x 0.3 | VIHL_AC x 0.7 |

### 2.11.2. tWPST Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tWPST is shown in the follwing figure.




Note
1. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
2. Write Postamble: 0.5tCK
3. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

**Figure 25 - Method for calculating tWPST transitions and endpoints**

**Table 25 - Reference Voltage for tWPRE Timing Measurements**

| Measured Parameter | Symbol | Vsw1 [V] | Vsw2 [V] |
|---|---|---|---|
| DQS_t, DQS_c differential Write Preamble | tWPST | - (VIHL_AC x 0.7) | - (VIHL_AC x 0.3) |

**Table 26 - Write AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write command to 1st DQS latching transition | tDQSS | Min | 0.75 | | | | | | | | tCK (avg) | |
| | | Max | 1.25 | | | | | | | | | |
| DQS input high-level width | tDQSH | Min | 0.4 | | | | | | | | tCK | |
| DQS input low-level width | tDQSL | Min | 0.4 | | | | | | | | tCK | |
| DQS falling edge to CK setup time | tDSS | Min | 0.2 | | | | | | | | tCK (avg) | |
| DQS falling edge hold time from CK | tDSH | Min | 0.2 | | | | | | | | tCK (avg) | |
| Write preamble | tWPRE | Min | 1.8 | | | | | | | | tCK | |
| 0.5 tCK Write postamble | tWPST | Min | 0.4 | | | | | | | | tCK | 1 |
| 1.5 tCK Write postamble | tWPST | Min | 1.4 | | | | | | | | tCK | 1 |

Notes
1. The length of Write Postamble depends on MR3 OP1 setting.

## 2.12. Read and Write Latencies

**Table 27 - Read and Write Latencies for x16 mode**

| Read Latency | | Write Latency | | nWR | nRTP | Freq. limit (Greater than) | Freq. limit (Same or less than) | Notes |
|---|---|---|---|---|---|---|---|---|
| No DBI | w/ DBI | Set "A" | Set "B" | | | | | |
| 6 | 6 | 4 | 4 | 6 | 8 | 10 | 266 | 1,2,3,4,5,6 |
| 10 | 12 | 6 | 8 | 10 | 8 | 266 | 533 | |
| 14 | 16 | 8 | 12 | 16 | 8 | 533 | 800 | |
| 20 | 22 | 10 | 18 | 20 | 8 | 800 | 1066 | |
| 24 | 28 | 12 | 22 | 24 | 10 | 1066 | 1333 | |
| 28 | 32 | 14 | 26 | 30 | 12 | 1333 | 1600 | |
| 32 | 36 | 16 | 30 | 34 | 14 | 1600 | 1866 | |
| 36 | 40 | 18 | 34 | 40 | 16 | 1866 | 2133 | |
| nCK | nCK | nCK | nCK | nCK | nCK | MHz | MHz | |

Notes

1. The LPDDR4-SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3-OP[6]. When MR3-OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3-OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set "A" and Set "B" is determined by MR2-OP[6]. When MR2-OP[6]=0, then Write Latency Set "A" should be used. When MR2-OP[6]=1, then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write burst with AP (auto-pre-charge) enabled. It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Read burst with AP (auto-pre-charge) enabled. It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a pre-charge.

## 2.13. Write and Masked Write operation DQS controls (WDQS Control)

LPDDR4-SDRAMs support write and masked write operations with the following DQS controls. Before and after Write and Masked Write operations are issued, DQS_t/DQS_c is required to have a sufficient voltage gap to make sure the write buffers operating normally without any risk of metastability.

The LPDDR4-SDRAM is supported by either of two WDQS control modes

Mode 1: Read Based Control

Mode 2 : WDQS_on / WDQS_off definition based control

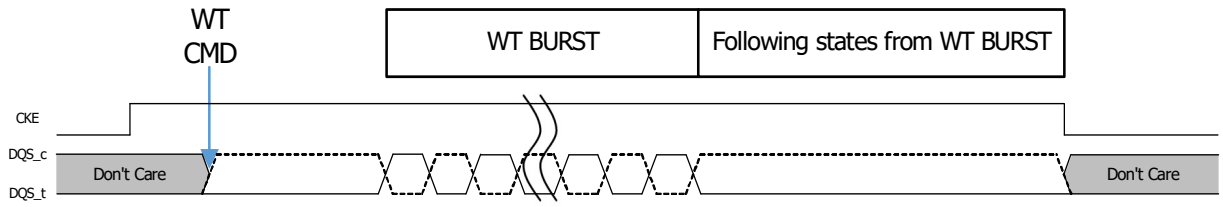
Regardless of ODT enable/disable, WDQS related timing described in 2.13 does not allow any change of existing command timing constraints for all read/write operations. In case of any conflict or ambiguity on the command timing constraints caused by what is specified in 2.13, the specifications defined in 2.35, Table 72 (or 2.13.1, and 2.13.2) should have higher priority than WDQS control requirements.

Some legacy products may not provide WDQS control described below. However, in order to prevent the write preamble related failure, it is strongly recommended to support either of two WDQS controls to LPDDR4-SDRAMs. In the case of legacy SoC which may not provide WDQS control modes, it is required to consult DRAM vendors to guarantee the write / masked write operation appropriately.

### 2.13.1. WDQS Control Mode 1 - Read Based Control

The LPDDR4-SDRAM needs to be guaranteed the differential WDQS, but the differential WDQS can be controlled as described below. WDQS control requirements here can be ignored while differential read DQS is operated or while DQS hands over from Read to Write and vice versa.

1. At the time a write / masked write command is issued, SoC makes the transition from driving DQS_c high to driving differential DQS_t/DQS_c, followed by normal differential burst on DQS pins.
2. At the end of post amble of write /masked write burst, SoC resumes driving DQS_c high through the subsequent states except for DQS toggling and DQS turn around time of WT-RD and RD-WT as long as CKE is high.
3. When CKE is low, the state of DQS_t and DQS_c is allowed to be "Don't Care".



### 2.13.2. WDQS Control Mode 2 - WDQS_on/off

After write / masked write command is issued, DQS_t and DQS_c required to be differential from WDQS_on, and DQS_t and DQS_c can be "Don't Care" status from WDQS_off of write / masked write command. When ODT is enabled, WDQS_on and WDQS_off timing is located in the middle of the operations. When host disables ODT, WDQS_on and WDQS_off constraints conflict with tRTW. The timing does not conflict when ODT is enabled because WDQS_on and WDQS_off timing is covered in ODTLon and ODTLoff. However, regardless of ODT on/off, WDQS_on/off timing below does not change any command timing constraints for all read and write operations. In order to prevent the conflict, WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD). In addition, the period during DQS toggling caused by Read and Write can be counted as WDQS_on/off.

Parameters

- WDQS_on: the max delay from write / masked write command to differential DQS_t and DQS_c.
- WDQS_off : the min delay for DQS_t and DQS_c differential input after the last write / masked write command.
- WDQS_Exception : the period where WDQS_on and WDQS_off timing is overlapped with read operation or with DQS turn around (RD-WT, WT-RD).

- WDQS_Exception @ ODT disable = max (WL-WDQS_on+tDQSTA- tWPRE - n*tCK, 0 tCK) where RD to WT command gap = tRTW(min)@ODT disable + n*tCK
- WDQS_Exception @ ODT enable = tDQSTA

**Table 28 - WDQS_on / WDQS_off Definition**

| RL | | WL | | nWR | nRTP | WDQS_on (max) | | WDQS_off (min) | | Lower Clock Freq limit (>) | Upper Clock Freq limit (<=) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Set A | Set B | Set A | Set B | | | Set A | Set B | Set A | Set B | | |
| 6 | 6 | 4 | 4 | 6 | 8 | 0 | 0 | 15 | 15 | 10 | 266 |
| 10 | 12 | 6 | 8 | 10 | 8 | 0 | 0 | 18 | 20 | 266 | 533 |
| 14 | 16 | 8 | 12 | 16 | 8 | 0 | 6 | 21 | 25 | 533 | 800 |
| 20 | 22 | 10 | 18 | 20 | 8 | 4 | 12 | 24 | 32 | 800 | 1066 |
| 24 | 28 | 12 | 22 | 24 | 10 | 4 | 14 | 27 | 37 | 1066 | 1333 |
| 28 | 32 | 14 | 26 | 30 | 12 | 6 | 18 | 30 | 42 | 1333 | 1600 |
| 32 | 36 | 16 | 30 | 34 | 14 | 6 | 20 | 33 | 47 | 1600 | 1866 |
| 36 | 40 | 18 | 34 | 40 | 16 | 8 | 24 | 36 | 52 | 1866 | 2133 |
| nCK | nCK | nCK | nCK | nCK | nCK | nCK | nCK | nCK | nCK | Mhz | Mhz |

Notes
1. WDQS_on/off requirement can be ignored wWDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).
2. The period DQS toggling caused by Read and Write can be counted as WDQS_on/off.

**Table 29 - WDQS_on / WDQS_off Allowable Variation Range**

| | min | max | Unit |
|---|---|---|---|
| WDQS_On | -0.25 | +0.25 | tCK (avg) |
| WDQS_Off | -0.25 | +0.25 | tCK (avg) |

**Table 30 - DQS turn around parameter**

| Parameter | Description | Value | Unit | Notes |
|---|---|---|---|---|
| tDQSTA | Turn-around time RDQS to WDQS for WDQS control case | TBD | - | 1 |

Notes
1. tDQSTA is only applied to WDQS_exception case when WDQS Control. Except for WDQS Control, tDQSTA can be ignored.

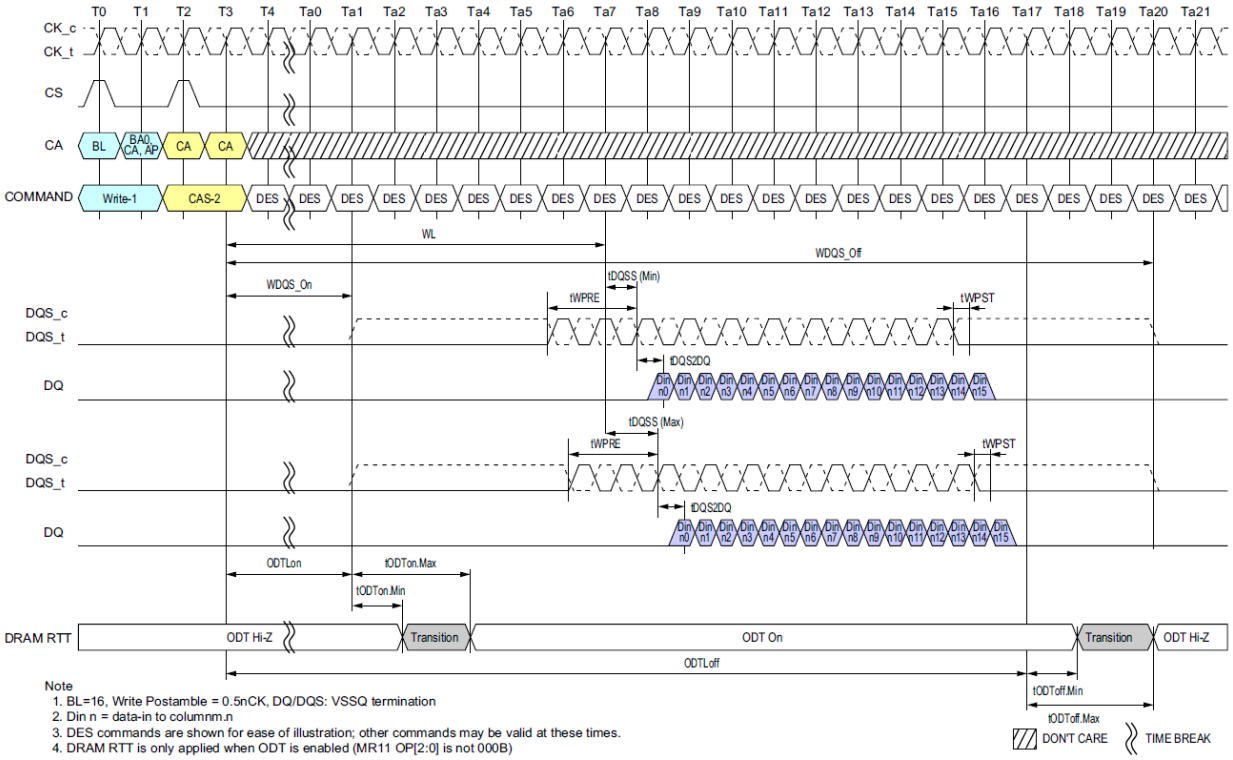
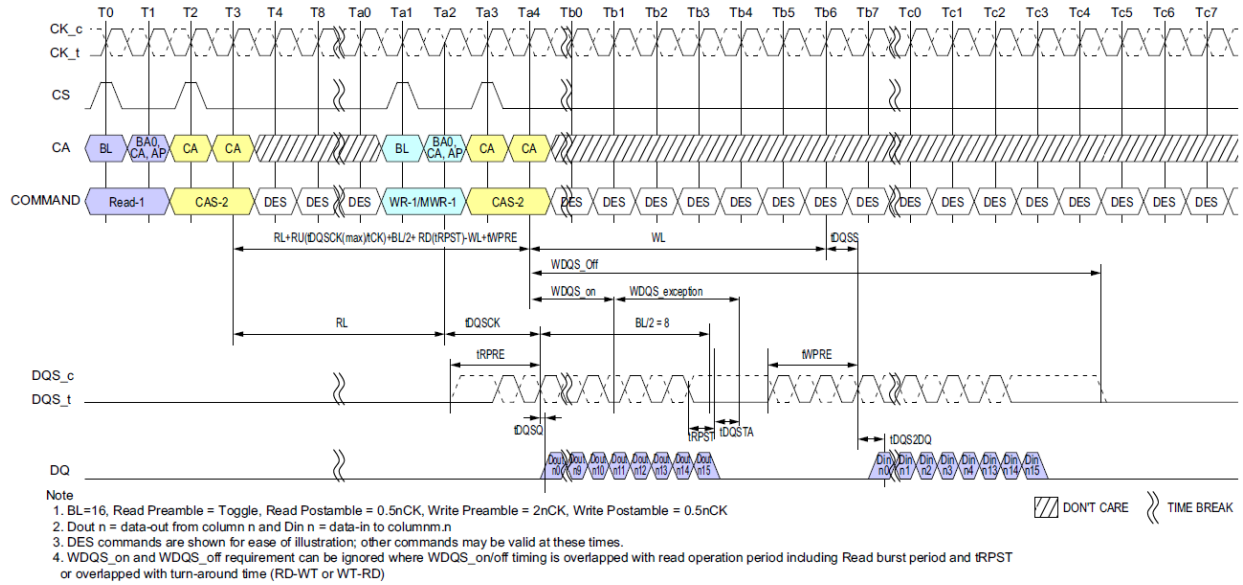
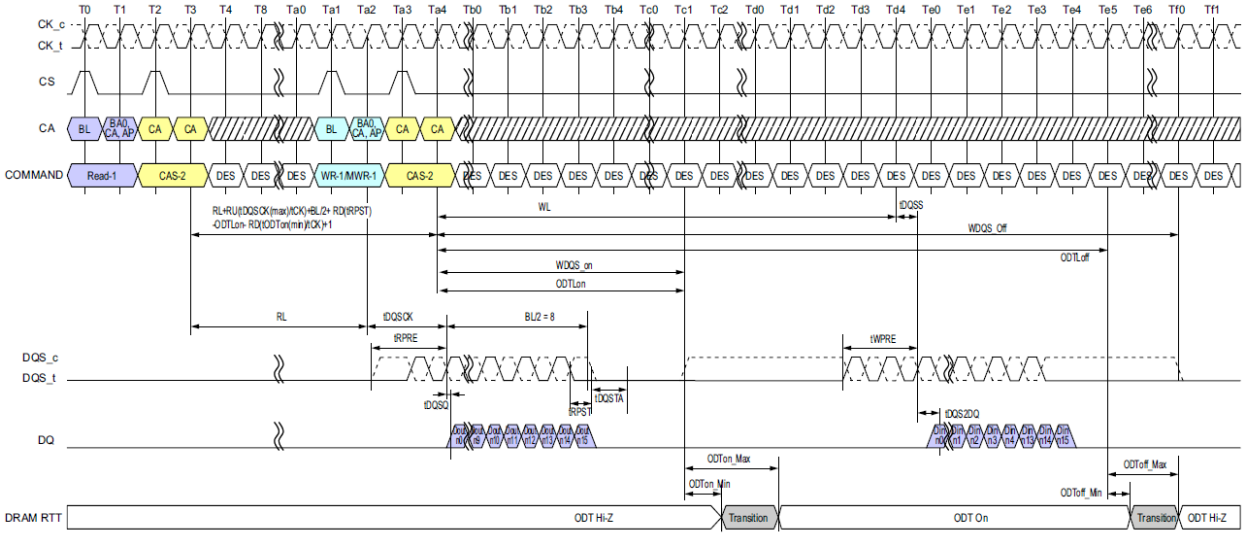



**Figure 26 - Burst Write Operation**




Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK
2. Dout n = data-out from column n and Din n = data-in to columnm.n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

**Figure 27 - Burst Read followed by Burst Write or Burst Mask Write (ODT Disable)**




Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to columnm.n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

**Figure 28 - Burst Read followed by Burst Write or Burst Mask Write (ODT Enable)**

## 2.14. Postamble and Preamble merging behavior

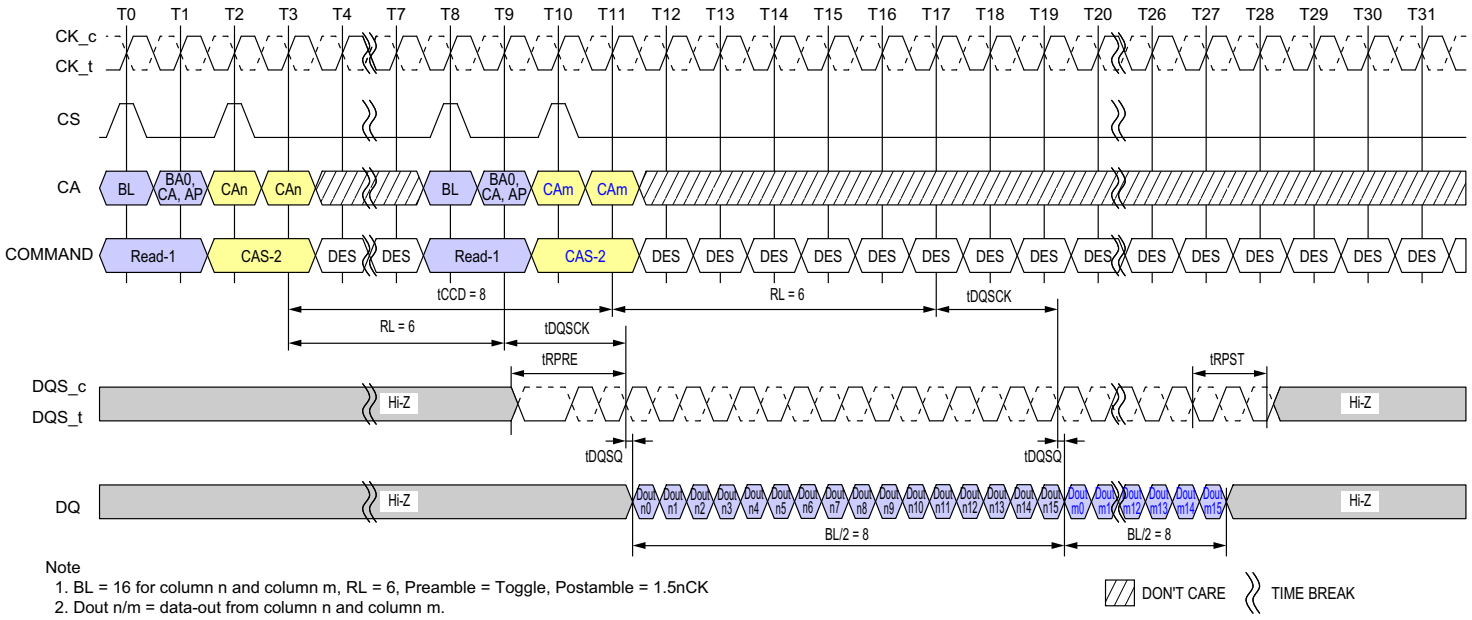
The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via Mode Register Write commands.

In Read to Read or Write to Write operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command will disappear to create consecutive DQS latching edge for seamless burst operations.

But in the case of Read to Read or Write to Write operations with command interval of tCCD+1,tCCD+2, etc., they will not completely disappear because it's not seamless burst operations.

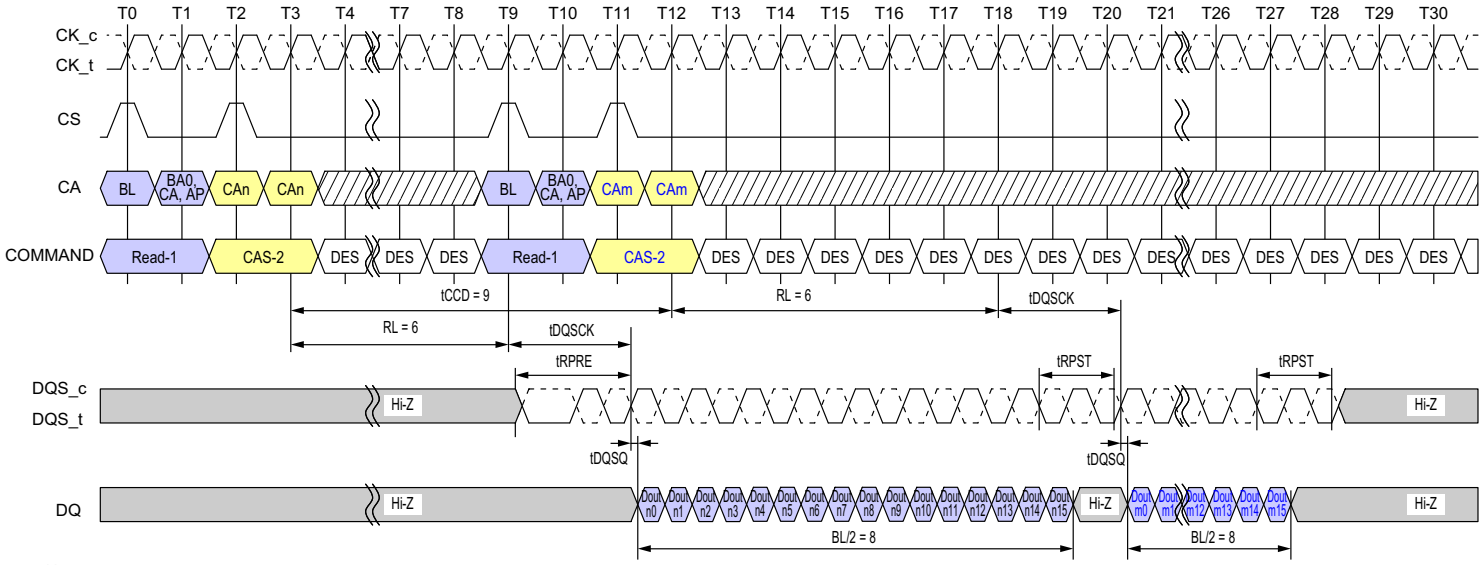
Timing diagrams in this material describe Postamble and Preamble merging behavior in Read to Read or Write to Write operations with tCCD+n.

### 2.14.1. Read to Read Operation



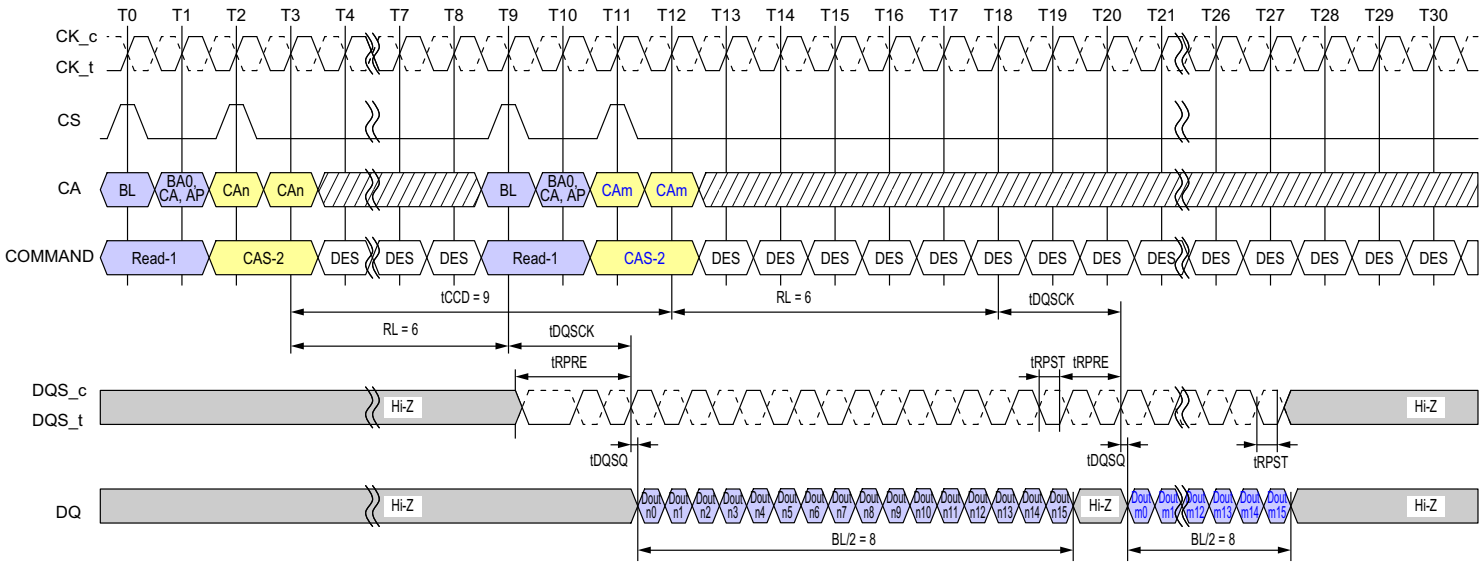

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 29 - Seamless Reads Operation: tCCD = Min, Preamble = Toggle, 1.5nCK Postamble**



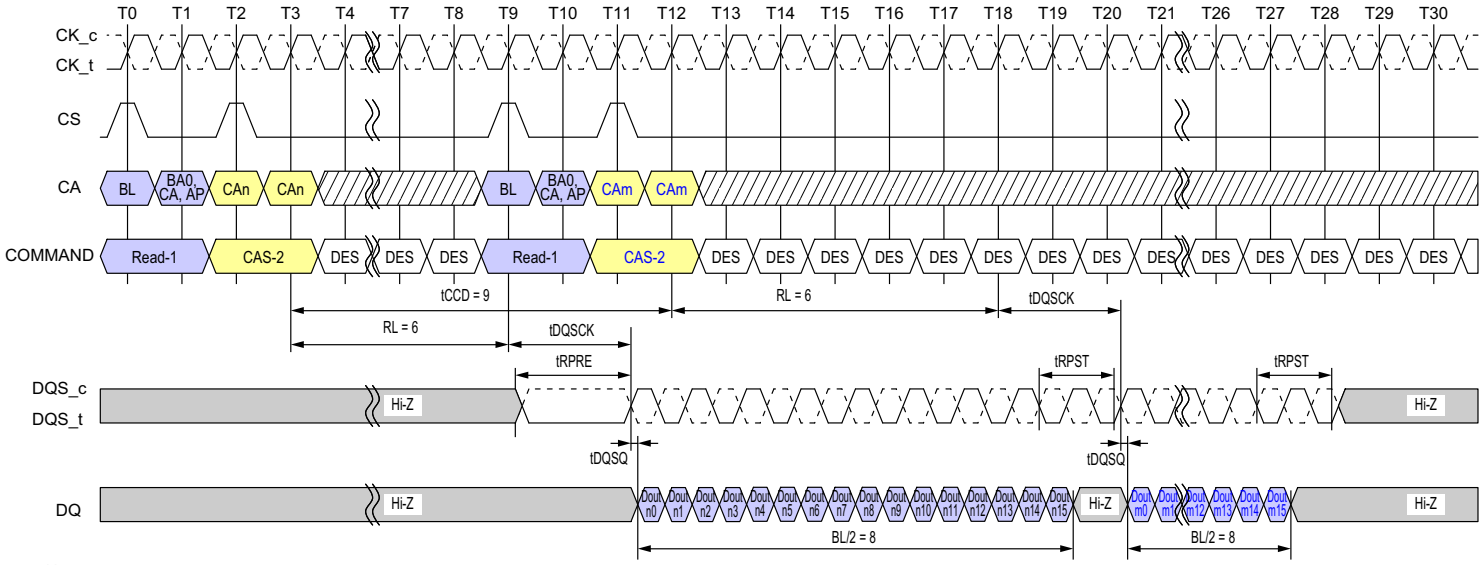

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 30 - Consecutive Reads Operation: tCCD = Min+1, Preamble=Toggle, 1.5nCK Postamble**



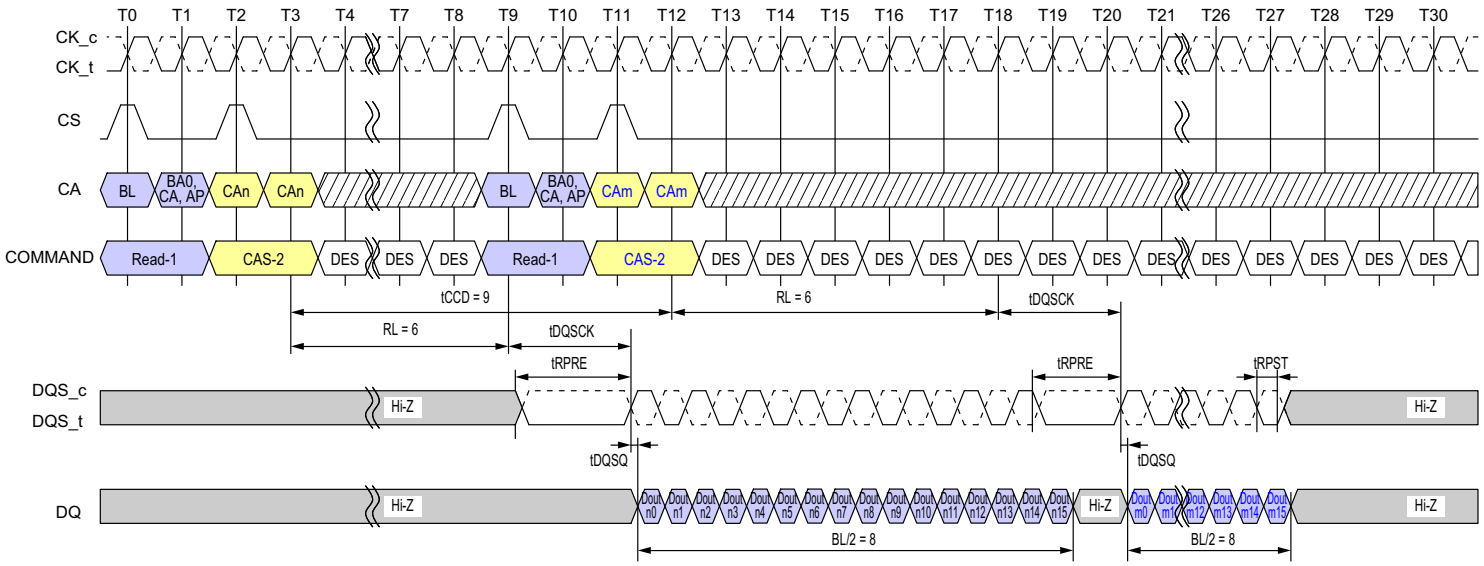

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 31 - Consecutive Reads Operation: tCCD=Min+1, Preamble=Toggle, 0.5nCK Postamble**



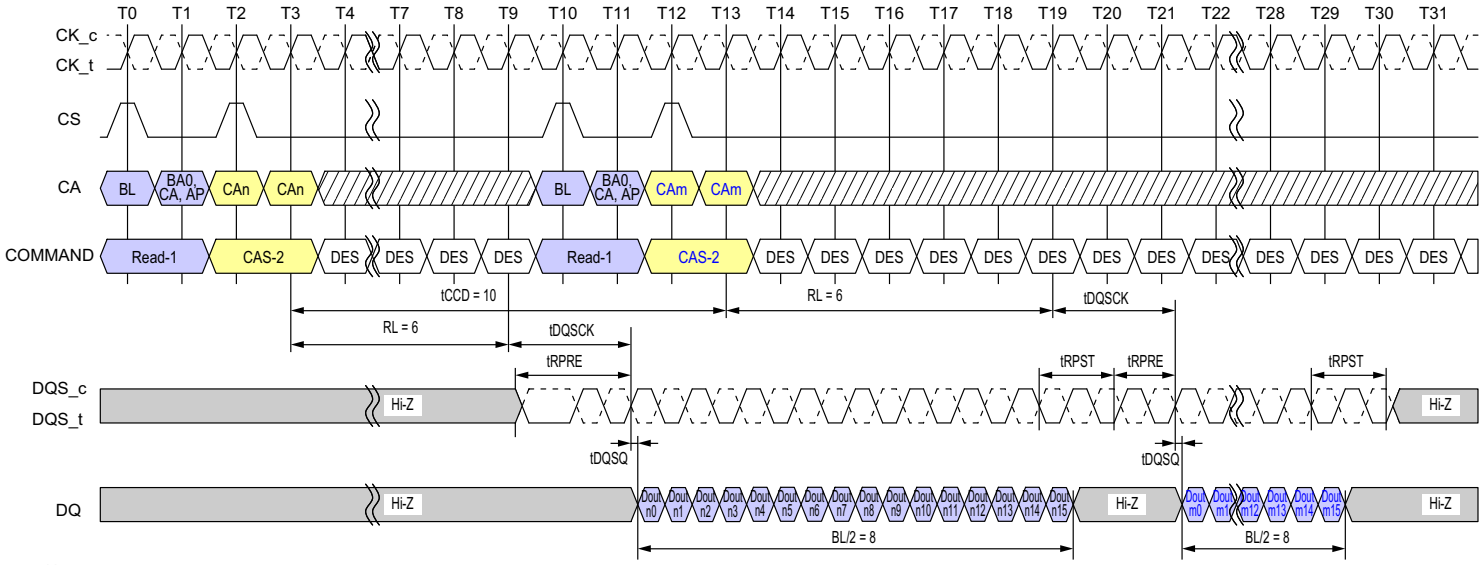

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 32 - Consecutive Reads Operation: tCCD = Min +1, Preamble = Static, 1.5nCK Postamble**



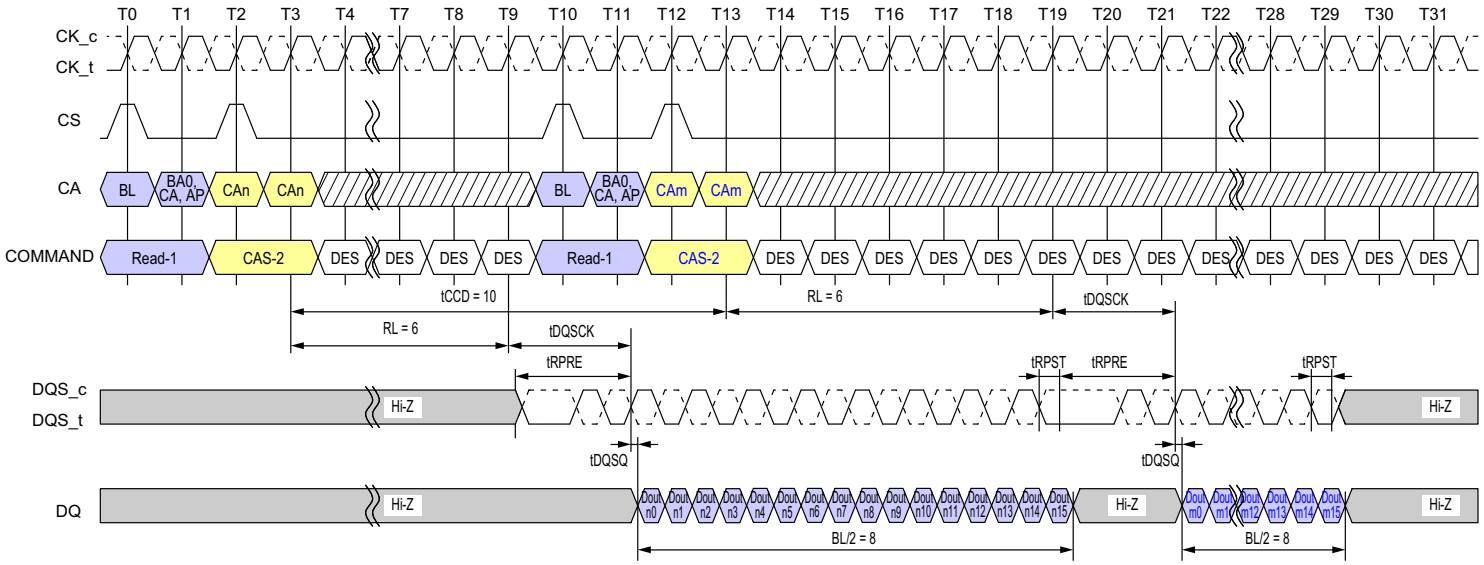

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 33 - Consecutive Reads Operation: tCCD = Min +1, Preamble = Static, 0.5nCK Postamble**



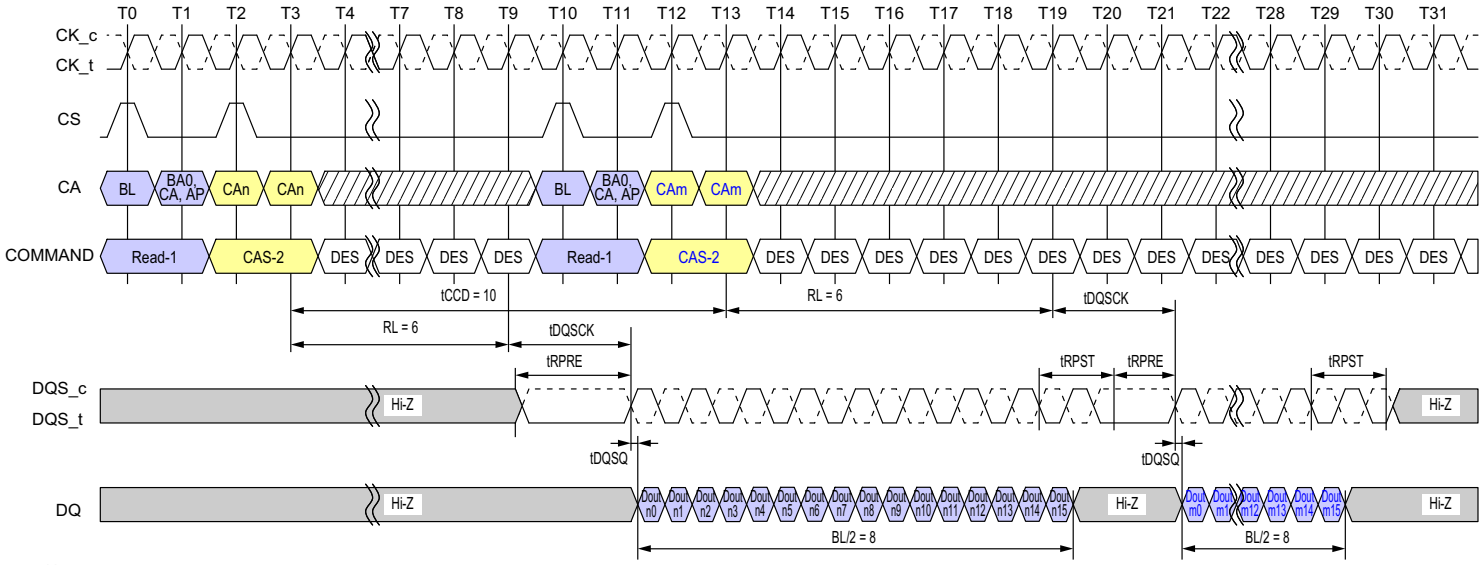

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 34 - Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 1.5nCK Postamble**



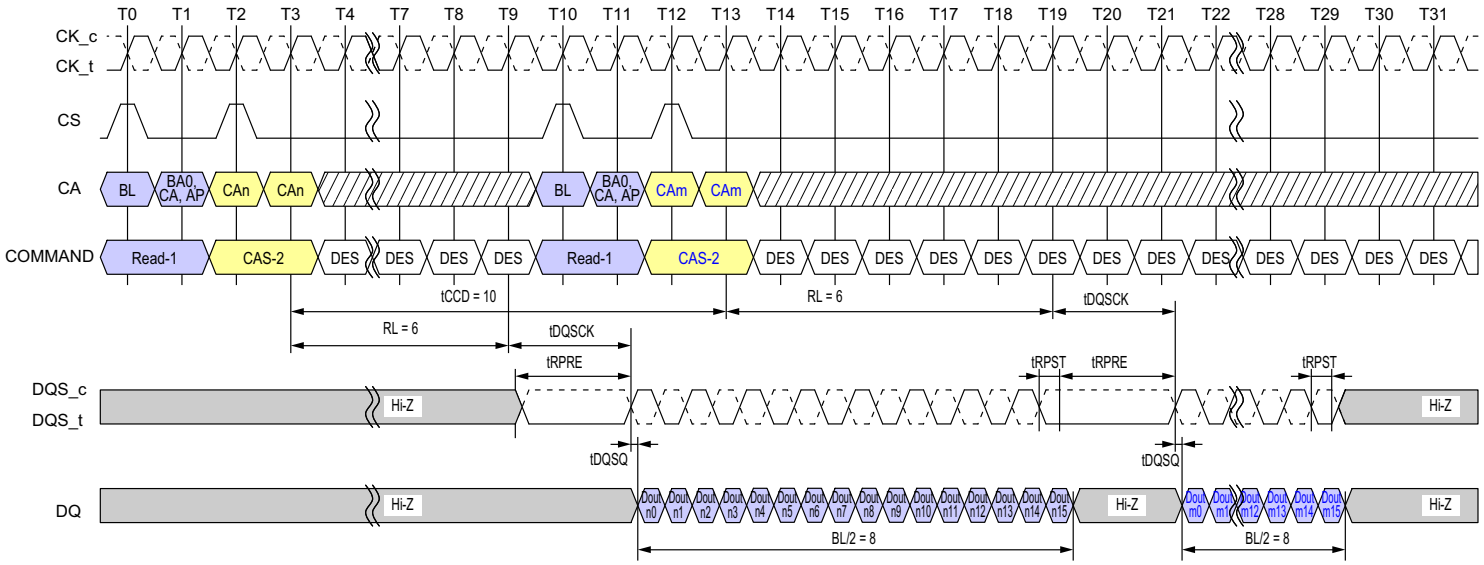

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 35 - Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 0.5nCK Postamble**



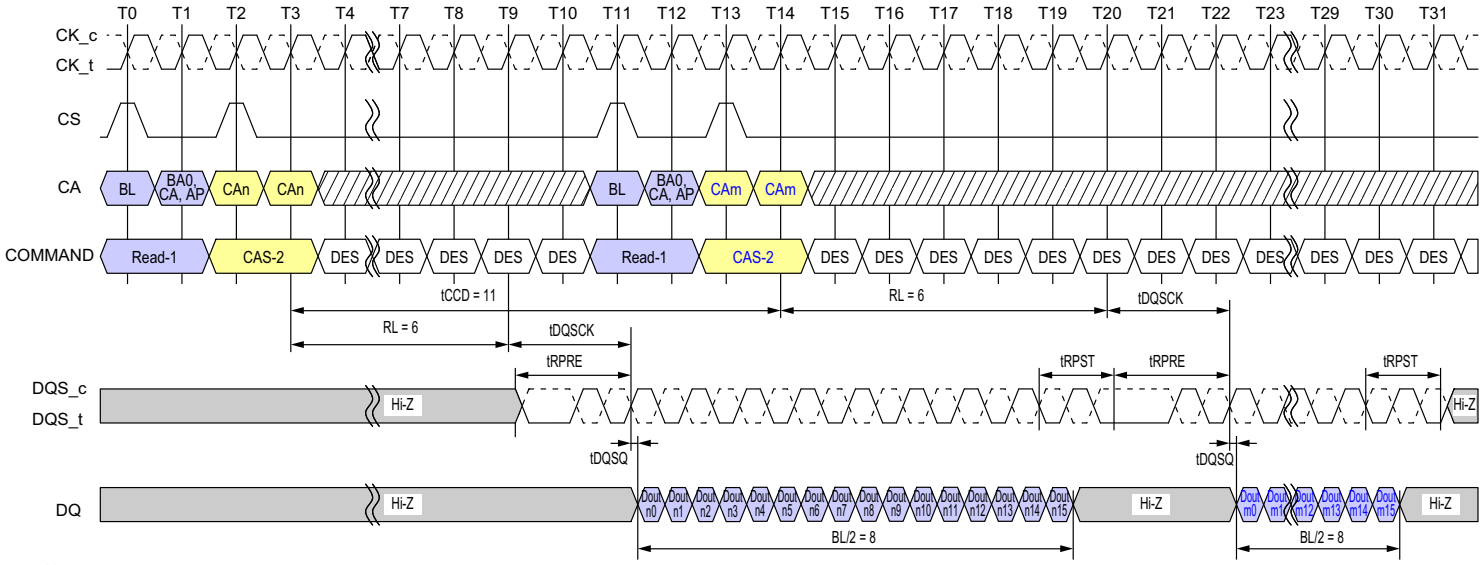

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 36 - Consecutive Reads Operation: tCCD = Min +2, Preamble = Static, 1.5nCK Postamble**



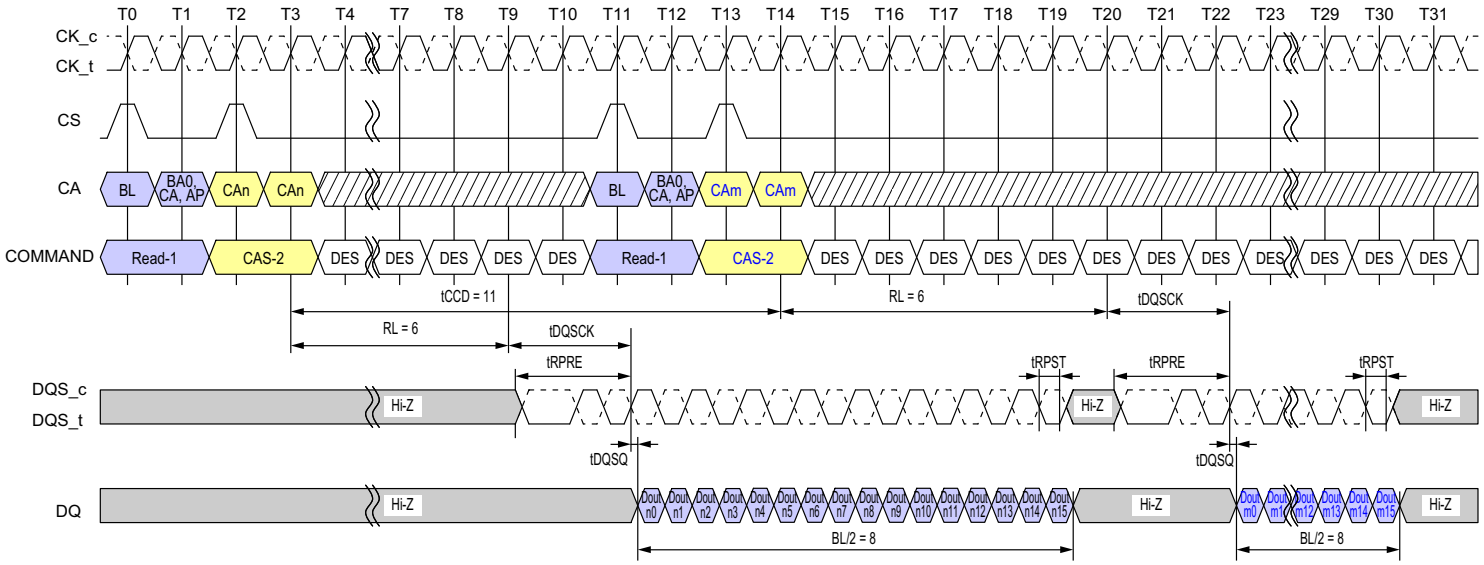

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 37 - Consecutive Reads Operation: tCCD = Min +2, Preamble = Static, 0.5nCK Postamble**



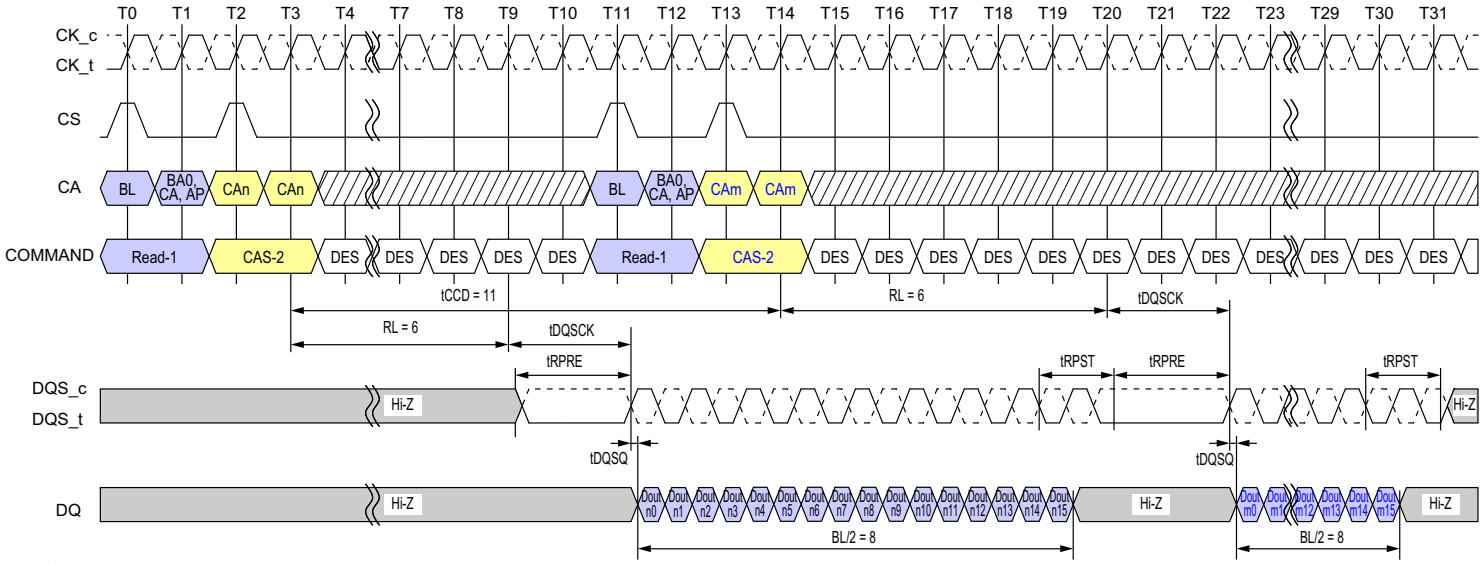

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 38 - Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 1.5nCK Postamble**



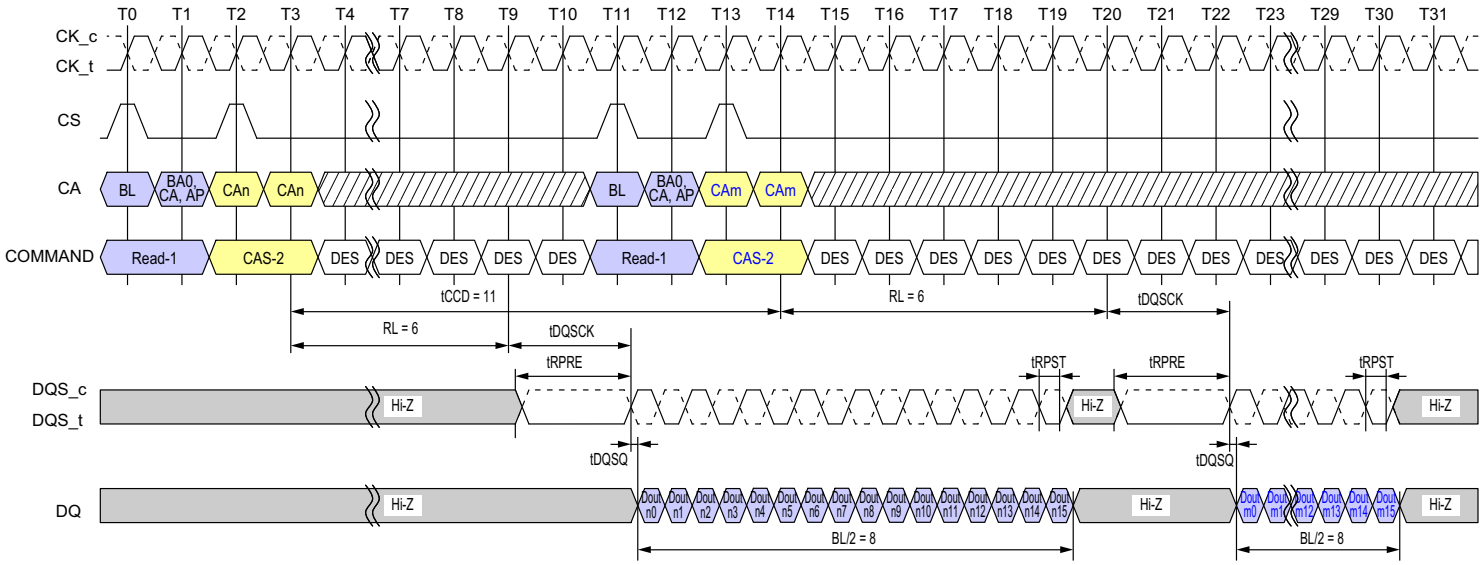

Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 39 - Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 0.5nCK Postamble**




Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

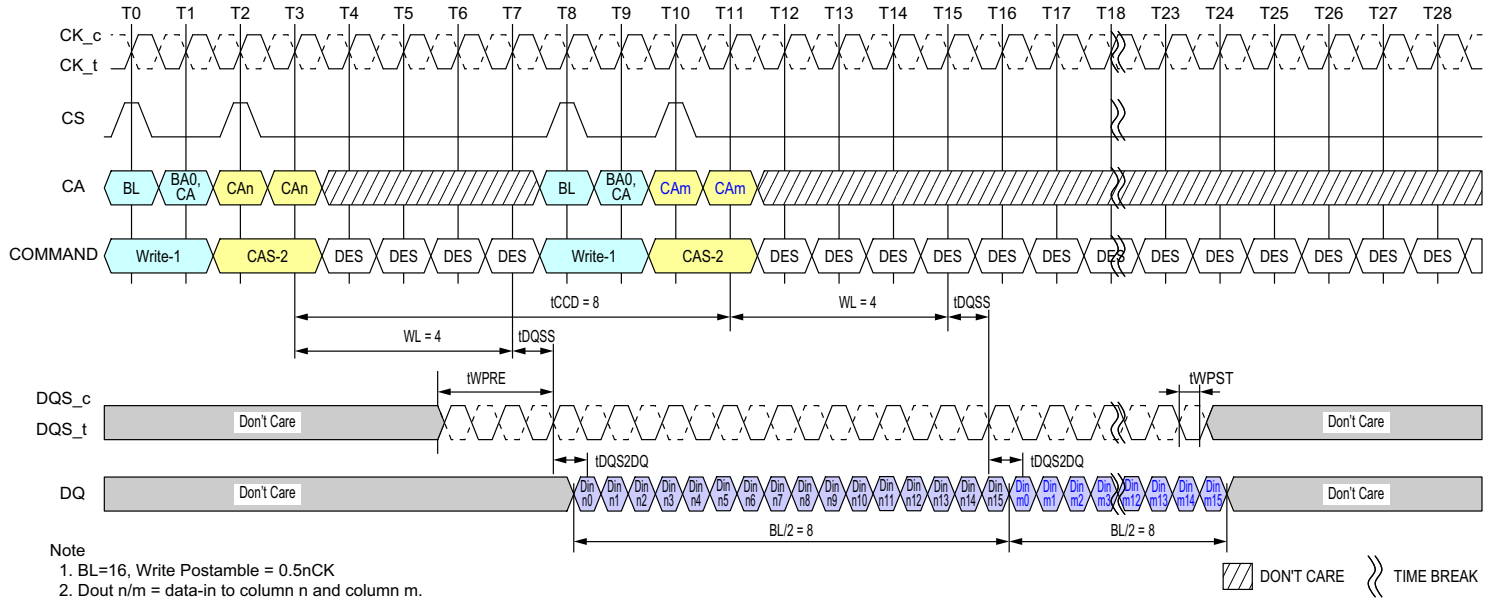
**Figure 40 - Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 1.5nCK Postamble**




Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

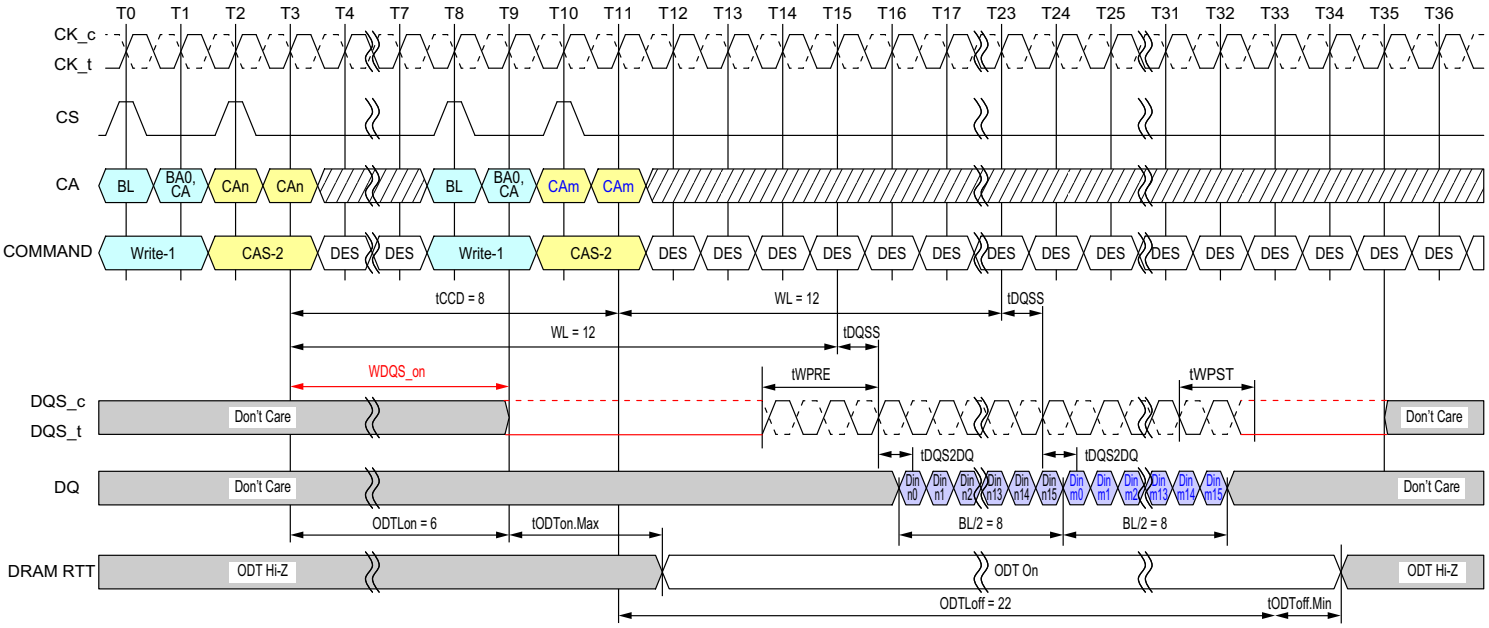
**Figure 41 - Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 0.5nCK Postamble**

### 2.14.2. Write to Write operation



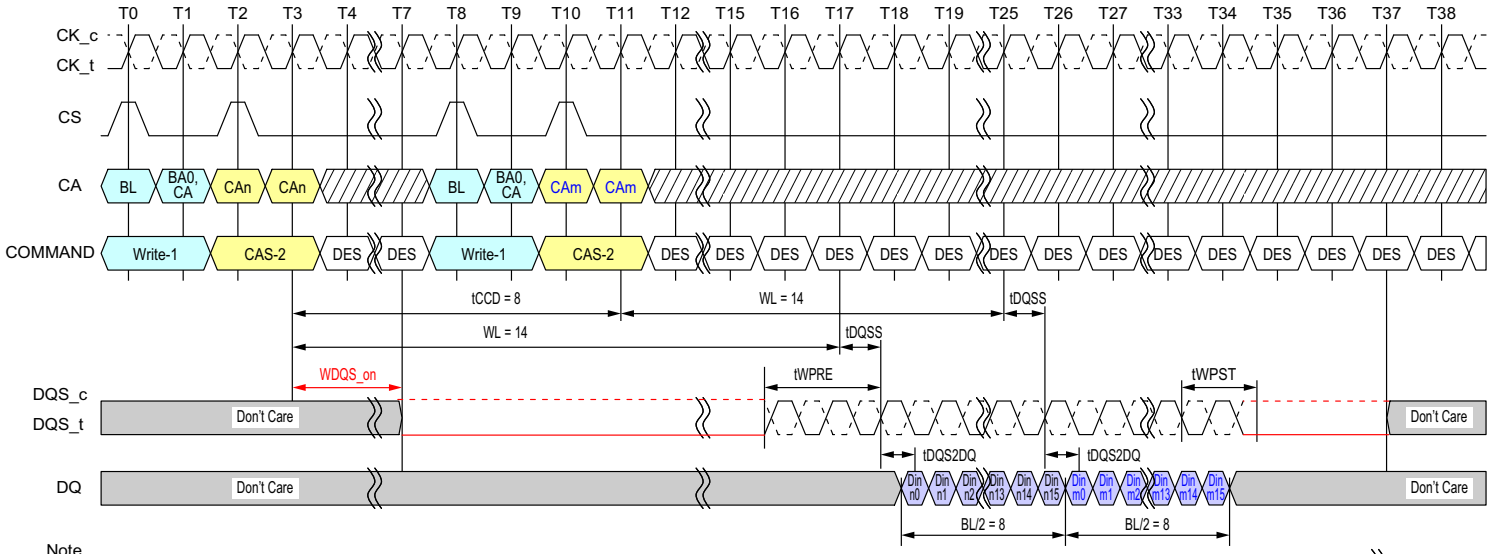

Note
1. BL=16, Write Postamble = 0.5nCK
2. Dout n/m = data-in to column n and column m.
3. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 42 - Seamless Writes Operation: tCCD = Min, 0.5nCK Postamble**



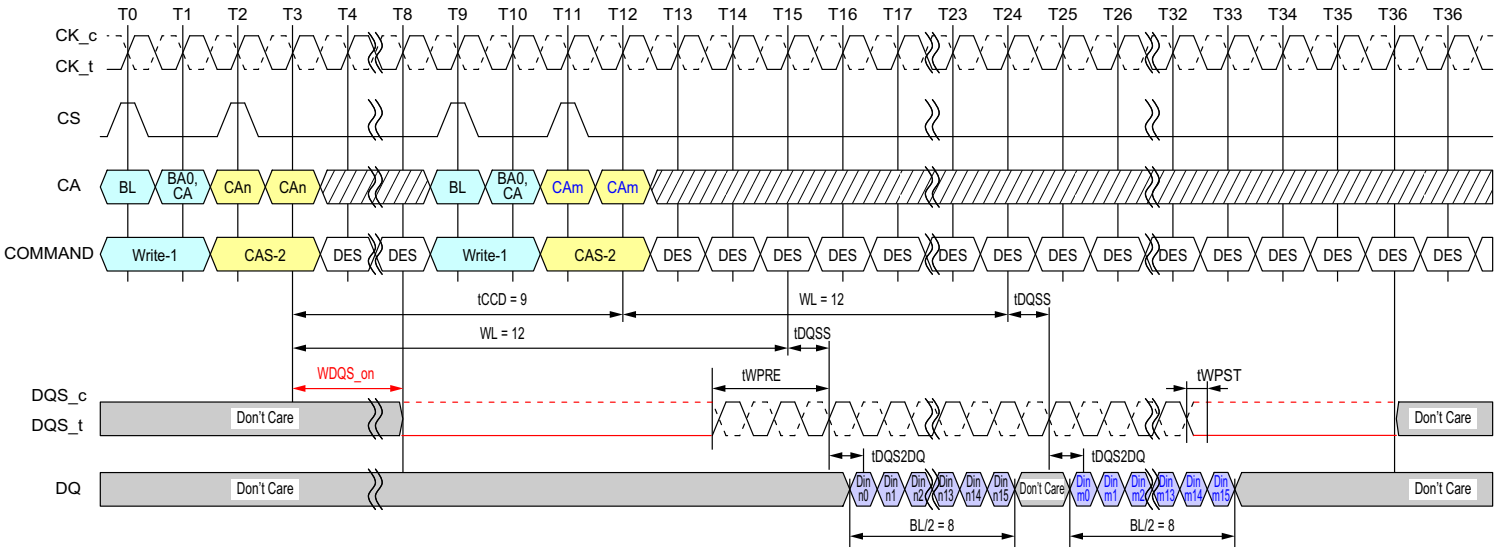

Note
1. Clock Frequency = 800MHz, tCK(AVG) = 1.25ns
2. BL=16, Write Postamble = 1.5nCK
3. Dout n/m = data-in to column n and column m.
3. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 43 - Seamless Writes Operation: tCCD = Min, 1.5nCK Postamble, 533MHz < Clock Freq. ≤ 800MHz, ODT Worst Timing Case**



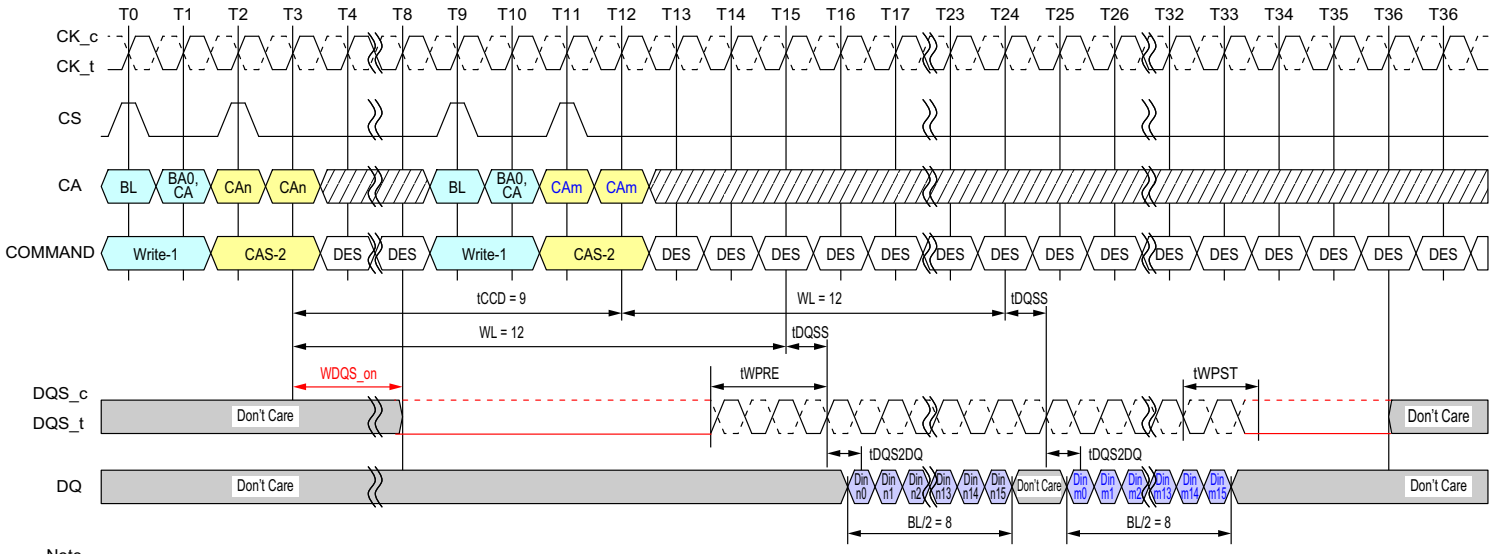

Note
1. BL=16, Write Postamble = 1.5nCK
2. Dout n/m = data-in to column n and column m.
3. The minimum number of clock cycles from the burst write command to the burst write command for any bank is BL/2
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 44 - Seamless Writes Operation: tCCD = Min, 1.5nCK Postamble**



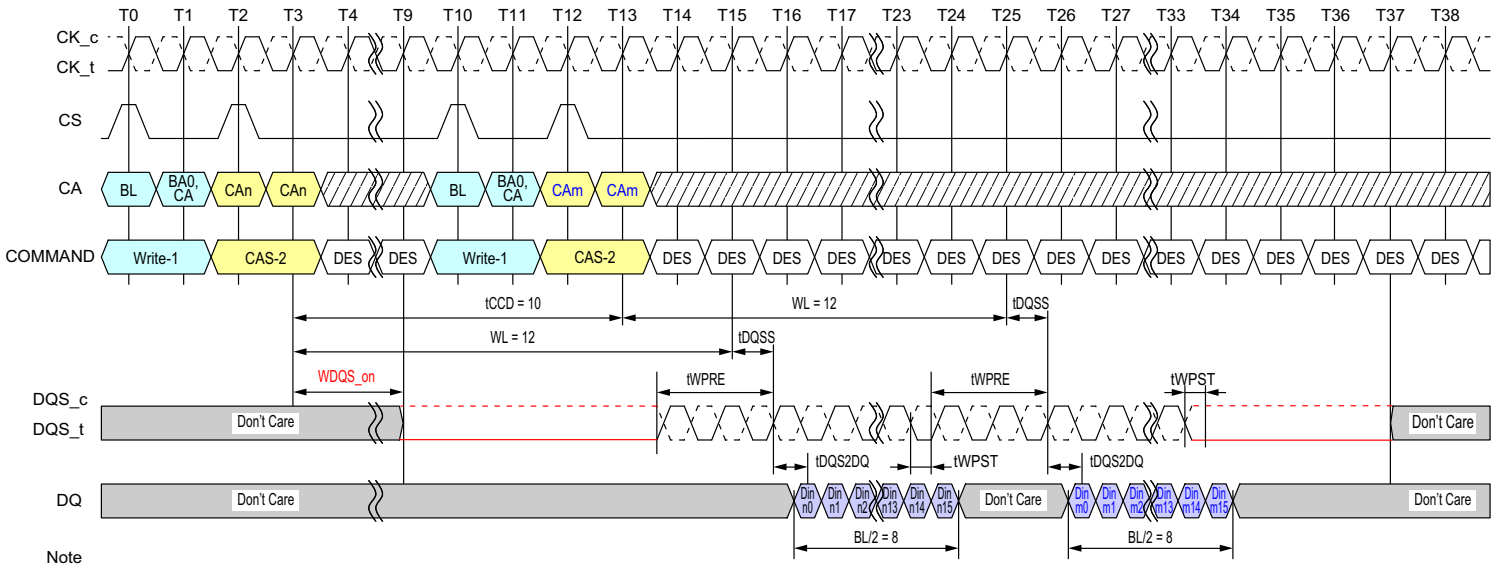

Note
1. BL=16, Write Postamble = 0.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 45 - Consecutive Writes Operation: tCCD = Min + 1, 0.5nCK Postamble**



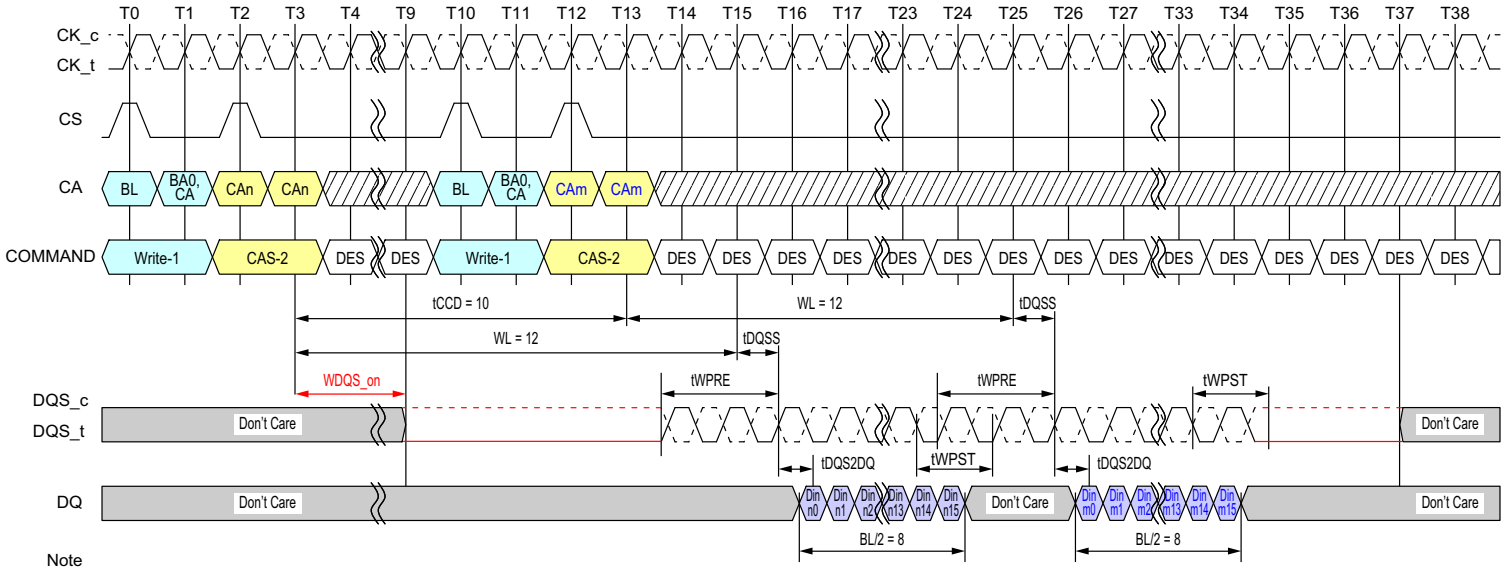

Note
1. BL=16, Write Postamble = 1.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 46 - Consecutive Writes Operation: tCCD = Min + 1, 1.5nCK Postamble**



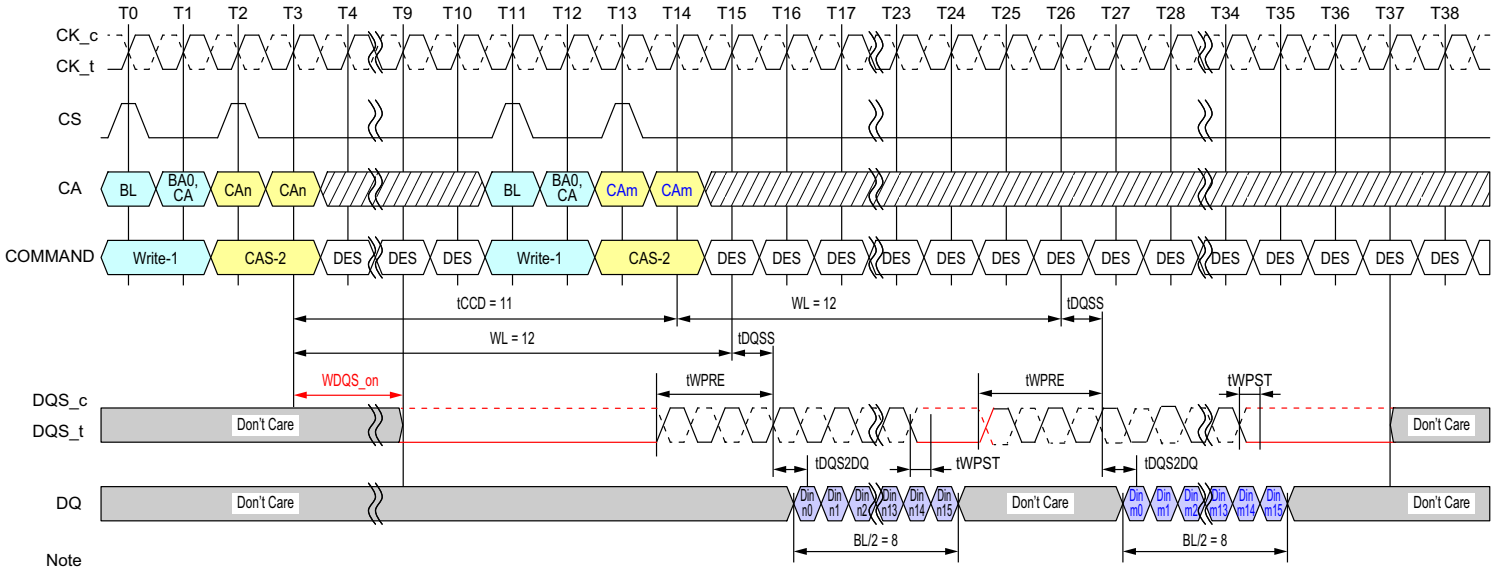

Note
1. BL=16, Write Postamble = 0.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 47 - Consecutive Writes Operation: tCCD = Min + 2, 0.5nCK Postamble**



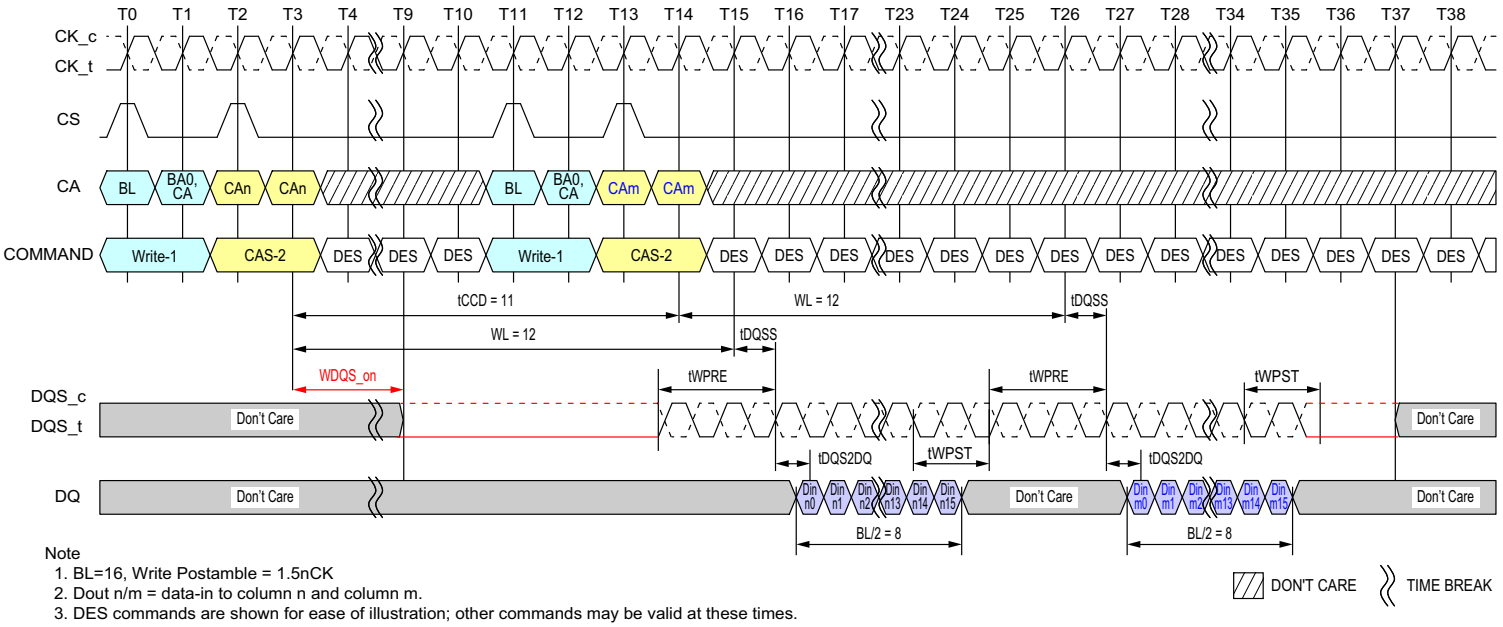

Note
1. BL=16, Write Postamble = 1.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 48 - Consecutive Writes Operation: tCCD = Min + 2, 1.5nCK Postamble**



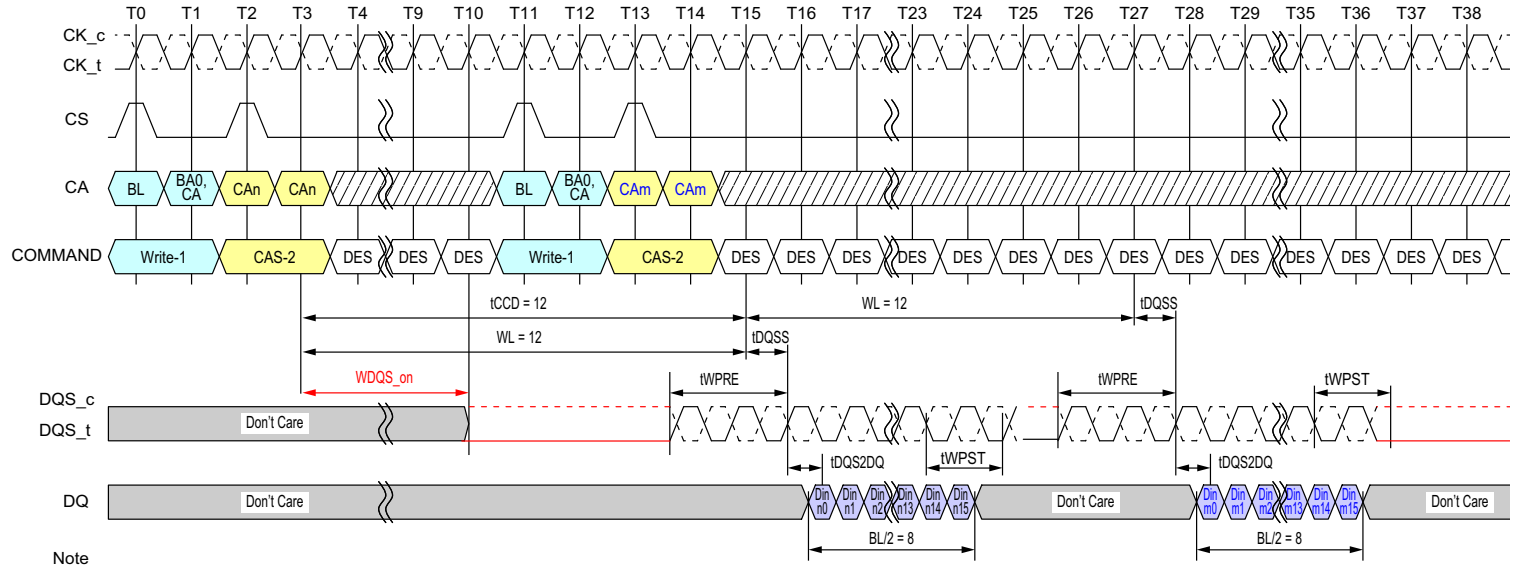

Note
1. BL=16, Write Postamble = 0.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 49 - Consecutive Writes Operation: tCCD = Min + 3, 0.5nCK Postamble**




Note
1. BL=16, Write Postamble = 1.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 50 - Consecutive Writes Operation: tCCD = Min + 3, 1.5nCK Postamble**

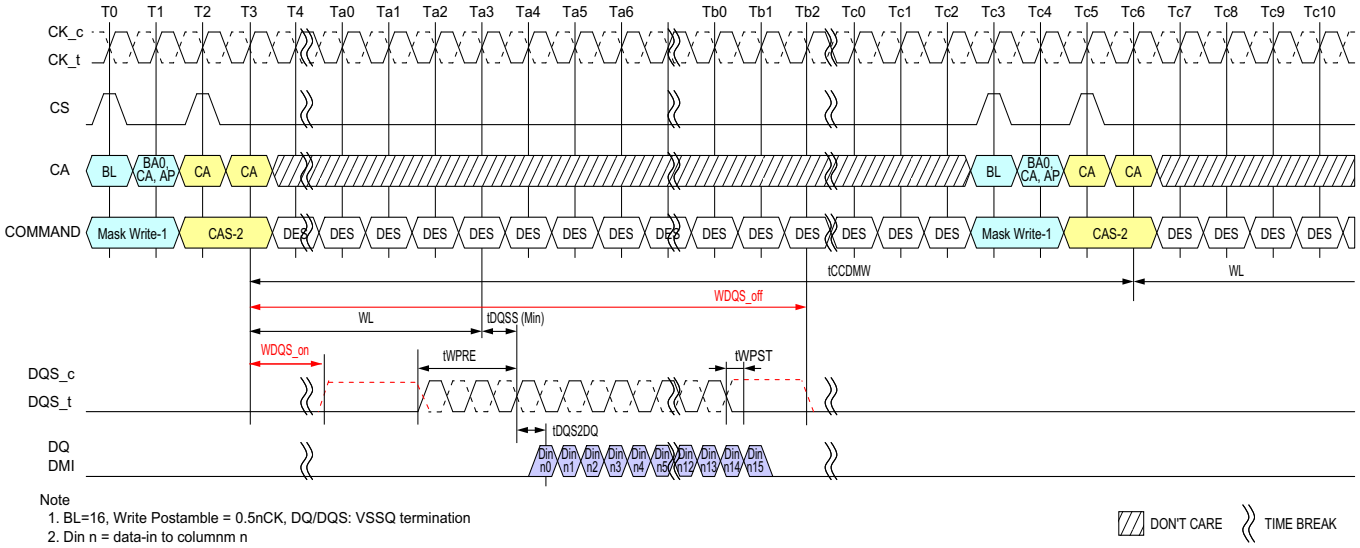



Note
1. BL=16, Write Postamble = 1.5nCK
2. Dout n/m = data-in to column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 51 - Consecutive Writes Operation: tCCD = Min + 4, 1.5nCK Postamble**

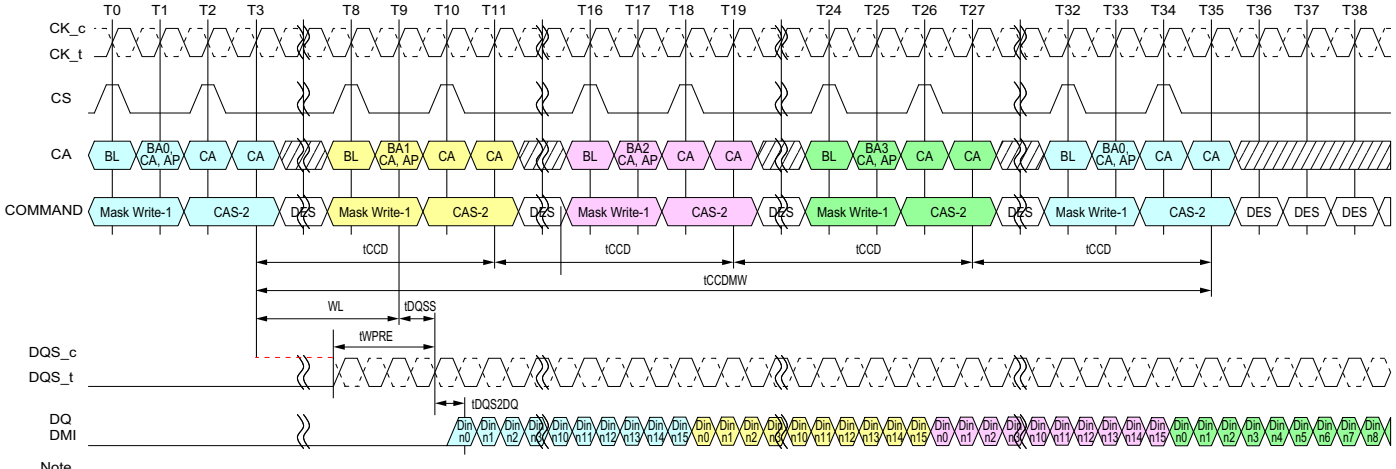
## 2.15. Masked Write Operation

The LPDDR4-SDRAM requires that Write operations which include a byte mask anywhere in the burst sequence must use the Masked Write command. This allows the DRAM to implement efficient data protection schemes based on larger data blocks. The Masked Write-1 command is used to begin the operation, followed by a CAS-2 command. A Masked Write command to the same bank cannot be issued until tCCDMW later, to allow the LPDDR4-SDRAM to finish the internal Read-Modify-Write. One Data Mask-Invert (DMI) pin is provided per byte lane, and the Data Mask-Invert timings match data bit (DQ) timing. See the section on "Data Mask Invert" for more information on the use of the DMI signal.




Note
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnm n
3. Mask-Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.
4. DES commands are shown for ease of illustration; other commands may be valid at these time.

**Figure 52 - Masked Write Command - Same Bank**




Note
1. BL=16, DQ/DQS/DMI: VSSQ termination
2. Din n = data-in to columnm n
3. Mask-Write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16 bit wide data for masked write operation.
4. DES commands are shown for ease of illustration; other commands may be valid at these time.

**Figure 53 - Masked Write Command - Different Bank**

### 2.15.1. Masked Write Timing constraints

**Table 31 - Masked Write Timing constraints - Same bank : DQ ODT is Disabled**

| Next CMD / Current CMD | Activate | Read (BL16 or 32) | Write (BL16 or 32) | Masked Write | Precharge |
|---|---|---|---|---|---|
| Active | illegal | RU(tRCD/tCK) | RU(tRCD/tCK) | RU(tRCD/tCK) | RU(tRAS/tCK) |
| Read with BL = 16 | illegal | 8[1)] | RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+RD(tRPST) | BL/2+max{(8,RU(tRTP/ tCK)}-8 |
| Read with BL = 32 | illegal | 16[2)] | RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/ tCK) +BL/2-WL+tWPRE+RD(tRPST) | BL/2+max{(8,RU(tRTP/ tCK)}-8 |
| Write with BL = 16 | illegal | WL+1+BL/2 +RU(tWTR/tCK) | 8[1)] | tCCDMW[3)] | WL+ 1 + BL/2+RU(tWR/ tCK) |
| Write with BL = 32 | illegal | WL+1+BL/2 +RU(tWTR/tCK) | 16[2)] | tCCDMW +8[4)] | WL+ 1 + BL/2+RU(tWR/ tCK) |
| Masked Write | illegal | WL+1+BL/2 +RU(tWTR/tCK) | tCCD | tCCDMW[3)] | WL+ 1 + BL/2 +RU(tWR/tCK) |
| Precharge | RU(tRP/tCK), RU(tRPab/tCK) | illegal | illegal | illegal | 4 |

Notes
1. In the case of BL = 16, tCCD is 8*tCK.
2. In the case of BL = 32, tCCD is 16*tCK.
3. tCCDMW = 32*tCK (4*tCCD at BL=16)
4. Write with BL=32 operation has 8*tCK longer than BL =16.
5. tRPST values depend on MR1-OP[7] respectively.

**Table 32 - Masked Write Timing constraints - Same bank : DQ ODT is Enabled**

| Next CMD / Current CMD | Activate | Read (BL16 or 32) | Write (BL16 or 32) | Masked Write | Precharge |
|---|---|---|---|---|---|
| Read with BL = 16 | illegal | 8[1)] | RL+RU(tDQSCK(max)/ tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/ tCK)+1 | RL+RU(tDQSCK(max)/ tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/ tCK)+1 | BL/2+max{(8,RU(tRTP/ tCK)}-8 |
| Read with BL = 32 | illegal | 16[2)] | RL+RU(tDQSCK(max)/ tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/ tCK)+1 | RL+RU(tDQSCK(max)/ tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/ tCK)+1 | BL/2+max{(8,RU(tRTP/ tCK)}-8 |

Notes
1. In the case of BL = 16, tCCD is 8*tCK.
2. In the case of BL = 32, tCCD is 16*tCK.
3. The rest of the timing is same as DQ ODT is Disable case
4. tRPST values depend on MR1-OP[7] respectively.

**Table 33 - Masked Write Timing constraints - Different bank : DQ ODT is Disabled**

| Next CMD<br>Current CMD | Activate | Read<br>(BL16 or 32) | Write<br>(BL16 or 32) | Masked Write<br>(BL16) | Precharge |
|---|---|---|---|---|---|
| Active | RU(tRRD/tCK) | 4 | 4 | 4 | 2 |
| Read with BL = 16 | 4 | 8[1)] | RL+RU(tDQSCK(max)/tCK)<br>+BL/2-<br>WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK)<br>+BL/2-<br>WL+tWPRE+RD(tRPST) | 2 |
| Read with BL = 32 | 4 | 16[2)] | RL+RU(tDQSCK(max)/tCK)<br>+BL/2-<br>WL+tWPRE+RD(tRPST) | RL+RU(tDQSCK(max)/tCK)<br>+BL/2-<br>WL+tWPRE+RD(tRPST) | 2 |
| Write with BL = 16 | 4 | WL+1+BL/2<br>+RU(tWTR/tCK) | 8[1)] | 8[1)] | 2 |
| Write with BL = 32 | 4 | WL+1+BL/2<br>+RU(tWTR/tCK) | 16[2)] | 16[2)] | 2 |
| Masked Write | 4 | WL+1+BL/2<br>+RU(tWTR/tCK) | 8[1)] | 8[1)] | 2 |
| Precharge | 4 | 4 | 4 | 4 | 4 |

Notes
1. In the case of BL = 16, tCCD is 8*tCK.
2. In the case of BL = 32, tCCD is 16*tCK.
3. tRPST values depend on MR1-OP[7] respectively

**Table 34 - Masked Write Timing constraints - Different bank : DQ ODT is Enabled**

| Next CMD<br>Current CMD | Activate | Read<br>(BL16 or 32) | Write<br>(BL16 or 32) | Masked Write<br>(BL16) | Precharge |
|---|---|---|---|---|---|
| Read with BL = 16 | 4 | 8[1)] | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | 2 |
| Read with BL = 32 | 4 | 16[2)] | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | 2 |

Notes
1. In the case of BL = 16, tCCD is 8*tCK.
2. In the case of BL = 32, tCCD is 16*tCK.
3. The rest of the timing is same as DQ ODT is Disable case
4. tRPST values depend on MR1-OP[7] respectively.

## 2.16. LPDDR4 Data Mask (DM) and Data Bus Inversion (DBIdc) Function

LPDDR4 SDRAM supports the function of Data Mask and Data Bus inversion. Details are as follows:.

- LPDDR4 device supports Data Mask (DM) function for Write operation.
- LPDDR4 device supports Data Bus Inversion (DBIdc) function for Write and Read operation.
- LPDDR4 supports DM and DBIdc function with a byte granularity.
- DBIdc function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBIdc function during Read can be enabled or disabled through MR3 OP[6].
- DM function during Masked Write can be enabled or disabled through MR13 OP[5].
- LPDDR4 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals per channel.
- DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

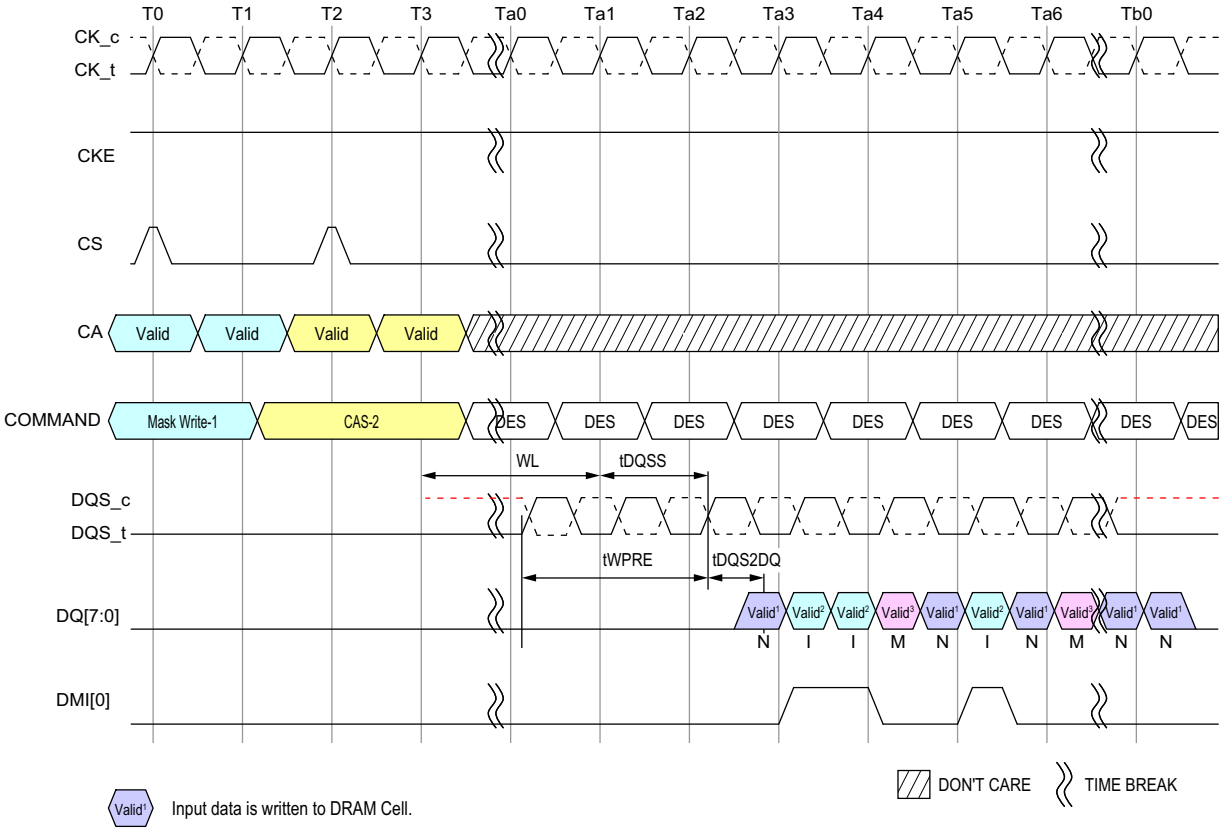
There are eight possible combinations for LPDDR4 device with DM and DBIdc function. Below table describes the functional behavior for all combinations.

**Table 35 - Function Behavior of DMI Signal During Write, Masked Write and Read Operation**

| DM Fuction | Write DBIdc Fuction | Read DBIdc Fuction | DMI Signal during Write Command | DMI Signal during Masked Write Command | DMI Signal during Read | DMI Signal during MPC [WR FIFO] | DMI Signal during MPC [RD FIFO] | DMI Signal during MPC [DQ Read calibration] | DMI Signal during MRR Command |
|---|---|---|---|---|---|---|---|---|---|
| Disable | Disable | Disable | Note: 1 | Note: 1, 3 | Note: 2 | Note: 1 | Note: 2 | Note: 2 | Note: 2 |
| Disable | Enable | Disable | Note: 4 | Note: 3 | Note: 2 | Note: 9 | Note: 10 | Note: 11 | Note: 2 |
| Disable | Disable | Enable | Note: 1 | Note: 3 | Note: 5 | Note: 9 | Note: 10 | Note: 11 | Note: 12 |
| Disable | Enable | Enable | Note: 4 | Note: 3 | Note: 5 | Note: 9 | Note: 10 | Note: 11 | Note: 12 |
| Enable | Disable | Disable | Note: 6 | Note: 7 | Note: 2 | Note: 9 | Note: 10 | Note: 11 | Note: 2 |
| Enable | Enable | Disable | Note: 4 | Note: 8 | Note: 2 | Note: 9 | Note: 10 | Note: 11 | Note: 2 |
| Enable | Disable | Enable | Note: 6 | Note: 7 | Note: 5 | Note: 9 | Note: 10 | Note: 11 | Note: 12 |
| Enable | Enable | Enable | Note: 4 | Note: 8 | Note: 5 | Note: 9 | Note: 10 | Note: 11 | Note: 12 |

Notes

1. DMI input signal is a don't care. DMI input receivers are turned OFF.
2. DMI output drivers are turned OFF.
3. Masked Write Command is not allowed and is considered an illegal command as DM function is disabled.
4. DMI signal is treated as DBI signal and it indicates whether DRAM needs to invert the Write data received on DQs within a byte. The LPDDR4 device inverts Write data received on the DQ inputs in case DMI was sampled HIGH, or leaves the Write data non-inverted in case DMI was sampled LOW.
5. The LPDDR4 DRAM inverts Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.
6. The LPDDR4 DRAM does not perform any mask operation when it receives Write command. During the Write burst associated with Write command, DMI signal must be driven LOW.
7. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. DMI signal is treated as DM signal and it indicates which bit time within the burst is to be masked. When DMI signal is HIGH, DRAM masks that bit time across all DQs associated within a byte. All DQ input signals within a byte are don't care (either HIGH or LOW) when DMI signal is HIGH. When DMI signal is LOW, the LPDDR4 DRAM does not perform mask operation and data received on DQ input is written to the array.
8. The LPDDR4 DRAM requires an explicit Masked Write command for all masked write operations. The LPDDR4 device masks the Write data received on the DQ inputs if the total count of '1' data bits on DQ[2:7] or DQ[10:15] (for Lower Byte or Upper Byte respectively) is equal to or greater than five and DMI signal is LOW. Otherwise the LPDDR4 DRAM does not perform mask operation and treats it as a legal DBI pattern; DMI signal is treated as DBI signal and data received on DQ input is written to the array.
9. DMI signal is treated as a training pattern. The LPDDR4 DRAM does not perform any mask operation and does not invert Write data received on the DQ inputs.
10. DMI signal is treated as a training pattern. The LPDDR4 DRAM returns DMI pattern written in WR FIFO.
11. DMI signal is treated as a training pattern. For more details, see 4.34, RD DQ Calibration.
12. DBI may apply or may not apply during normal MRR. It's vendor specific.
    If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DBI pin status should be low.
    If read DBI is enable with MRS and vendor can support the DBI during MRR, the LPDDR4 DRAM inverts Mode Register Read data on its DQ outputs associated within a byte and drives DMI signal HIGH when the number of '1' data bits within a given byte lane is greater than four; otherwise the DRAM does not invert the read data and drives DMI signal LOW.



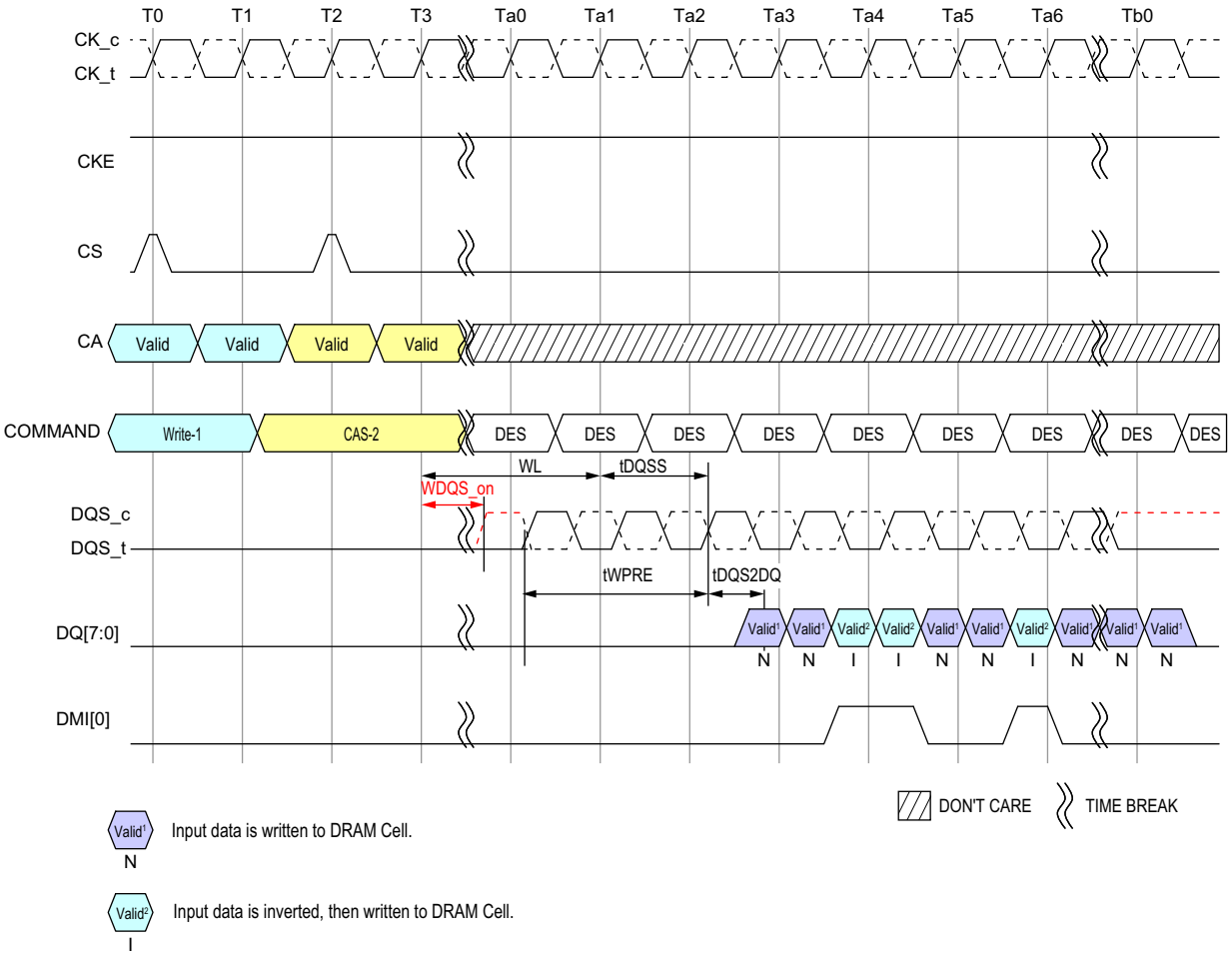

Valid[1] N — Input data is written to DRAM Cell.

Valid[2] I — Input data is inverted, then written to DRAM Cell.

Valid[3] M — Input data is masked. The total count of '1' data bits on DQ[2:7] is equal to or greater than five.

NOTES : 1. Data Mask (DM) is Enable: MR13 OP [5] = 0, Data BUS Inversion (DBI) Write is Enable: MR3 OP[7] = 1

**Figure 54 - Masked Write Command w/ Write DBI Enabled; DM Enabled**




NOTES : 1. Data Mask (DM) is Disable: MR13 OP [5] = 1, Data BUS Inversion (DBI) Write is Enable: MR3 OP[7] = 1

**Figure 55 - Write Command w/ Write DBI Enabled; DM Disabled**

## 2.17. Precharge Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS, and CA[5:0] in the proper state as defined by the Command Truth Table. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

To ensure that LPDDR4 devices can meet the instantaneous current demands, the row-precharge time for an all bank PRECHARGE (tRPab) is longer than the per bank precharge time (tRPpb).

**Table 36 - Precharge Bank Selection**

| AB (CA[5], R1) | BA2 (CA[2], R2) | BA1 (CA[1], R2) | BA0 (CA[0], R2) | Precharged Bank(s) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Bank 0 Only |
| 0 | 0 | 0 | 1 | Bank 1 Only |
| 0 | 0 | 1 | 0 | Bank 2 Only |
| 0 | 0 | 1 | 1 | Bank 3 Only |
| 0 | 1 | 0 | 0 | Bank 4 Only |
| 0 | 1 | 0 | 1 | Bank 5 Only |
| 0 | 1 | 1 | 0 | Bank 6 Only |
| 0 | 1 | 1 | 1 | Bank 7 Only |
| 1 | Valid | Valid | Valid | All banks |

### 2.17.1. Burst Read Operation followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but PRECHARGE cannot be issued until after tRAS is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row PRECHARGE time (tRP) has elapsed. The minimum READ-to-PRECHARGE time must also satisfy a minimum analog time from the 2nd rising clock edge of the CAS-2 command. tRTP begins BL/2 - 8 clock cycles after the READ command. For LPDDR4 READ-to-PRECHARGE timings see Table "Timing Between Commands (Precharge and Auto-Precharge)".

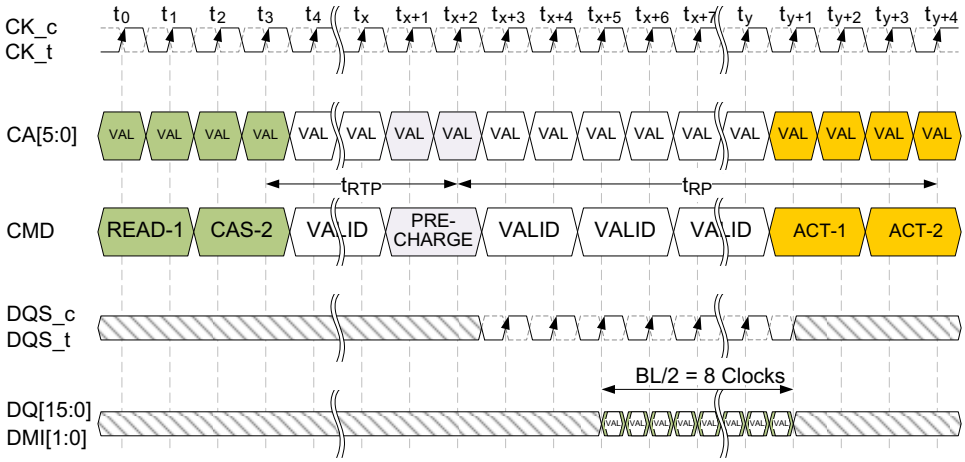



**Figure 56 - Burst Read followed by Precharge (Shown with BL16, 2tCK pre-amble)**

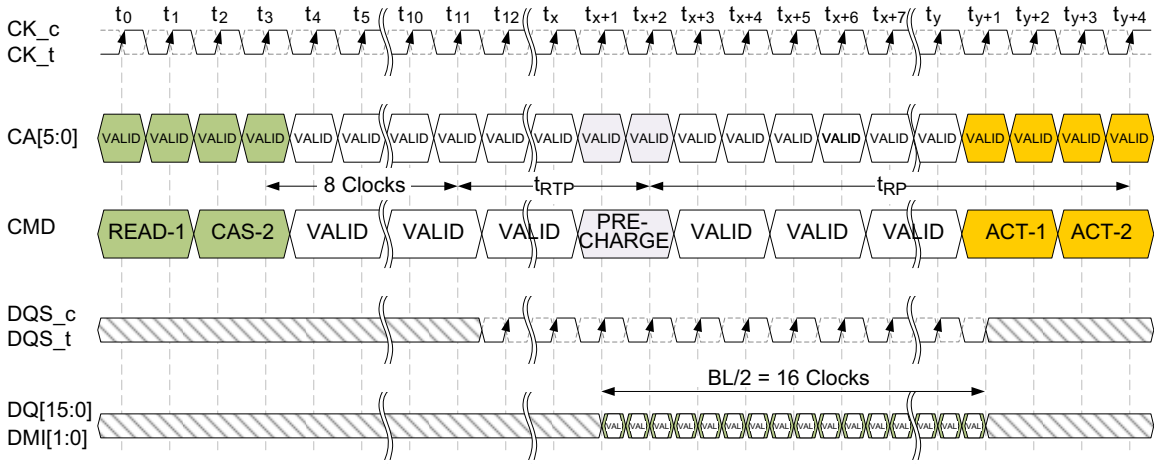



**Figure 57 - Burst Read followed by Precharge (Shown with BL32, 2tCK Preamble)**

### 2.17.2. Burst Write followed by Precharge

A Write Recovery time (tWR) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK_t after the last latching DQS clock of the burst.

LPDDR4-SDRAM devices write data to the memory array in prefetch multiples (prefetch=16). An internal WRITE operation can only begin after a prefetch group has been clocked, so tWR starts at the prefetch boundaries. The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles.

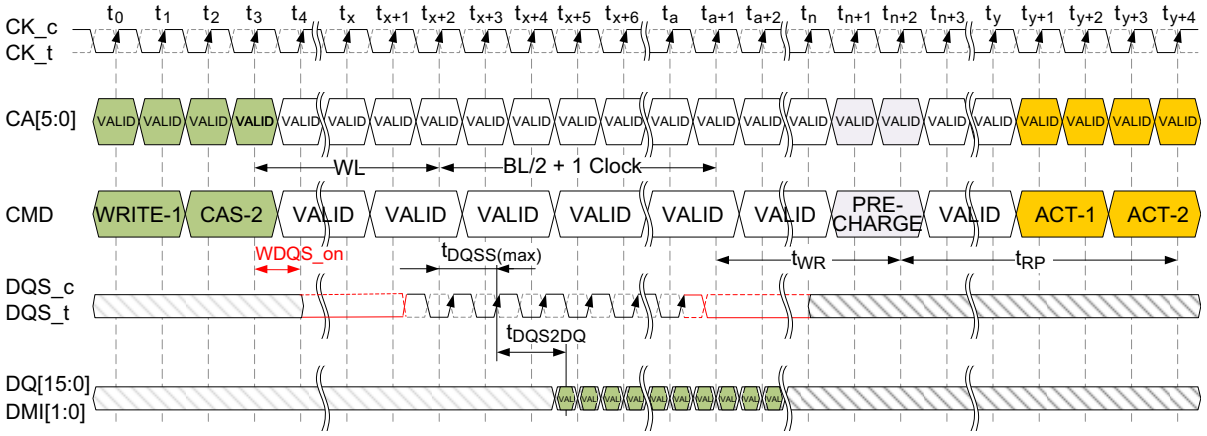



**Figure 58 - Burst Write followed by Precharge (Shown with BL16, 2tCK preamble)**

### 2.17.3. Scaling Parameters

To enable DRAM manufacturers to use advanced process nodes for LPDDR4, some scaling of timing parameters may be required. The primary timing parameter impacted by DRAM scaling is currently tWR, although other parameters may be affected.

**Table 37 - LPDDR4 Scaling Parameters Definition**

| Scaling Level | Parameter Value(s) |
|---|---|
| 0 | Default LPDDR4/LPDDR4X<br>tWR = 18ns |
| 1 | tWR default + 16ns (34ns) |
| 2 | RFU |
| 3 | RFU |

The requirement for a device to be operated using scaling parameters is indicated by read-only MR26 OP[1:0] (Table 75). When SCL is set to other than 0, the memory controller must adjust SDRAM timing parameters according to Table 111. When SCL is set to 0 no adjustment of timing parameters is required.

### 2.17.4. Auto Precharge operation

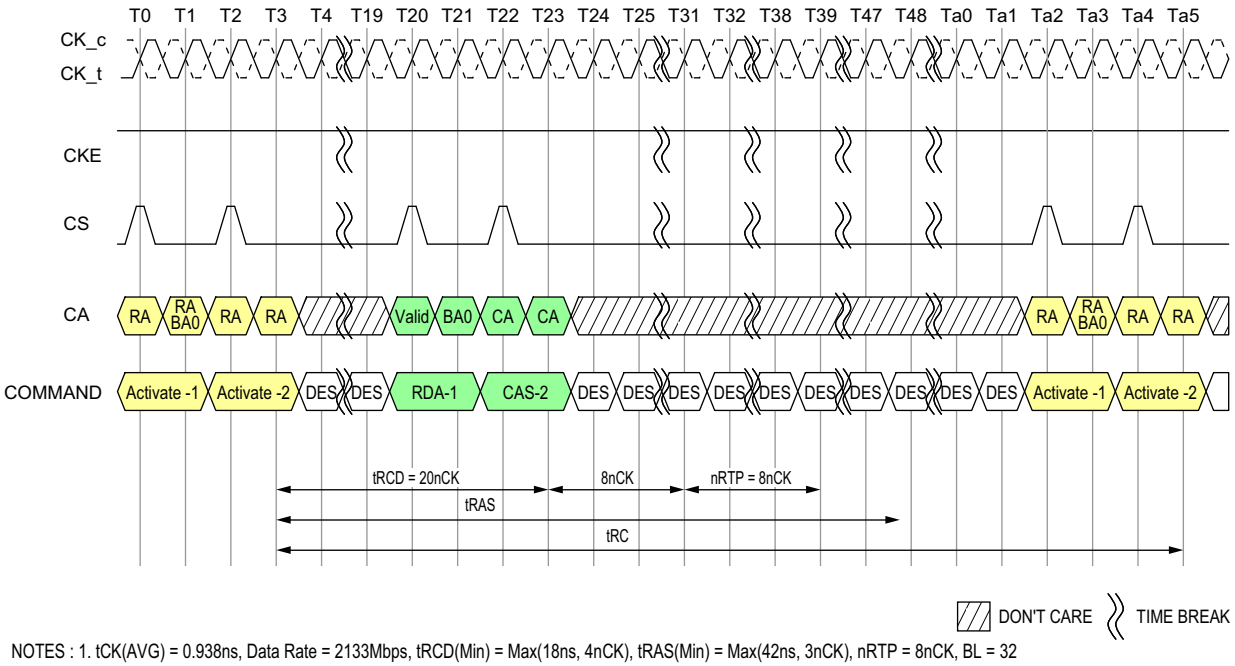
Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the Auto-Precharge function. When a READ, a WRITE or Masked Write command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ, WRITE or Masked Write cycle.

If AP is LOW when the READ or WRITE command is issued, then the normal READ, WRITE or Masked Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the READ, WRITE or Masked Write command is issued, the Auto-Precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Read with Auto-Precharge or Write/Mask Write with Auto-Precharge commands may be issued after tRCD has been satisfied. The LPDDR4 SDRAM RAS Lockout feature will schedule the internal precharge to assure that tRAS is satisfied.

tRC needs to be satisfied prior to issuing subsequent Activate commands to the same bank.
Below Figure shows example of RAS lock function.




NOTES : 1. tCK(AVG) = 0.938ns, Data Rate = 2133Mbps, tRCD(Min) = Max(18ns, 4nCK), tRAS(Min) = Max(42ns, 3nCK), nRTP = 8nCK, BL = 32
2. tRCD = 20nCK comes from Roundup(18ns/0.938ns)
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 59 - Command Input Timing with RAS lock**

### 2.17.5. Burst Read with Auto-Precharge

If AP is HIGH when a READ command is issued, the READ with Auto-Precharge function is engaged. An internal precharge procedure starts a following delay time after the READ command. And this delay time depends on BL setting.

BL = 16: nRTP
BL = 32: 8nCK + nRTP

For LPDDR4 Auto-Precharge calculations, see Table 38. Following an Auto-Precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

a. The RAS precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge began, or
b. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

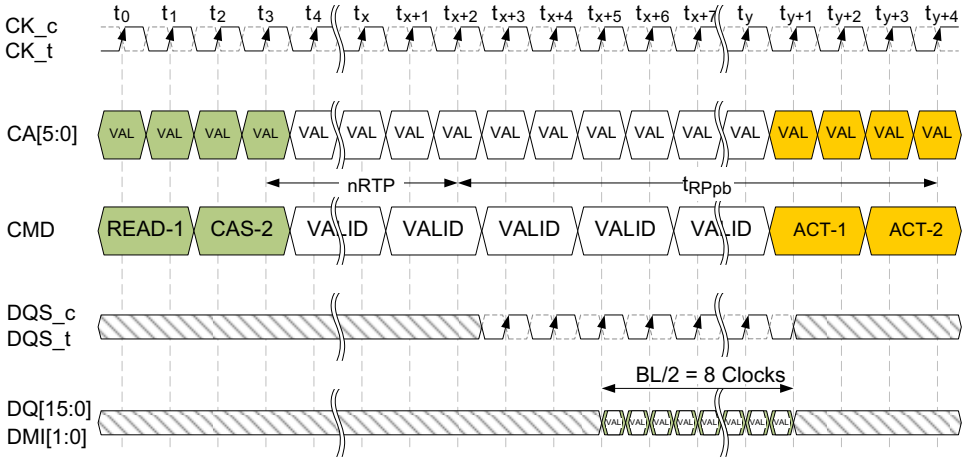



**Figure 60 - Burst Read with Auto-Precharge (Shown with BL16, 2tCK preamble)**

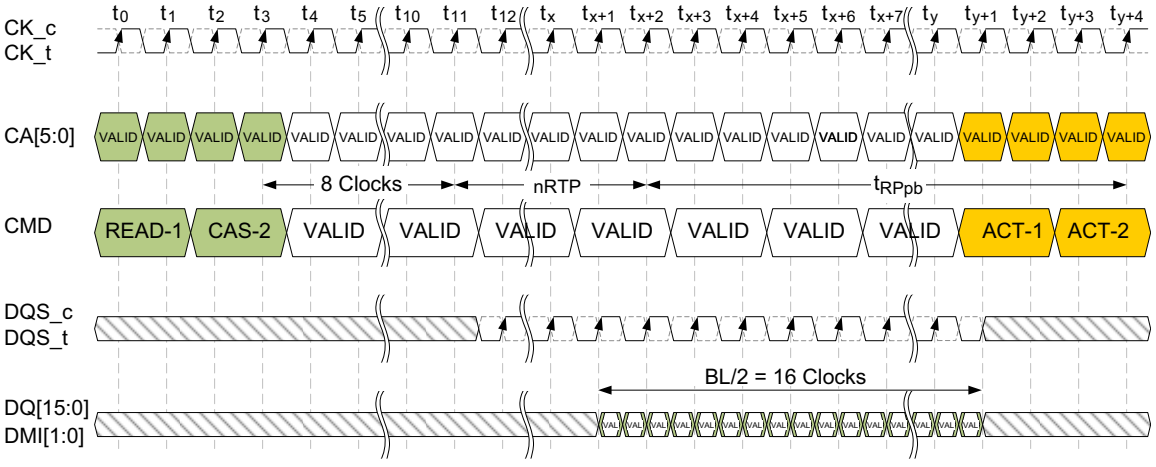



**Figure 61 - Burst Read with Auto-Precharge (Shown with BL32, 2tCK preamble)**

### 2.17.6. Burst Write with Auto-Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with Auto-Precharge function is engaged. The device starts an Auto-Precharge on the rising edge tWR cycles after the completion of the Burst WRITE.

Following a WRITE with Auto-Precharge, an ACTIVATE command can be issued to the same bank if the following conditions are met:

a. The RAS precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge began, and

b. The RAS cycle time (tRC) from the previous bank activation has been satisfied.

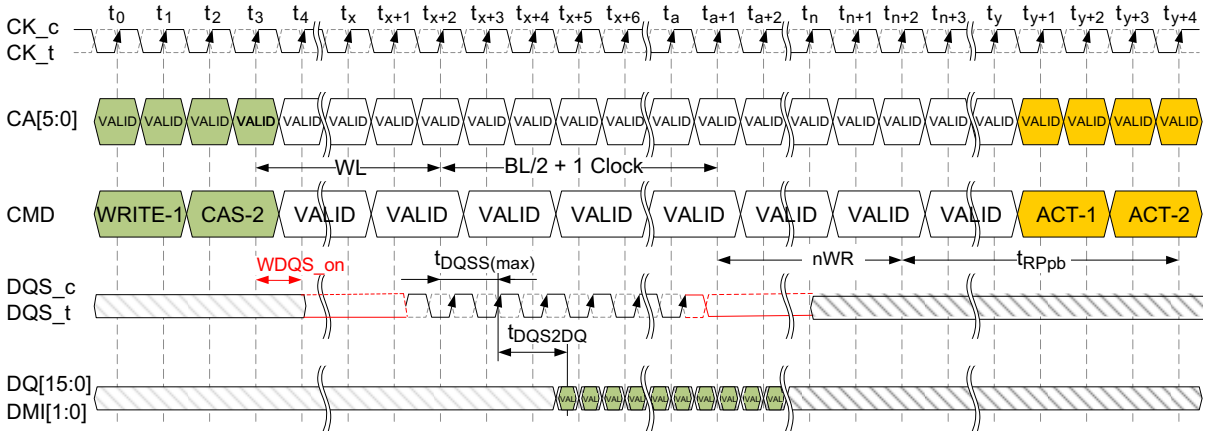



**Figure 62 - Burst Write with Auto-Precharge (Shown with BL16, 2tCK preamble)**

### 2.17.7. Delay Time from Write to Read with Auto Precharge

In the case of write command followed by read with Auto-Precharge, controller must satisfy tWR for the write command before initiating the DRAM internal Auto-Precharge. It means that (tWTR + nRTP) should be equal or longer than (tWR) when BL setting is 16, as well as (tWTR + nRTP +8nCK) should be equal or longer than (tWR) when BL setting is 32. Refer to the following figure for details.

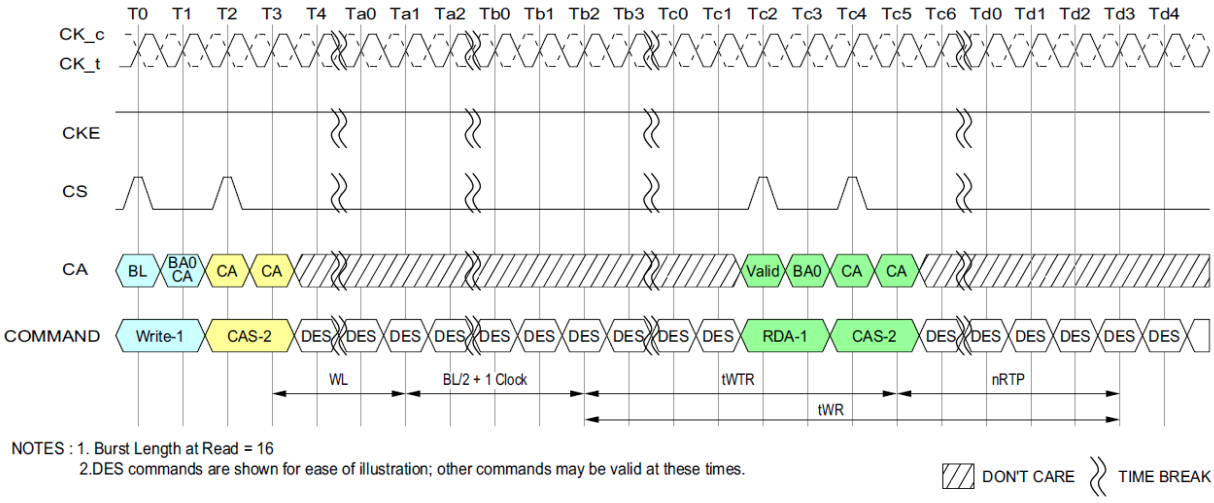



**Figure 63 - Delay time from Write to Read with Auto-Precharge**

**Table 38 - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Disabled**

| From Command | To Command | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|---|---|---|---|---|
| Read (BL16) | Precharge (to same bank as Read) | tRTP | tCK | 1,6 |
| | Precharge All | tRTP | tCK | 1,6 |
| Read (BL32) | Precharge (to same bank as Read) | 8*tCK + tRTP | tCK | 1,6 |
| | Precharge All | 8*tCK + tRTP | tCK | 1,6 |
| Read w/ AP (BL16) | Precharge (to same bank as Read w/ AP) | nRTP | tCK | 1,10 |
| | Precharge All | nRTP | tCK | 1,10 |
| | Activate (to same bank as Read w/ AP) | nRTP + tRPpb | tCK | 1,8,10 |
| | Write or Write w/ AP (same bank) | Illegal | - | 3 |
| | Masked Write or Masked Write w/ AP (same bank) | Illegal | - | |
| | Write or Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE | tCK | 3,4,5 |
| | Masked Write or Masked Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE | tCK | 3,4,5 |
| Read w/ AP (BL16) | Read or Read w/ AP (same bank) | Illegal | - | |
| | Read or Read w/ AP (different bank) | BL/2 | tCK | 3 |
| Read w/ AP (BL32) | Precharge (to same bank as Read w/ AP) | 8*tCK + nRTP | tCK | 1,10 |
| | Precharge All | 8*tCK + nRTP | tCK | 1,10 |
| | Activate (to same bank as Read w/ AP) | 8*tCK + nRTP + tRPpb | tCK | 1,8,10 |
| | Write or Write w/ AP (same bank) | Illegal | - | |
| | Masked Write or Masked Write w/ AP (same bank) | Illegal | - | |
| | Write or Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE | tCK | 3,4,5 |
| | Masked Write or Masked Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE | tCK | 3,4,5 |
| | Read or Read w/ AP (same bank) | Illegal | - | |
| | Read or Read w/ AP (different bank) | BL/2 | tCK | 3 |
| Write (BL16 & BL32) | Precharge (to same bank as Masked Write) | WL + BL/2 + tWR + 1 | tCK | 1,7 |
| | Precharge All | WL + BL/2 + tWR + 1 | tCK | 1,7 |

| From Command | To Command | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|---|---|---|---|---|
| Masked Write (BL16) | Precharge (to same bank as Masked Write) | WL + BL/2 + tWR + 1 | tCK | 1,7 |
| | Precharge All | WL + BL/2 + tWR + 1 | tCK | 1,7 |
| Write w/ AP (BL16 & BL32) | Precharge (to same bank as Write w/ AP) | WL + BL/2 + nWR + 1 | tCK | 1,11 |
| | Precharge All | WL + BL/2 + nWR + 1 | tCK | 1,11 |
| | Activate (to same bank as Write w/ AP) | WL + BL/2 + nWR + 1 + tRPpb | tCK | 1,8,11 |
| | Write or Write w/ AP (same bank) | Illegal | - | |
| | Write or Write w/ AP (different bank) | BL/2 | tCK | 3 |
| | Masked-Write or Masked-Write w/ AP (different bank) | BL/2 | tCK | 3 |
| | Read or Read w/ AP (same bank) | Illegal | - | |
| | Read or Read w/ AP (different bank) | WL + BL/2 + tWTR + 1 | tCK | 3,9 |
| Masked Write w/ AP (BL16) | Precharge (to same bank as Masked Write w/ AP) | WL + BL/2 + nWR + 1 | tCK | 1,11 |
| | Precharge all | WL + BL/2 + nWR + 1 | tCK | 1,11 |
| | Activate (to same bank as Masked Write w/ AP) | WL + BL/2 + nWR + 1 + tRPpb | tCK | 1,8,11 |
| | Write or Write w/ AP (same bank) | Illegal | - | |
| | Masked Write or Masked Write w/ AP (same bank) | Illegal | - | |
| | Write or Write w/ AP (different bank) | BL/2 | tCK | 3 |
| | Masked Write or Masked Write w/ AP (differenet bank) | BL/2 | tCK | 3 |
| | Read or Read w/ AP (same bank) | Illegal | - | |
| | Read or Read w/ AP (different bank) | WL + BL/2 + tWTR + 1 | tCK | 3,9 |
| Precharge | Precharge (to same bank as Precharge) | 4 | tCK | 1 |
| | Precharge All | 4 | tCK | 1 |
| Precharge All | Precharge | 4 | tCK | 1 |
| | Precharge All | 4 | tCK | 1 |

Notes

1. For a given bank, the precharge period should be counted from the latest precharge command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied tRP after that latest precharge command.
2. Any command issued during the minimum delay time as specified in the table above is illegal.
3. After READ w/AP, seamless read operations to different banks are supported. After WRITE w/AP or Masked Write w/AP, seamless write operations to different banks are supported. READ, WRITE, and Masked Write operations may not be truncated or interrupted.
4. tRPST values depend on MR1 OP[7] repectively
5. tWPRE values depend on MR1 OP[2] respectively
6. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRTP(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRTP[ns] / tCK[ns])
7. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up

to the next integer: Minimum Delay[cycles] = Roundup(tWR[ns] / tCK[ns])

8. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tRPpb(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tRPpb[ns] / tCK[ns])
9. Minimum Delay between "From Command" and "To Command" in clock cycle is calculated by dividing tWTR(in ns) by tCK(in ns) and rounding up to the next integer: Minimum Delay[cycles] = Roundup(tWTR[ns] / tCK[ns])
10. For Read w/AP the value is nRTP which is defined in Mode Register 2.
11. For Write w/AP the value is nWR which is defined in Mode Register 1.

**Table 39 - Timing Between Commands (Precharge and Auto-Precharge) - DQ ODT is Enabled**

| From Command | To Command | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|---|---|---|---|---|
| Read w/ AP (BL16) | Write or Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | tCK | 2,3 |
| | Masked Write or Masked Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | tCK | 2,3 |
| Read w/ AP (BL32) | Write or Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | tCK | 2,3 |
| | Masked Write or Masked Write w/ AP (different bank) | RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-ODTLon-RD(tODTon,min/tCK)+1 | tCK | 2,3 |

Notes

1. The rest of Precharge and Auto-Precharge timings are as same as DQ ODT disabled case.
2. After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and Masked Write operations may not be truncated or interrupted.
3. tRPST values depend on MR1 OP[7] respectively.

## 2.18. Refresh command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of the clock. Per bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. All bank REFRESH is initiated with CA5 HIGH at the first rising edge of the clock.

A per bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1 and CA2 at the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1 and bank address BA2 is transferred on CA2. A per bank REFRESH command (REFpb) to the eight banks can be issued in any order. e.g. REFpb commands are issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per bank REFRESH command the controller can send another set of per bank REFRESH commands in the same order or a different order. e.g. REFpb commands are issued in the following order that is different from the previous order:
7-1-3-5-0-4-2-6. One of the possible order can also be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per bank REFRESH command to the same bank unless all eight banks have been refreshed using the per bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon asserting RESET_n or at every exit from Self Refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in Self Refresh or a REFab command can be issued at any time without cycling through all eight banks using per bank REFRESH command. After the bank count is synchronized to zero the controller can issue per bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFpb) is issued after the REFab command, then it uses an incremented value of the row counter. Table below shows examples of both bank and refresh couter increment behavior.

**Table 40 - Bank and Refresh counter increment behavior**

| # | Sub # | Command | BA0 | BA1 | BA2 | Refresh Bank# | Bank Counter # | Ref Counter # (Row Address #) |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | Reset, SRX or REFab | | | | | To 0 | - |
| 1 | 1 | REFpb | 0 | 0 | 0 | 0 | 0 to 1 | n |
| 2 | 2 | REFpb | 0 | 0 | 1 | 1 | 1 to 2 | |
| 3 | 3 | REFpb | 0 | 1 | 0 | 2 | 2 to 3 | |
| 4 | 4 | REFpb | 0 | 1 | 1 | 3 | 3 to 4 | |
| 5 | 5 | REFpb | 1 | 0 | 0 | 4 | 4 to 5 | |
| 6 | 6 | REFpb | 1 | 0 | 1 | 5 | 5 to 6 | |
| 7 | 7 | REFpb | 1 | 1 | 0 | 6 | 6 to 7 | |
| 8 | 8 | REFpb | 1 | 1 | 1 | 7 | 7 to 0 | |
| 9 | 1 | REFpb | 1 | 1 | 0 | 6 | 0 to 1 | n + 1 |
| 10 | 2 | REFpb | 1 | 1 | 1 | 7 | 1 to 2 | |
| 11 | 3 | REFpb | 0 | 0 | 1 | 1 | 2 to 3 | |
| 12 | 4 | REFpb | 0 | 1 | 1 | 3 | 3 to 4 | |
| 13 | 5 | REFpb | 1 | 0 | 1 | 5 | 4 to 5 | |
| 14 | 6 | REFpb | 0 | 1 | 0 | 2 | 5 to 6 | |
| 15 | 7 | REFpb | 0 | 0 | 0 | 0 | 6 to 7 | |
| 16 | 8 | REFpb | 1 | 0 | 0 | 4 | 7 to 0 | |
| 17 | 1 | REFpb | 0 | 0 | 0 | 0 | 0 to 1 | n + 2 |
| 18 | 2 | REFpb | 0 | 0 | 1 | 1 | 1 to 2 | |
| 19 | 3 | REFpb | 0 | 1 | 0 | 2 | 2 to 3 | |
| 24 | 0 | REFab | V | V | V | 0~7 | To 0 | n + 2 |
| 25 | 1 | REFpb | 1 | 1 | 0 | 6 | 0 to 1 | n + 3 |
| 26 | 2 | REFpb | 1 | 1 | 1 | 7 | 1 to 2 | |
| Snip | | | | | | | | |

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per-bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions are met:

- tRFCab has been satisfied after the prior REFab command
- tRFCpb has been satisfied after the prior REFpb command
- tRP has been satisfied after the prior PRECHARGE command to that bank
- tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFpb command).

The target bank is inaccessible during per-bank REFRESH cycle time (tRFCpb), however, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be

maintained in an active state or accessed by a READ or a WRITE command. When the per-bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, these conditions must be met:

- tRFCpb must be satisfied before issuing a REFab command
- tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
- tRRD must be satisfied before issuing an ACTIVATE command to a different bank
- tRFCpb must be satisfied before issuing another REFpb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-all command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command
- tRFCpb has been satisfied following the prior REFpb command
- tRP has been satisfied following the prior PRECHARGE commands.

When an all-bank refresh cycle has completed, all banks will be idle. After issuing REFab:

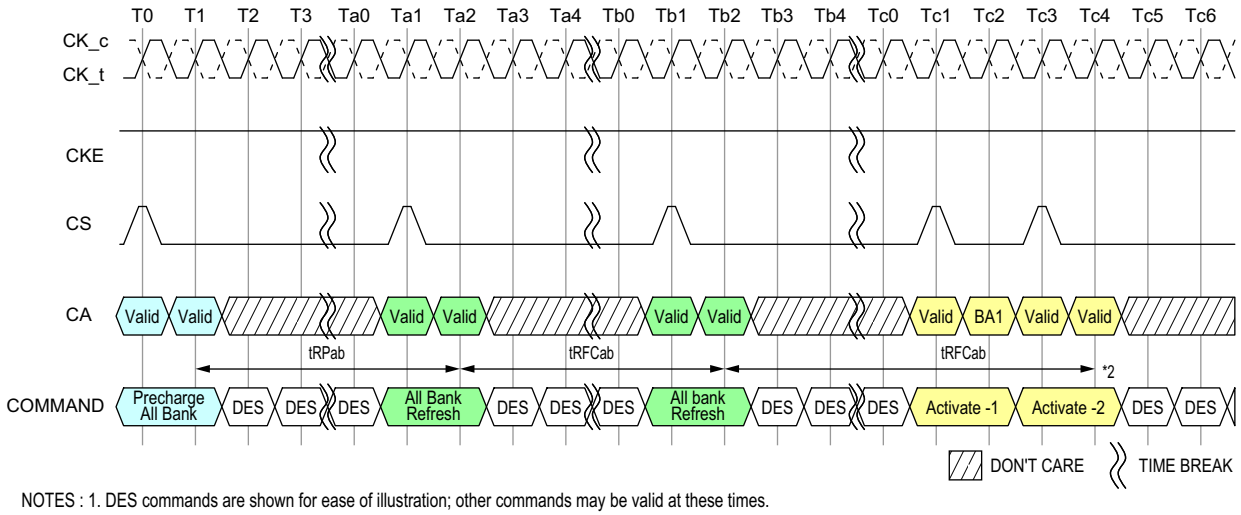
- tRFCab latency must be satisfied before issuing an ACTIVATE command
- tRFCab latency must be satisfied before issuing a REFab or REFpb command.

**Table 41 - REFRESH Command Scheduling Seperation requirements**

| Symbol | minimum delay from | to | Notes |
|---|---|---|---|
| tRFCab | REFab | REFab | |
| | | Activate command to any bank | |
| | | REFpb | |
| tRFCpb | REFpb | REFab | |
| | | Activate command to same bank as REFpb | |
| | | REFpb | |
| tRRD | REFpb | Activate command to different bank than REFpb | |
| | Activate | REFpb | 1 |
| | | Activate command to different bank than prior Activate command | |

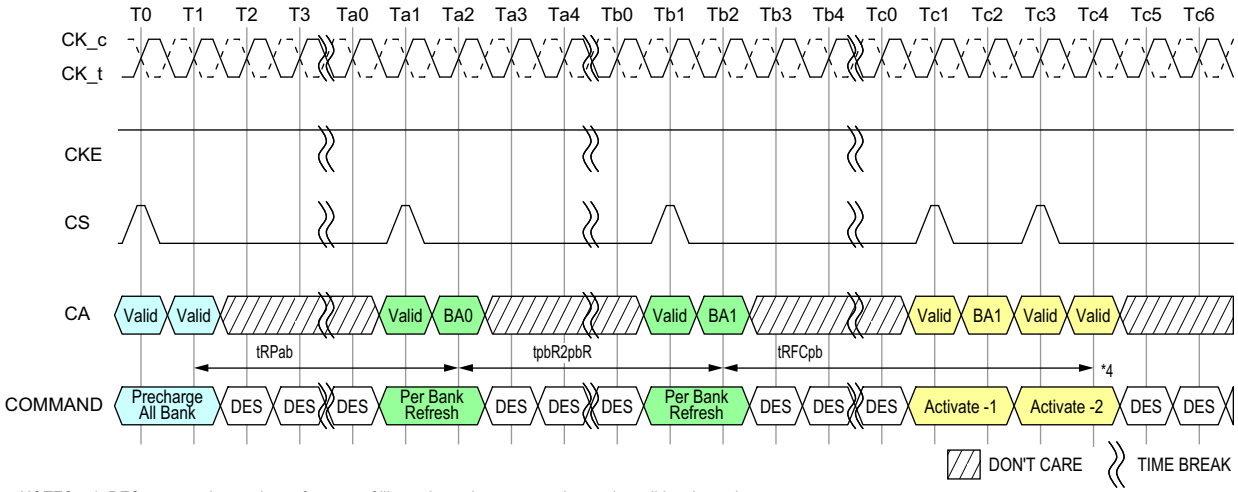
Notes

1. A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFpb is supported only if it affects a bank that is in the idle state.



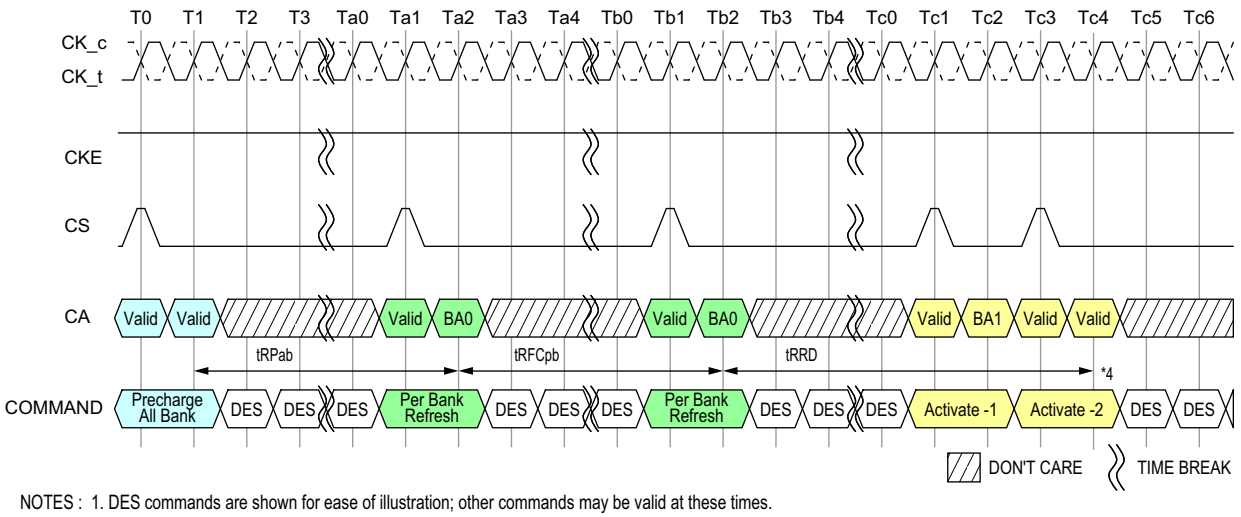

NOTES : 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 64 - All-Bank REFRESH Operation**




NOTES : 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. In the beginning of this example, the REFpb bank is pointing to bank 0.
3. Operations to banks other than the bank being refreshed are supported during the tpbR2pbR period.
4. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 65 - Per Bank Refresh to a different bank Operation**




NOTES : 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
2. In the beginning of this example, the REFpb bank is pointing to bank 0.
3. Operations to banks other than the bank being refreshed are supported during the tRFCpb period.
4. Activate Command is shown as an example. Other commands may be valid provided the timing specification is satisfied.

**Figure 66 - Per Bank Refresh to the same bank Operation**

In general, a Refresh command needs to be issued to the LPDDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR4 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI. A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI.

At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI. Self-Refresh Mode may be entered with a maximum of eight Refresh commands being postponed. After exiting Self- Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self- Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

And for per bank refresh, a maximum 8 x 8 per bank refresh commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per bank refresh commands can be issued within 2 x tREFI.

**Table 42 - Legacy Refresh Command Timing Constraints**

| MR4 OP[2:0] | Refresh rate | Max. No. of pulled in or postponed REFab | Max. interval between two REFab | Max. No. of REFab within max(2*tREFI*Refresh rate multiplier, 16*tRFC) | Per-bank Refresh |
|---|---|---|---|---|---|
| 000B | Low Temp. Limit | N/A | N/A | N/A | N/A |
| 001B | 4 x tREFI | 8 | 9 x 4 x tREFI | 16 | 1/8 of REFab |
| 010B | 2 x tREFI | 8 | 9 x 2 x tREFI | 16 | 1/8 of REFab |
| 011B | 1 x tREFI | 8 | 9 x tREFI | 16 | 1/8 of REFab |
| 100B | 0.5 x tREFI | 8 | 9 x 0.5 x tREFI | 16 | 1/8 of REFab |
| 101B | 0.25 x tREFI | 8 | 9 x 0.25 x tREFI | 16 | 1/8 of REFab |
| 110B | 0.25 x tREFI | 8 | 9 x 0.25 x tREFI | 16 | 1/8 of REFab |
| 111B | High Temp. Limit | N/A | N/A | N/A | N/A |

**Table 43 - Modified Refresh Command Timing Constraints**

| MR4 OP[2:0] | Refresh rate | Max. No. of pulled in or postponed REFab | Max. interval between two REFab | Max. No. of REFab within max(2*tREFI*Refresh rate multiplier, 16*tRFC) | Per-bank Refresh |
|---|---|---|---|---|---|
| 000B | Low Temp. Limit | N/A | N/A | N/A | N/A |
| 001B | 4 x tREFI | 2 | 3 x 4 x tREFI | 4 | 1/8 of REFab |
| 010B | 2 x tREFI | 4 | 5 x 2 x tREFI | 8 | 1/8 of REFab |
| 011B | 1 x tREFI | 8 | 9 x tREFI | 16 | 1/8 of REFab |
| 100B | 0.5 x tREFI | 8 | 9 x 0.5 x tREFI | 16 | 1/8 of REFab |
| 101B | 0.25 x tREFI | 8 | 9 x 0.25 x tREFI | 16 | 1/8 of REFab |
| 110B | 0.25 x tREFI | 8 | 9 x 0.25 x tREFI | 16 | 1/8 of REFab |
| 111B | High Temp. Limit | N/A | N/A | N/A | N/A |

Notes

1. For any thermal transition phase where Refresh mode is transitioned to either 2x tREFIor 4x tREFI, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.

2. LPDDR4 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[2:0]. If shorter refresh period is applied, the corresponding requirements from Table apply. For example, when MR4 OP[2:0]=001B, controller can be in any refresh rate from 4xtREFI to 0.25x tREFI. When MR4 OP[2:0]=010B, the only prohibited refresh rate is 4x tREFI.

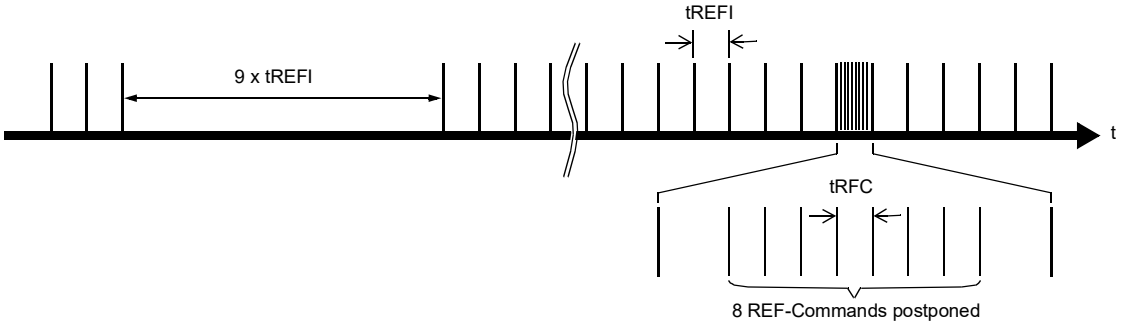



**Figure 67 - Postponing Refresh Commands (Example)**

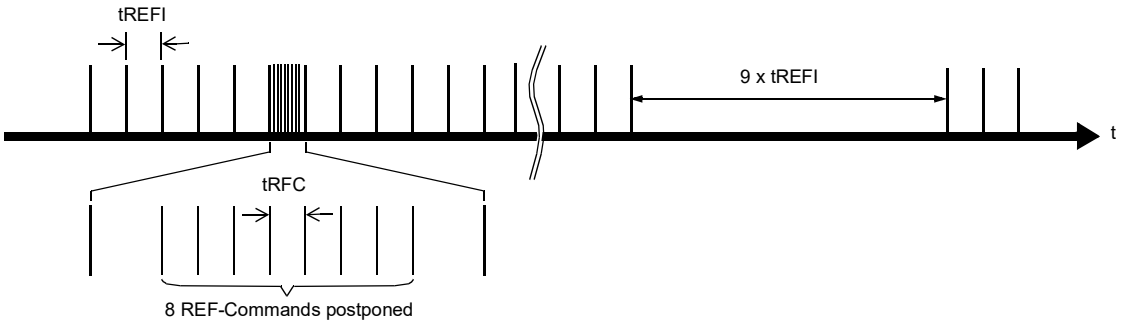
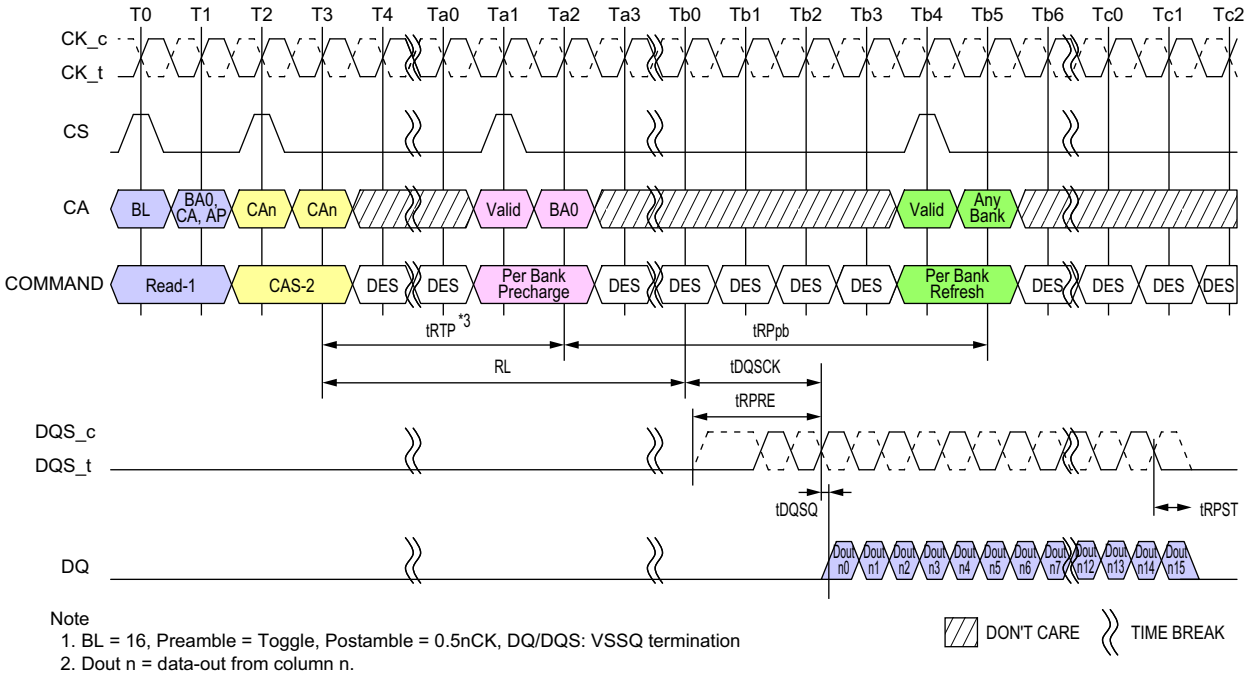



**Figure 68 - Pulling-in Refresh Commands (Example)**

### 2.18.1. Burst Read operation followed by Per Bank Refresh

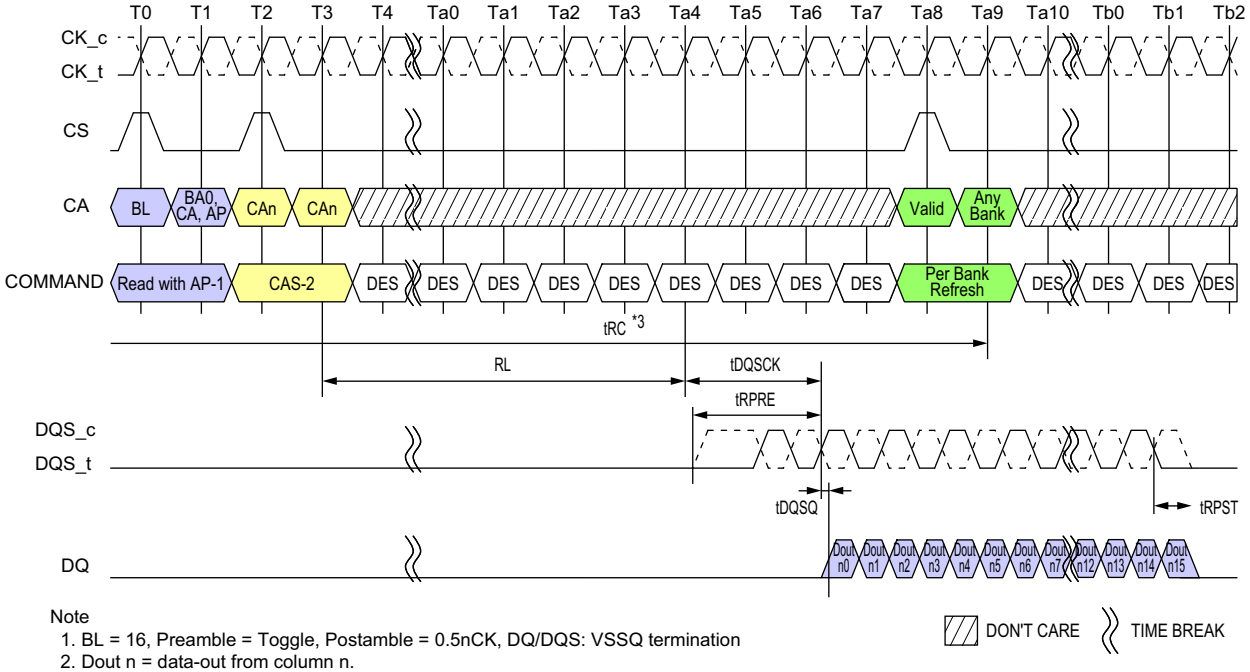
The Per Bank Refresh command can be issued after tRTP + tRPpb from Read command.




Note
1. BL = 16, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n.
3. In case of BL = 32, Delay time from Read to Per Bank Precharge is 8nCK + tRTP.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 69 - Burst Read operation followed by Per Bank Refresh**

The Per Bank Refresh command can be issued after tRC from Read with Auto Precharge command.




Note
1. BL = 16, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n.
3. tRC needs to be satisfied prior to issuing subsequent Per Bank Refresh command.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 70 - Burst Read with Auto-Precharge operation followed by Per Bank Refresh**

## 2.19. Refresh Requirements

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

**Table 44 - Refresh Requirement Parameters per die for Dual Channel SDRAM devices**

| Density | | Symbol | 2Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | 24Gb | 32Gb | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Density per channel | | | 1Gb | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | - |
| Number of Banks | | | 8 | | | | | | | | - |
| Refresh Window 1 x tREFI | | tREFW | 32 | | | | | | | | ms |
| Required number of REFRESH commands | | R | 8,192 | | | | | | | | - |
| Average Refresh Interval 1 x tREFI | REFab | tREFI | 3.904 | | | | | | | | us |
| | REFpb | tREFIpb | 488 | | | | | | | | ns |
| Average Refresh Interval 0.5 x tREFI | REFab | tREFI | 1.953 | | | | | | | | us |
| | REFpb | tREFIpb | 244 | | | | | | | | ns |
| Average Refresh Interval 0.25 x tREFI | REFab | tREFI | 0.965 | | | | | | | | us |
| | REFpb | tREFIpb | 122 | | | | | | | | ns |
| Refresh Cycle Time (All Banks) | | tRFCab | 130 | 130 | 180 | 180 | 280 | | 380 | | ns |
| Refresh Cycle Time (per Bank) | | tRFCpb | 60 | 60 | 90 | 90 | 140 | | 190 | | ns |
| Per-bank Refresh to Per-bank Refresh different bank Time | | tpbR2pbR | 60 | 60 | 90 | | | | | | ns |

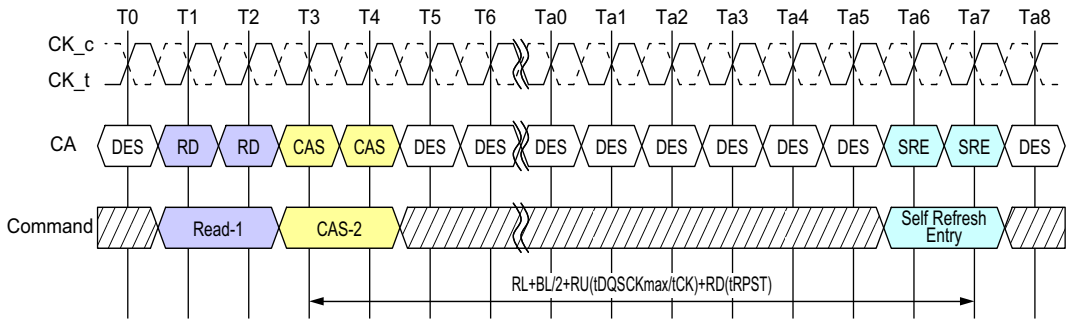
Notes

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with12 Gb device and tXSR_abort(min) is defined as tRFCpb + 17.5ns.
3. 1x refersh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[2:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.
4. Refer to MR4 OP[2:0] for detailed Refresh Rate and its multipliers.

## 2.20. Self Refresh Operation

### 2.20.1. Self Refresh Entry and Exit

The Self Refresh command can be used to retain data in the LPDDR4 SDRAM, the SDRAM retains data without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by having CS High, CA0 Low, CA1 Low, CA2 Low; CA3 High; CA4 High, CA5 Valid (Valid that means it is Logic Level, High or Low) for the first rising edge and CS Low, CA0 Valid, CA1 Valid, CA2 Valid, CA3 Valid, CA4 Valid, CA5 Valid at the second rising edge of the clock. Self Refresh command is only allowed when read data burst is completed and SDRAM is idle state.



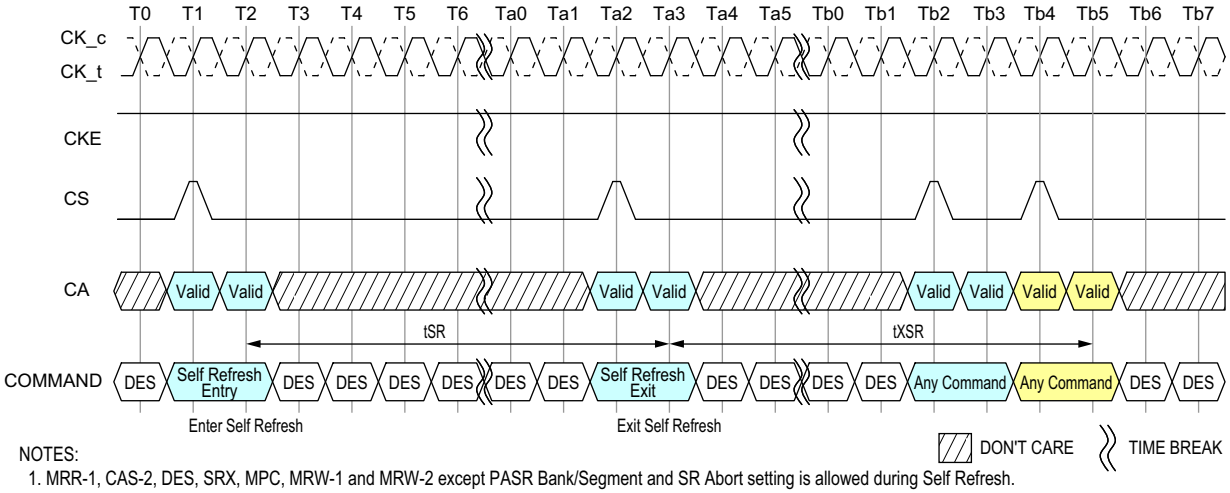

During Self Refresh mode, external clock input is needed and all input pin of SDRAM are activated. SDRAM can accept the following commands, MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 except PASR Bank/Segment and SR Abort setting.

LPDDR4 SDRAM can operate in Self Refresh in both the standard or elevated temperature ranges. SDRAM will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperature and higher at high temperatures.

For proper Self Refresh operation, power supply pins (VDD1, VDD2 and VDDQ) must be at valid levels. However VDDQ may be turned off during Self Refresh with Power Down after tCKELCK(Max(5ns,5nCK)) is satisfied (Refer to Figure 66 about tCKELCK).

Prior to exiting Self Refresh with Power Down, VDDQ must be within specified limits. The minimum time that the SDRAM must remain in Self Refresh model is tSR,min. Once Self Refresh Exit is registered, only MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment and SR Abort setting are allowed until tXSR is satisfied.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (8 per bank or 1 all bank) is issued before entry into a subsequent Self Refresh.
This REFRESH command is not included in the count of regular refresh commands required by the tREFI interval, and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 X tREFI.

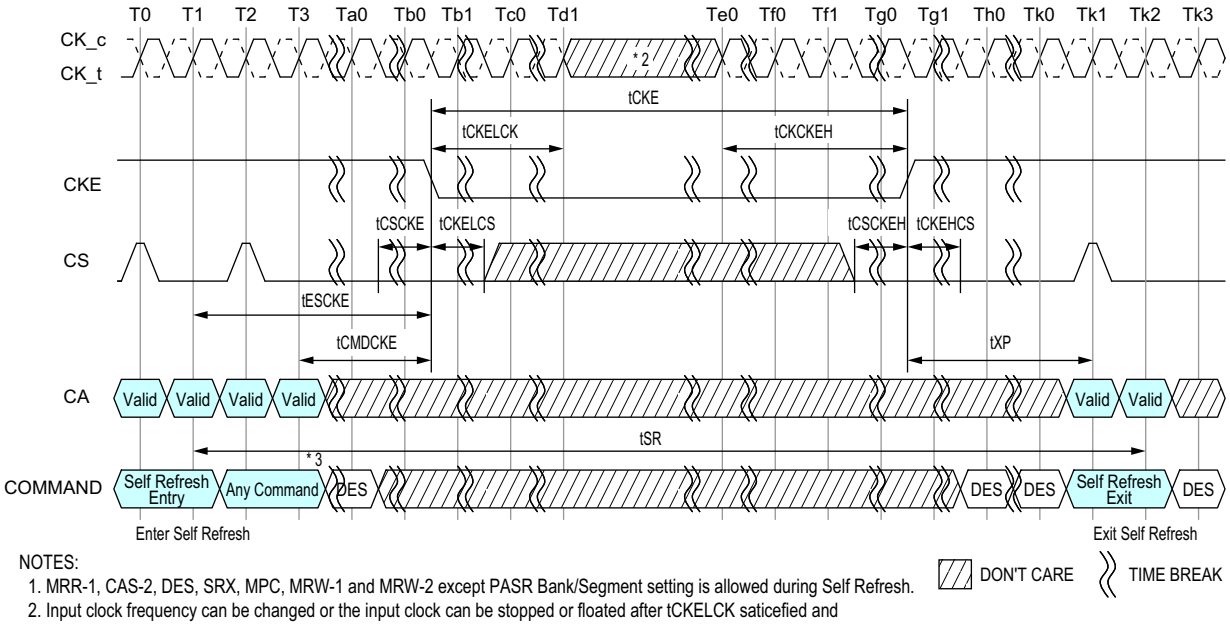



NOTES:
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment and SR Abort setting is allowed during Self Refresh.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 71 - Self Refresh Entry/Exit Timing**

### 2.20.2. Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in LPDDR4 SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure-Self Refresh Entry/Exit Timing with Power Down Entry/Exit.




NOTES:
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after tCKELCK saticefied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. 2 Clock command for example.

**Figure 72 - Self Refresh Entry/Exit Timing with Power Down Entry/Exit**

### 2.20.2.1. Partial Array Self-Refresh (PASR)

#### 2.20.2.1.1. PASR Bank Masking

The LPDDR4 SDRAM has eight banks. Each bank of an LPDDR4 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16.

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

#### 2.20.2.1.2. PASR Segment Masking

A segment masking scheme may be used in lieu of or in combination with the bank masking scheme in LPDDR4 SDRAM which utilize eight segments per bank. For segment masking bit assignments, see Mode Register 17. For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, "masked". Programming of segment mask bits is similar to the one of bank mask bits. Eight segments are used as listed in Mode Register 17. One mode register unit is used for the programming of segment mask bits up to 8 bits. One more mode register unit may be reserved for future use. Programming of bits in the reserved registers has no effect on the device operation.

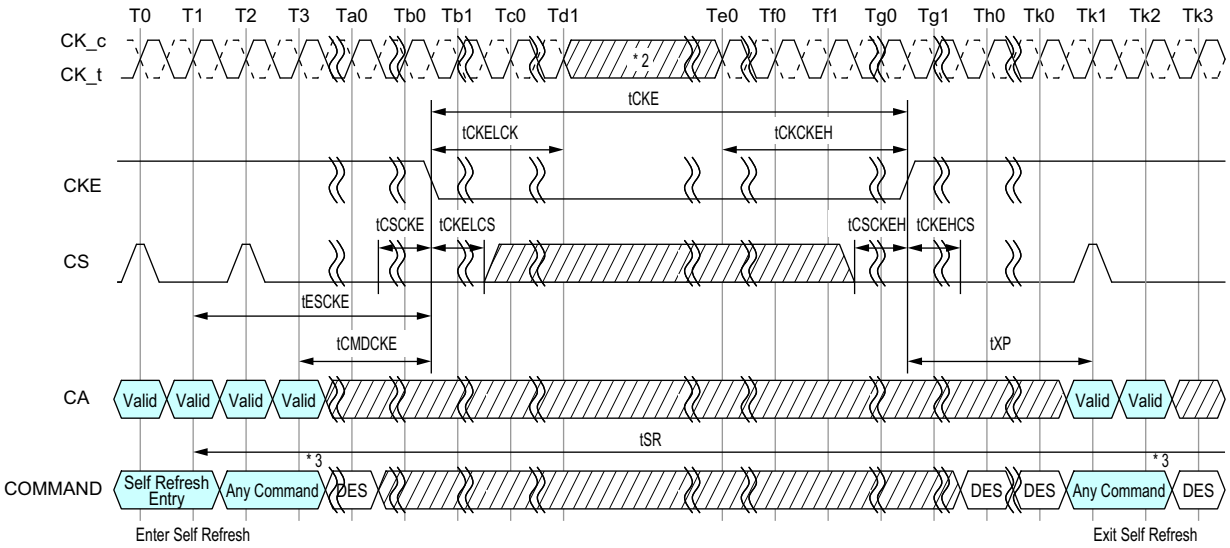
**Table 45 - Example of Bank and Segment Masking use in LPDDR4 SDRAM**

| | Segment Mask (MR17) | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 | Bank 6 | Bank 7 |
|---|---|---|---|---|---|---|---|---|---|
| Bank Mask (MR16) | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| Segment 0 | 0 | | M | | | | | | M |
| Segment 1 | 0 | | M | | | | | | M |
| Segment 2 | 1 | M | M | M | M | M | M | M | M |
| Segment 3 | 0 | | M | | | | | | M |
| Segment 4 | 0 | | M | | | | | | M |
| Segment 5 | 0 | | M | | | | | | M |
| Segment 6 | 0 | | M | | | | | | M |
| Segment 7 | 1 | M | M | M | M | M | M | M | M |

Notes
1. This table illustrates an example of an 8-bank LPDDR4 SDRAM, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

### 2.20.3. Command Input Timing after Power Down Exit

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure below.




NOTES:

1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting is allowed during Self Refresh.
2. Input clock frequency can be changed or the input clock can be stopped or floated after tCKELCK saticefied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
3. 2 Clock command for example.

**Figure 73 - Command input timings after Power Down Exit during Self Refresh**

## 2.20.4. AC Timing Table

**Table 46 - Self Refresh Timing Parameters**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Delay from SRE command to CKE Input low | tESCKE | min | max (1.75ns,3tCK) | | | | | | | | tCK | 1 |
| Minimum Self Refresh Time | tSR | min | max (15ns, 3nCK) | | | | | | | | tCK | 1 |
| Exit Self Refresh to Valid commands | tXSR | min | max (tRFCab + 7.5ns, 2nCK) | | | | | | | | tCK | 1,2 |

Notes

1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.

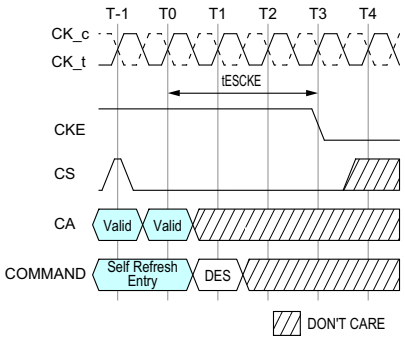



**Figure 74 - tESCKE Timing**

2. MRR-1, CAS-2, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are only allowed during this period.

## 2.21. Self Refresh Abort

If MR4 OP[3] is enabled then DRAM aborts any ongoing refresh during Self Refresh exit and does not increment the internal refresh counter. Controller can issue a valid command after a delay of tXSR_abort instead of tXSR.

The value of tXSR_abort(min) is defined as tRFCpb + 17.5ns.

Upon exit from Self Refresh mode, the LPDDR4 SDRAM requires a minimum of one extra refresh (8 per bank or 1 all bank) before entry into a subsequent Self Refresh mode. This requirement remains the same irrespective of the setting of the MR bit for Self Refresh abort.

Self Refresh abort feature is available for higher density devices starting with12 Gb dual channel device and 6 Gb single channel device.

## 2.22. MRR, MRW, MPC Command during tXSR, tRFC

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tXSR period.

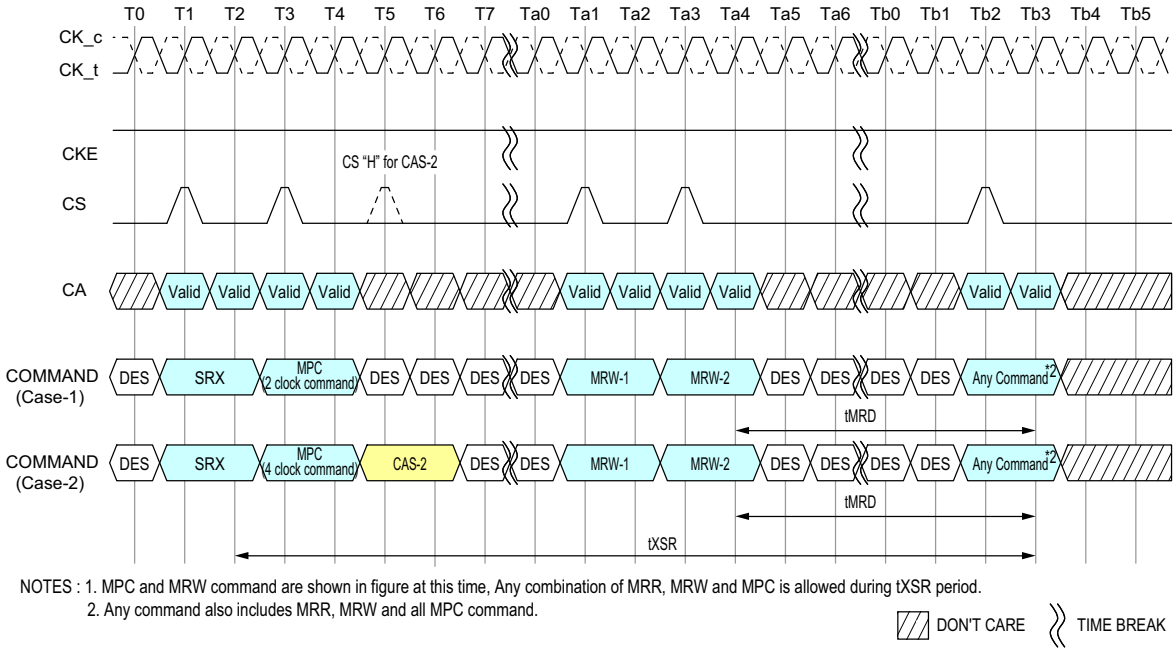



**Figure 75 - MRR, MRW and MPC Commands Issuing Timing during tXSR**

Mode Register Read (MRR), Mode Register Write (MRW) and Multi Purpose Command (MPC) can be issued during tRFC period.

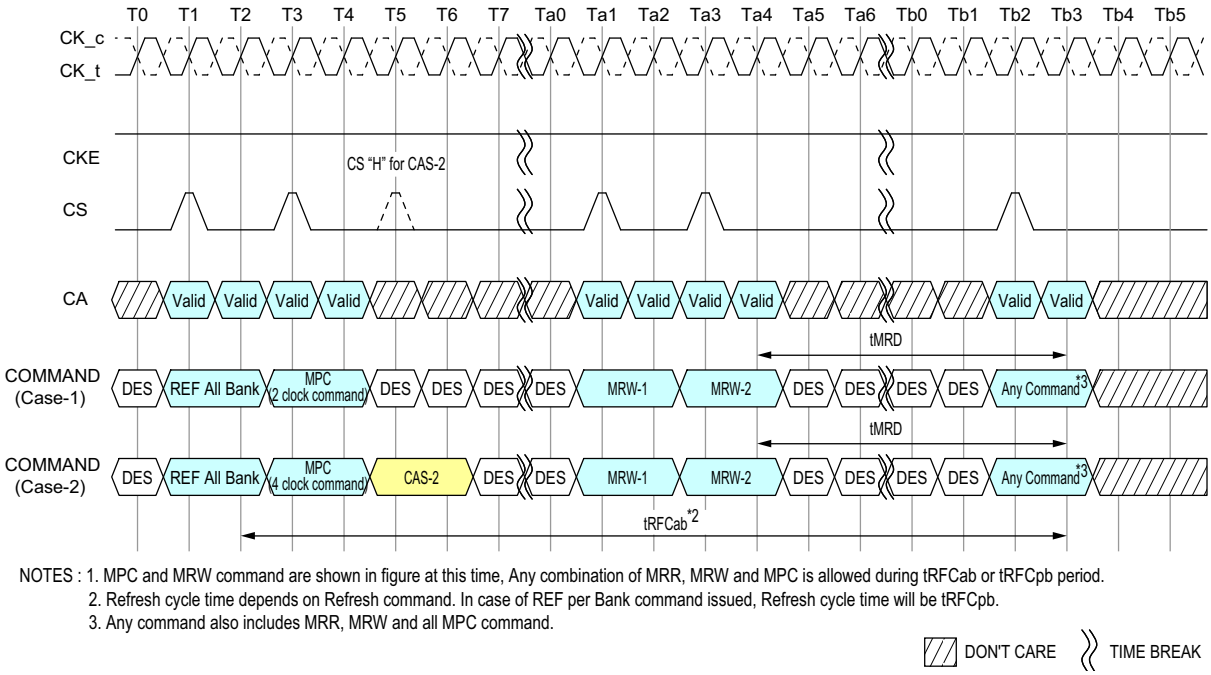



**Figure 76 - MRR, MRW and MPC Commands Issuing Timing during tRFC**

## 2.23. Mode Register Read (MRR) command

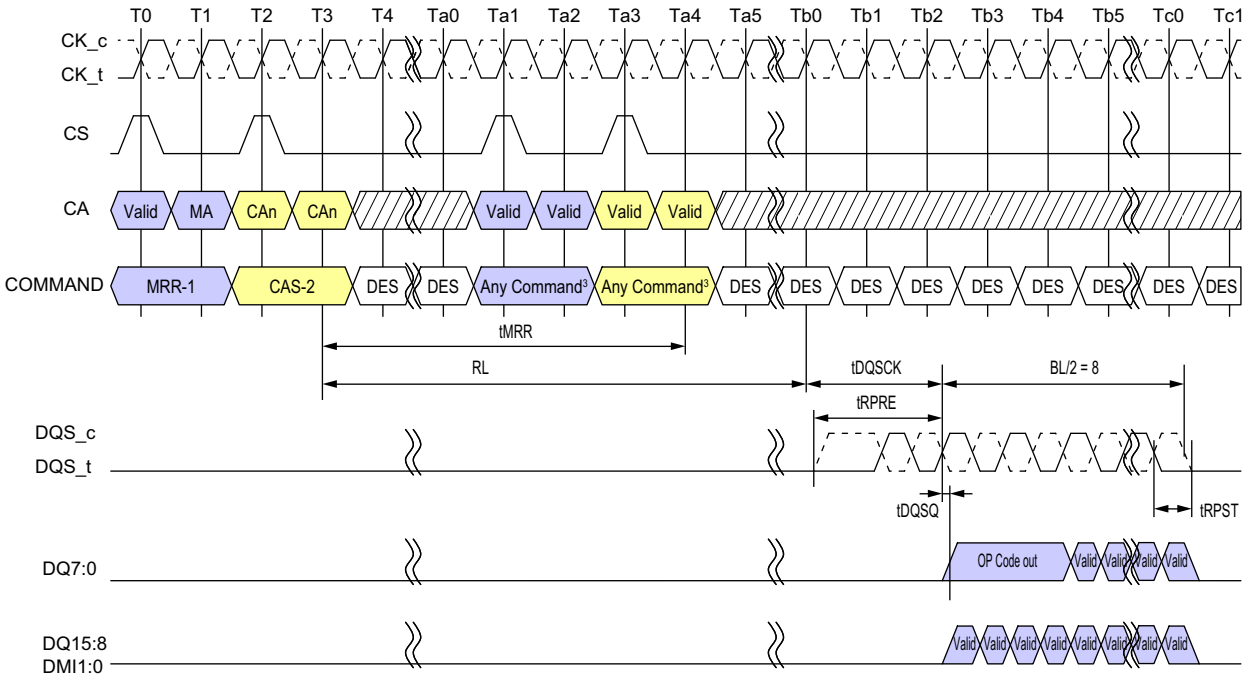
The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4-SDRAM registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after RL x tCK + tDQSCK + tDQSQ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16.

MRR operation must not be interrupted.

**Table 47 - DQ output mapping**

| BL | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQ0 | OP0 | | | | V | | | | | | | | | | | |
| DQ1 | OP1 | | | | V | | | | | | | | | | | |
| DQ2 | OP2 | | | | V | | | | | | | | | | | |
| DQ3 | OP3 | | | | V | | | | | | | | | | | |
| DQ4 | OP4 | | | | V | | | | | | | | | | | |
| DQ5 | OP5 | | | | V | | | | | | | | | | | |
| DQ6 | OP6 | | | | V | | | | | | | | | | | |
| DQ7 | OP7 | | | | V | | | | | | | | | | | |
| DQ8-15 | V | | | | | | | | | | | | | | | |
| DMI | V | | | | | | | | | | | | | | | |

Notes
1. MRR data are extended to first 4 UI's for DRAM controller to sample data easily.
2. DBI may apply or may not apply during normal MRR. It's vendor specific. If read DBI is enable with MRS and vendor cannot support the DBI during MRR, DMI pin status should be low.
3. The read pre-amble and post-amble of MRR are same as normal read.

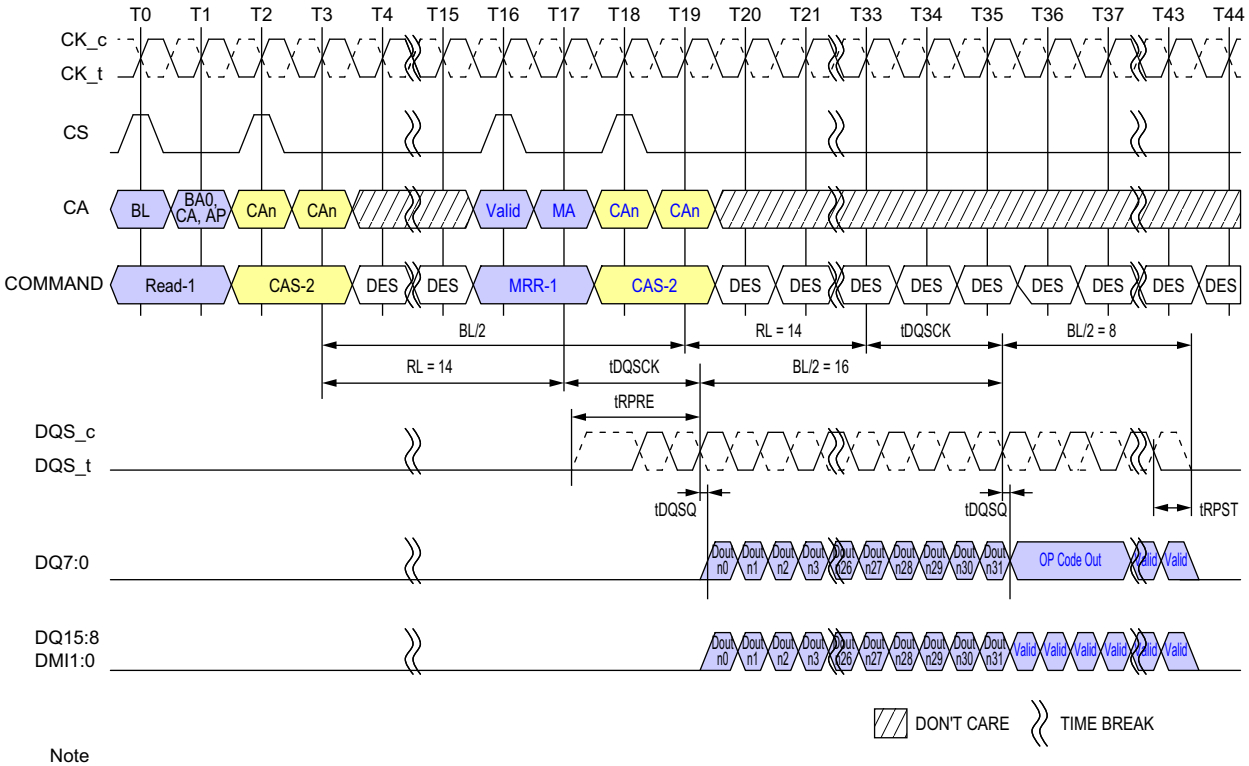



Note
1. Only BL=16 is supported
2. Only DES is allowed during tMRR period
3. There are some exceptions about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints Table for detail.
4. DBI is Disable mode.
5. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.
6 . DQ/DQS: VSSQ termination

**Figure 77 - Mode Register Read Operation**

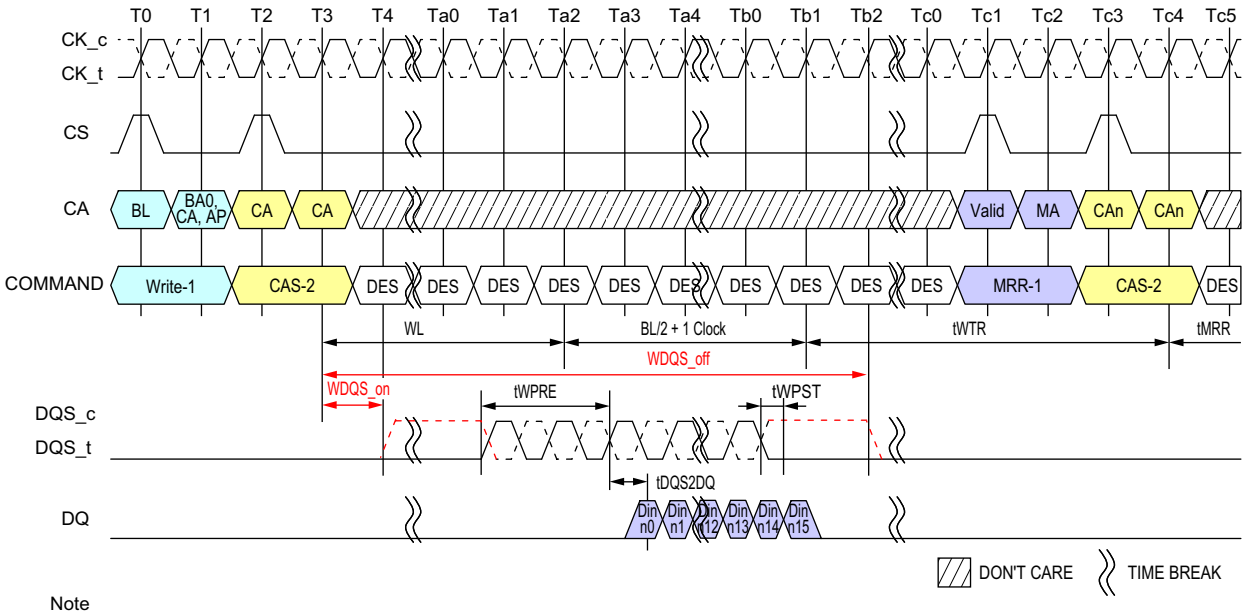
### 2.23.1. MRR After Read and Write Command

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles, in a similar way WL + BL/2 + 1 + RU(tWTR/tCK) clock cycles after a prior Write, Write with AP, Mask Write, Mask Write with AP and MPC Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus.




Note
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DBI = Disable, DQ/DQS: VSSQ termination
3. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 78 - Read to MRR Timing**

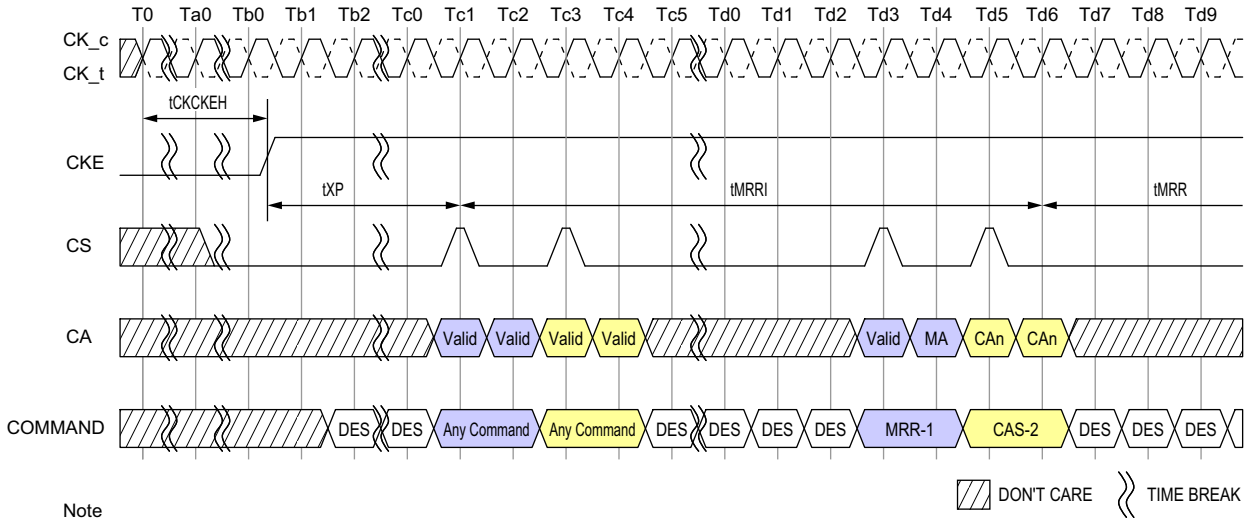



Note
1. Write BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination.
2. Only DES is allowed during tMRR period.
2. Din n = data-in to columnm n.
3. The minimum number of clock cycles from the burst write command to MRR command is WL + BL/2 + 1 + RU(tWTR/tCK).
4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 79 - Write to MRR Timing**

### 2.23.2. MRR after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power down mode.




Note
1. Only DES is allowed during tMRR period.
2. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

**Figure 80 - MRR Following Power-Down**

**Table 48 - Mode Register Read/Write AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Additional time after tXP has expired until the MRR command may be issued | tMRRI | min | tRCD + 3nCK | | | | | | | | ns | |
| MODE REGISTER Read command period | tMRR | min | 8 | | | | | | | | nCK | |
| MODE REGISTER Write command period | tMRW | min | max(10ns, 10nCK) | | | | | | | | ns | |
| Mode Register Write Set Command Delay | tMRD | min | max(14ns, 10nCK) | | | | | | | | ns | |

## 2.24. Mode Register Write (MRW) Operation

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (see Command Truth Table). The mode register address and the data written to the mode registers is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device.

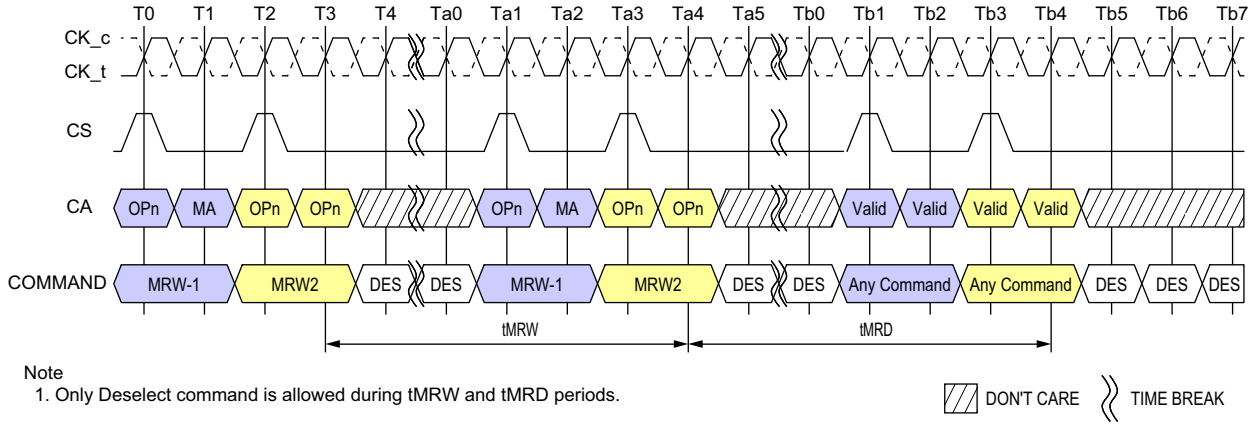



**Figure 81 - Mode Register Write Timing**

### 2.24.1. Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state.

**Table 49 - Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)**

| Current State | Command | Intermediate State | Next State |
|---|---|---|---|
| SDRAM | | SDRAM | SDRAM |
| All Banks Idle | MRR | Mode Register Reading (All Banks Idle) | All Banks Idle |
| | MRW | Mode Register Writing (All Banks Idle) | All Banks Idle |
| Bank(s) Active | MRR | Mode Register Reading | Bank(s) Active |
| | MRW | Mode Register Writing | Bank(s) Active |

**Table 50 - MRR/MRW Timing Constraints : DQ ODT Disabled**

| From Command | To Command | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|---|---|---|---|---|
| MRR | MRR | tMRR | - | |
| | RD/RDA | tMRR | - | |
| | WR/WRA/ MWR/MWRA | RL+RU(tDQSCK(max)/tCK)+BL/2-WL+tWPRE+RD(tRPST) | nCK | |
| | MRW | RL+RU(tDQSCK(max)/tCK)+BL/2+ 3 | nCK | |
| RD/RDA | MRR | BL/2 | nCK | |
| WR/WRA/ MWR/MWRA | | WL+1+BL/2+RU(tWTR/tCK) | nCK | |
| MRW | | tMRD | - | |
| Power Down Exit | | tXP+tMRRI | - | |
| MRW | RD/RDA | tMRD | - | |
| | WR/WRA/ MWR/MWRA | tMRD | - | |
| | MRW | tMRW | - | |
| RD/ RD FIFO/ RD DQ CAL | MRW | RL+BL/2+RU(tDQSCKmax/tCK) +RD(tRPST) +max(RU(7.5ns/ tCK),8nCK) | nCK | |
| RD with Auto-Precharge | | RL+BL/2+RU(tDQSCKmax/tCK) +RD(tRPST) +max(RU(7.5ns/ tCK),8nCK)+nRTP-8 | nCK | |
| WR/ MWR/ WR FIFO | | WL+1+BL/2+max(RU(7.5ns/tCK),8nCK) | nCK | |
| WR/MWR with Auto-Precharge | | WL+1+BL/2+max(RU(7.5ns/tCK),8nCK)+nWR | nCK | |

**Table 51 - MRR/MRW Timing Constraints : DQ ODT Enabled**

| From Command | To Command | Minimum Delay between "From Command" and "To Command" | Unit | Notes |
|---|---|---|---|---|
| MRR | MRR | Same as ODT Disable Case | - | |
| | RD/RDA | | | |
| | WR/WRA/ MWR/MWRA | RL+RU(tDQSCK(max)/tCK)+BL/2-ODTLon-RD(tODTon(min)/ tCK)+RD(tRPST)+1 | nCK | |
| | MRW | Same as ODT Disable Case | - | |
| RD/RDA | MRR | Same as ODT Disable Case | - | |
| WR/WRA/ MWR/MWRA | | | | |
| MRW | | | | |
| Power Down Exit | | | | |
| MRW | RD/RDA | Same as ODT Disable Case | - | |
| | WR/WRA/ MWR/MWRA | | | |
| | MRW | | | |
| RD/ RD FIFO/ RD DQ CAL | MRW | Same as ODT Disable Case | - | |
| RD with Auto-Precharge | | | | |
| WR/ MWR/ WR FIFO | | | | |
| WR/MWR with Auto-Precharge | | | | |

## 2.25. Vref Current Generator (VRCG)

LPDDR4 SDRAM $V_{REF}$ current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal VREF(DQ) and VREF(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown in Figure below.

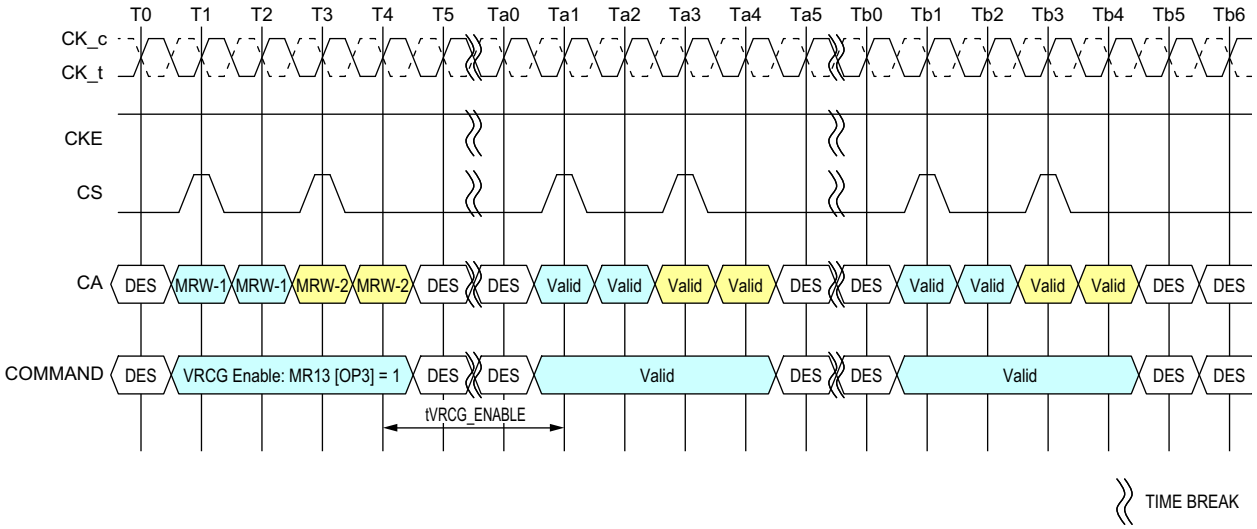



**Figure 82 - VRCG Enable timing**

VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown in figure below.

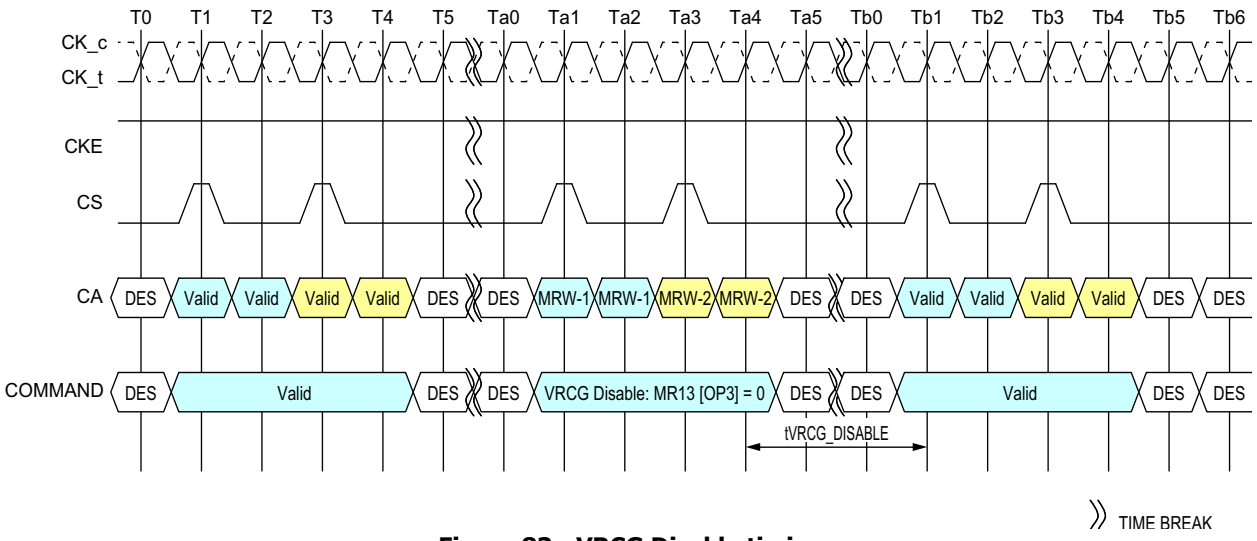



**Figure 83 - VRCG Disable timing**

Note that LPDDR4 SDRAM devices support VREF(CA) and VREF(DQ) range and value changes without enabling VRCG high current mode.

**Table 52 - VRCG Enable/Disable Timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VREF high current mode enable time | tVRCG_Enable | max | 200 | | | | | | | | ns | |
| VREF high current mode disable time | tVRCG_Disable | max | 100 | | | | | | | | ns | |

## 2.26. CA Vref Training

The DRAM internal CA Vref specification parameters are voltage operating range, step size, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

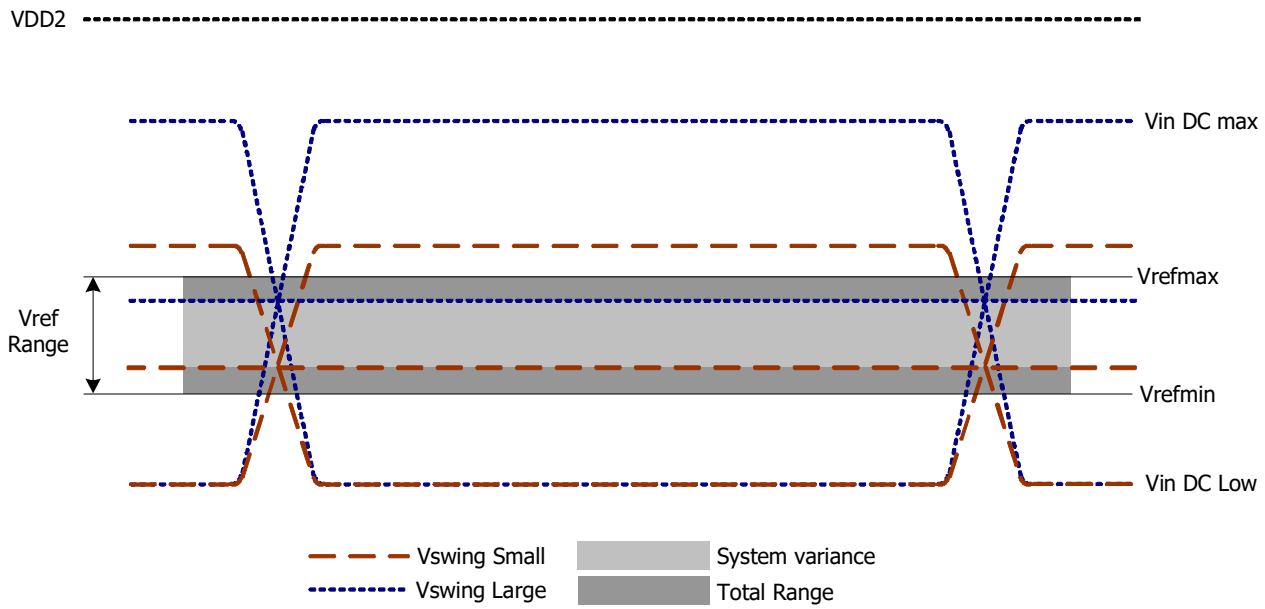



**Figure 84 - Vref operating range (Vref.min, Vref.max)**

The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.3% VDD2 to 0.5%VDD2. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainity is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

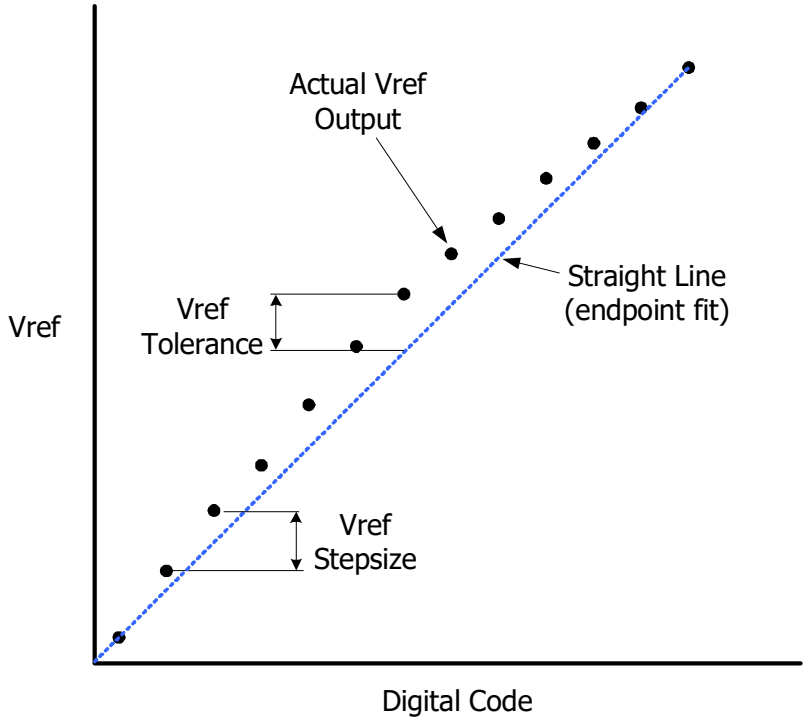



**Figure 85 - Example of Vref set tolerance (max case only shown) and stepsize**

The Vref increment/decrement step times are define by Vref_time-short, middle and long. The Vref_time-short, Vref_time-middle and Vref_time-long is defined from TS to TE as shown in the Figure "Vref_time for short, middle and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time TE as shown in Figure "Vref step single stepsize increment case". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characerization.

Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.
Vref_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefCA range in Vref voltage.
Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.

TS - is referenced to MRS command clock
TE - is referenced to the Vref_val_tol

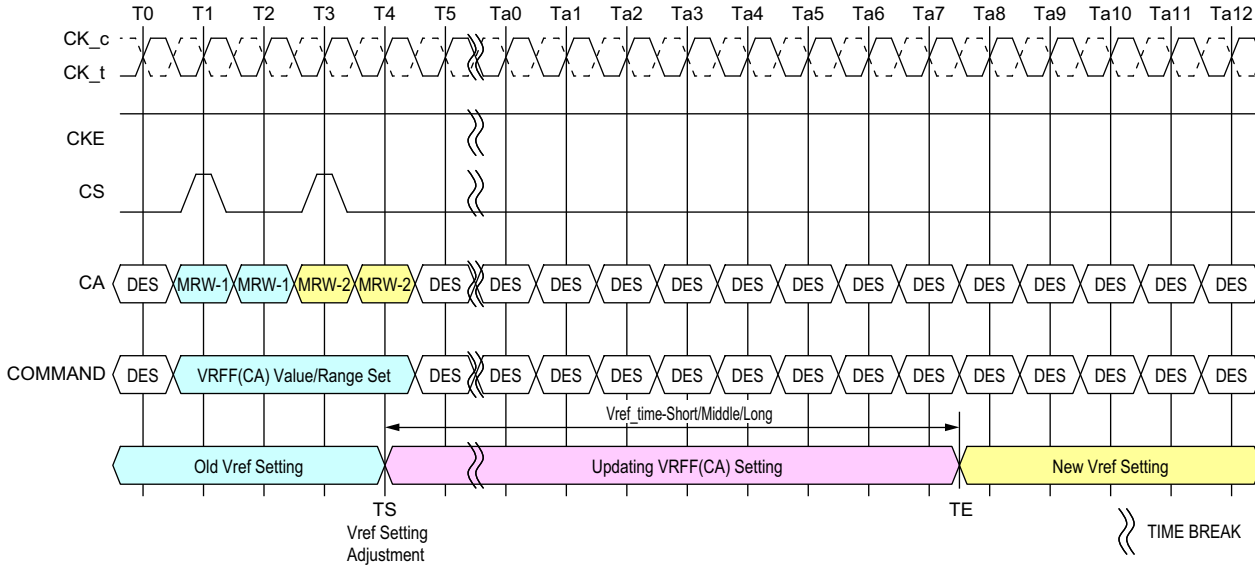



**Figure 86 - Vref_time for short, middle and long timing diagram**

The MRW command to the mode register bits are as follows.

MR12 OP[5:0] : VREF(CA) Setting
MR12 OP[6] : VREF(CA) Range

The minimum time required between two Vref MRS commands is Vref_time-short for single step and Vref_time-Middle for a full voltage range step.

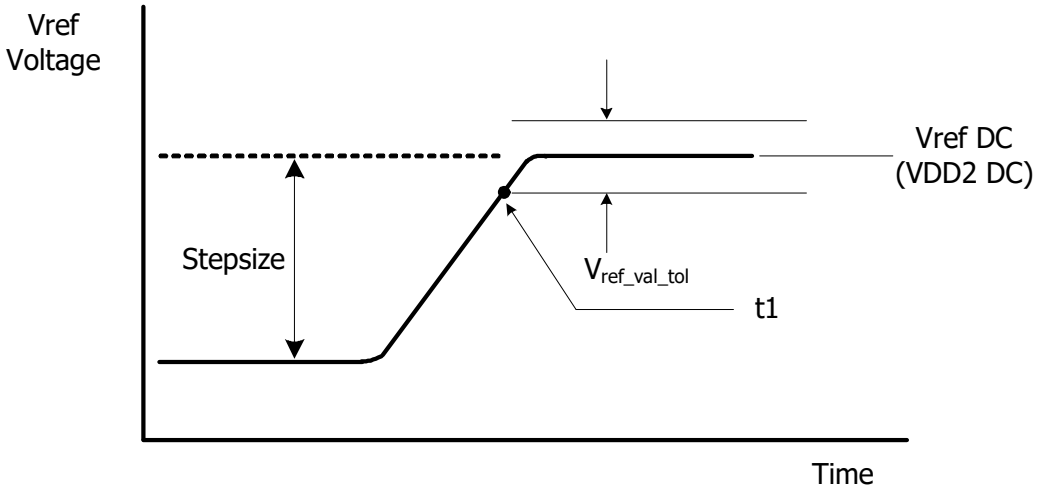



**Figure 87 - Vref step single stepsize increment case**

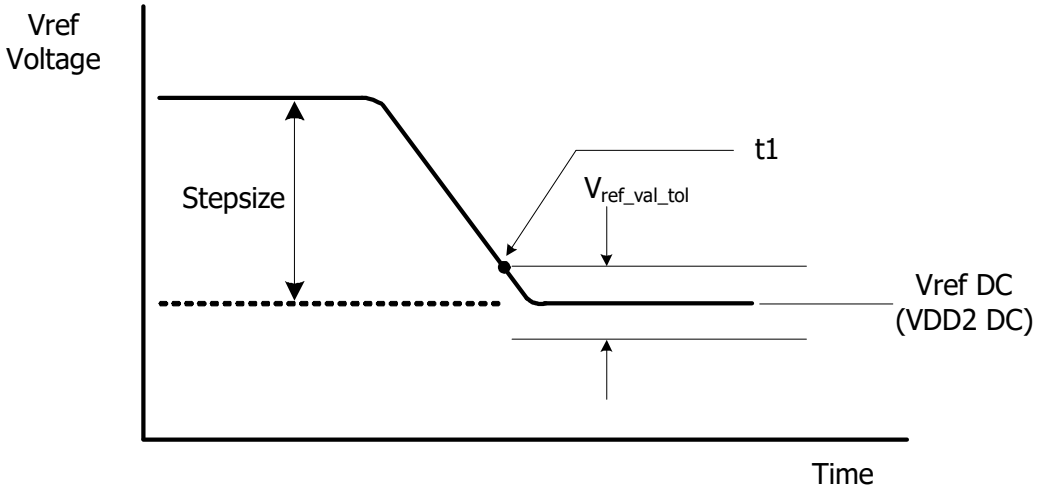



**Figure 88 - Vref step single stepsize decrement case**

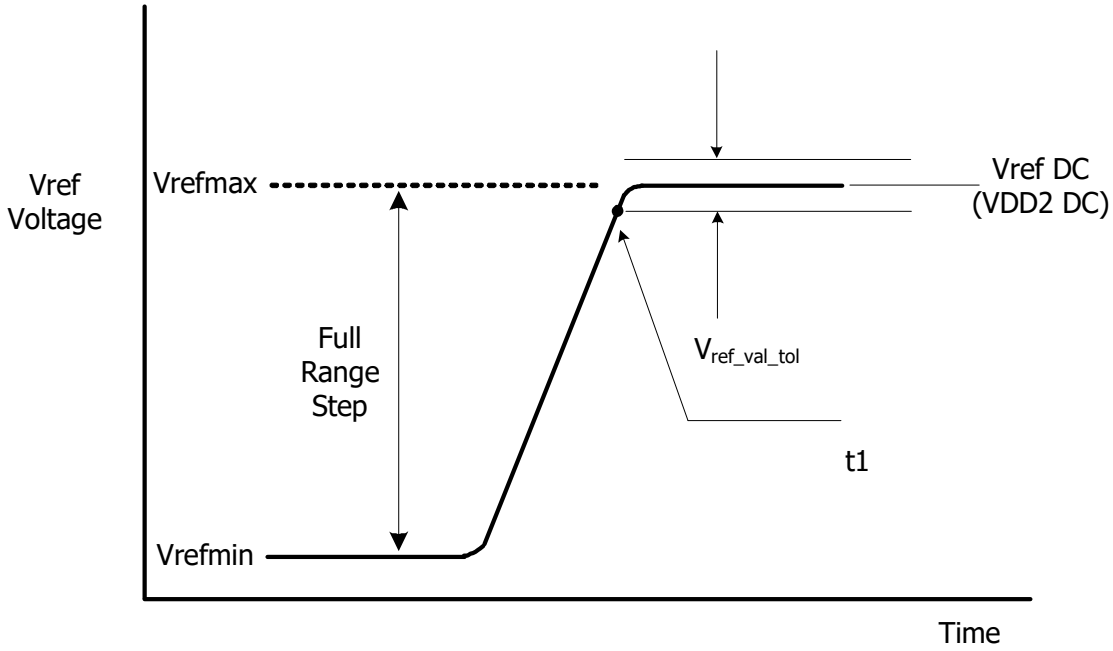



**Figure 89 - Vref full step from Vrefmin to Vrefmax case**

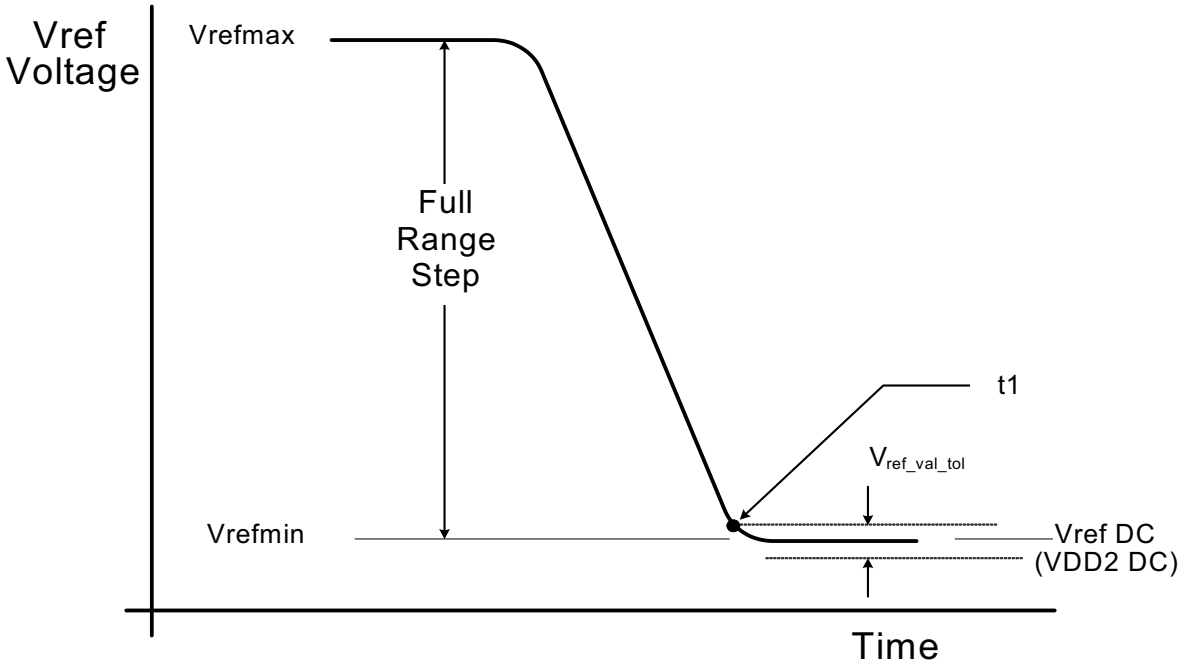



**Figure 90 - Vref full step from Vrefmax to Vrefmin case**

The table below contains the CA internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

**Table 53 - CA Internal Vref Specifications**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Vref Max operating point Range[0] | Vref_max_R0 | - | - | 44.9% | VDDQ | 1,11 |
| Vref Min operating point Range[0] | Vref_min_R0 | 15% | - | - | VDDQ | 1,11 |
| Vref Max operating point Range[1] | Vref_max_R1 | - | - | 62.9% | VDDQ | 1,11 |
| Vref Min operating point Range[1] | Vref_min_R1 | 32.9% | - | - | VDDQ | 1,11 |
| Vref Steps ize | Vref_step | 0.50% | 0.60% | 0.70% | VDDQ | 2 |
| Vref Set Tolerance | Vref_set_tol | -11 | 0 | 11 | mV | 3,4,6 |
| | | -1.1 | 0 | 1.1 | mV | 3,5,7 |
| Vref Step Time | Vref_time-short | - | - | 100 | ns | 8 |
| | Vref_time-middle | - | - | 200 | ns | 12 |
| | Vref_time-Long | - | - | 250 | ns | 9 |
| | Vref_time-weak | - | - | 1 | ms | 13,14 |
| Vref Valid tolerance | Vref_val_tol | -0.10% | 0.00% | 0.10% | VDDQ | 10 |

Notes

1. Vref DC voltage referenced to VDDQ_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3. Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance = Vref_new - 11mV.
   The maximum value of Vref setting tolerance = Vref_new + +11mV. For n>4
5. The minimum value of Vref setting tolerance = Vref_new - 1.1mV.
   The maximum value of Vref setting tolerance = Vref_new + 1.1mV. For n≤4.
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consectuive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefCA Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR12 OP[6].
12. Time from MRS command to increment or decrement more than one step size up a full range of Vref voltage within the same VrefCA range.
13. Applies when VRCG high current mode is not enabled, specified by MR13 OP[3] = 0.
14. Vref_time_weak covers all Vref(CA) Range and Value change conditions are applied to Vref_time_Short/Middle/Long.

## 2.27. DQ Vref Training

The DRAM internal DQ Vref specification parameters are voltage operating range, stepsize, Vref set tolerance, Vref step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for LPDDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure "Vref operating range (Vref.min, Vref.max)".

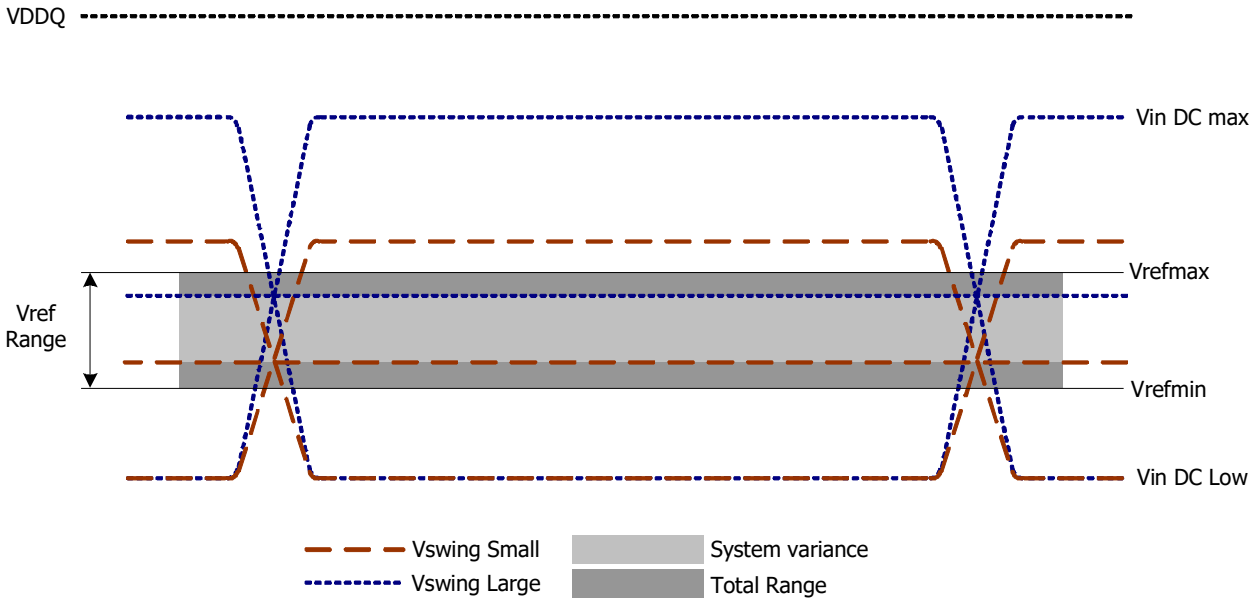



**Figure 91 - Vref operating range (Vref.min, Vref.max)**

The Vref stepsize is defined as the stepsize between adjacent steps. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainity is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

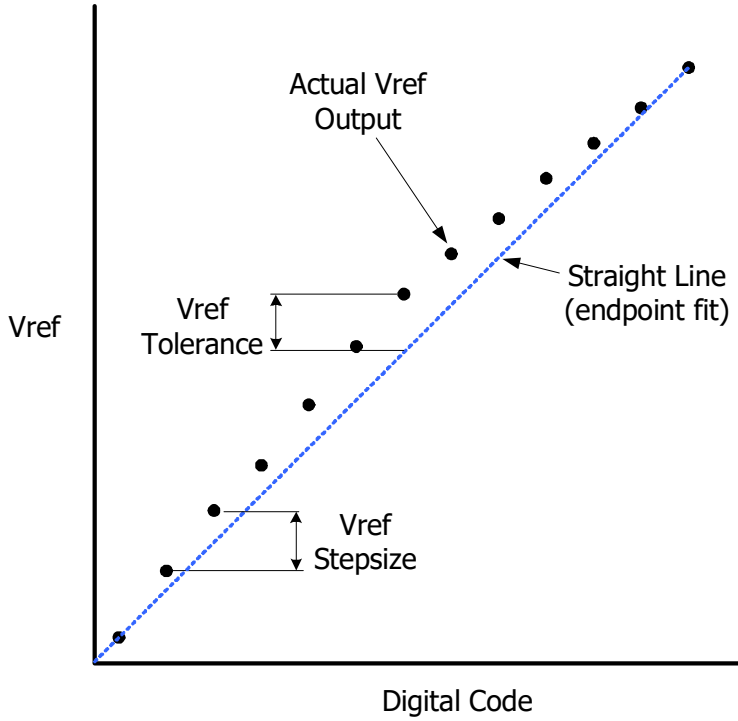



**Figure 92 - Example of Vref set tolerance (max case only shown) and stepsize**

The Vref increment/decrement step times are define by Vref_time-short, middle and long. The Vref_time-short, middle and Vref_-time-long is defined from TS to TE as shown in the Figure "Vref_time for short and long timing diagram" below where TE is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance(Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time TE as shown in Figure "Vref_time for short, middle, and long timing diagram". This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characerization.

Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.
Vref_time-Middle is at least 2 stepsizes increment/decrement change within the same VrefDQ range in Vref voltage.
Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range in Vref voltage.

TS - is referenced to MRS command clock
TE - is referenced to the Vref_val_tol

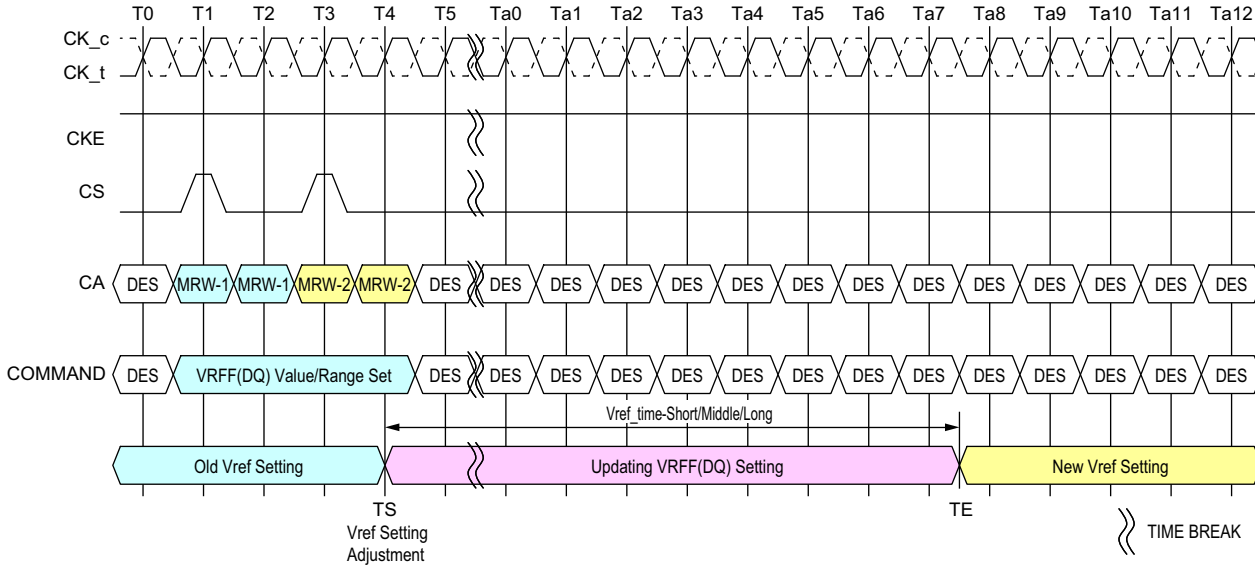



**Figure 93 - Vref_time for short and long timing diagram**

The MRW command to the mode register bits are as follows.

MR14 OP[5:0] : VREF(DQ) Setting
MR14 OP[6] : VREF(DQ) Range

The minimum time required between two Vref MRS commands is Vref_time-short for single step and Vref_time-Middle for a full voltage range step.

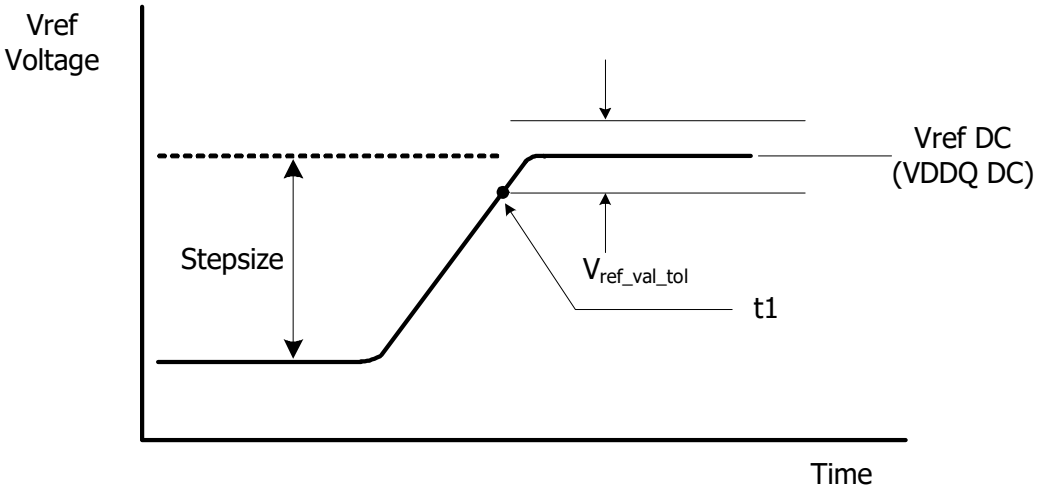



**Figure 94 - Vref step single stepsize increment case**

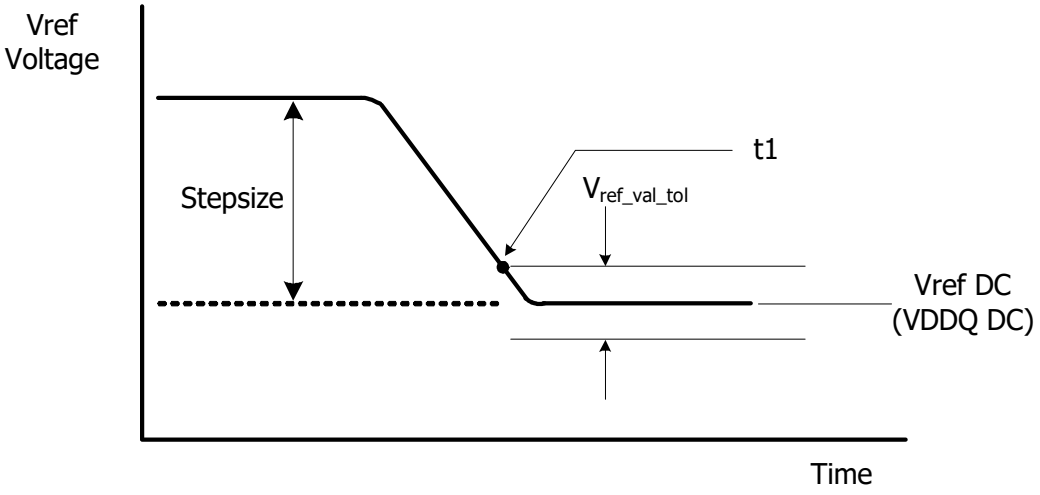



**Figure 95 - Vref step single stepsize decrement case**

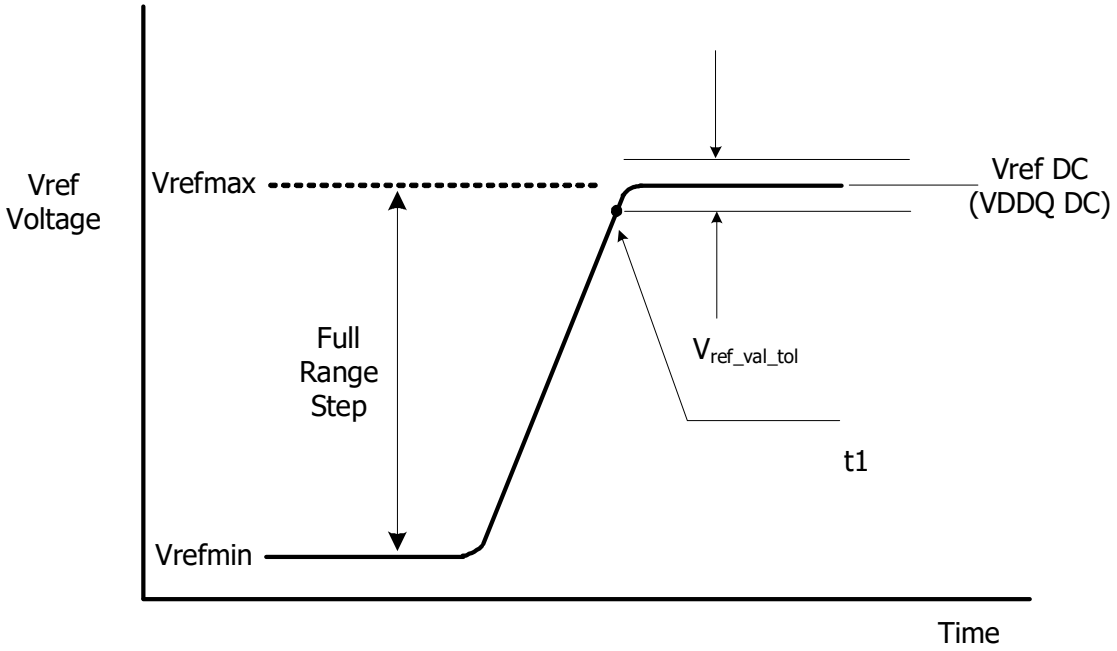



**Figure 96 - Vref full step from Vrefmin to Vrefmax case**

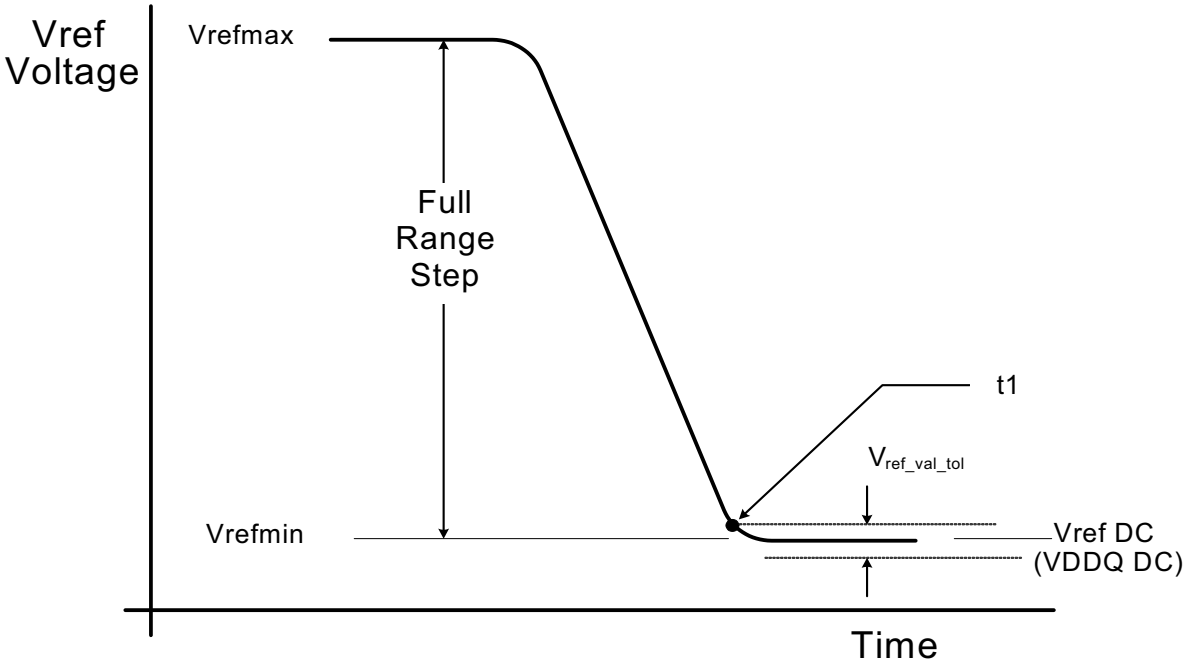



**Figure 97 - Vref full step from Vrefmax to Vrefmin case**

The table below contains the DQ internal vref specifications that will be characterized at the component level for compliance. The component level characterization method is tbd.

**Table 54 - DQ Internal Vref Specifications**

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Vref Max operating point Range[0] | Vref_max_R0 | - | - | 44.9% | VDDQ | 1,11 |
| Vref Min operating point Range[0] | Vref_min_R0 | 15% | - | - | VDDQ | 1,11 |
| Vref Max operating point Range[1] | Vref_max_R1 | - | - | 62.9% | VDDQ | 1,11 |
| Vref Min operating point Range[1] | Vref_min_R1 | 32.9% | - | - | VDDQ | 1,11 |
| Vref Step size | Vref_step | 0.50% | 0.60% | 0.70% | VDDQ | 2 |
| Vref Set Tolerance | Vref_set_tol | -11 | 0 | 11 | mV | 3,4,6 |
| | | -1.1 | 0 | 1.1 | mV | 3,5,7 |
| Vref Step Time | Vref_time-short | - | - | 100 | ns | 8 |
| | Vref_time-Middle | - | - | 200 | ns | 12 |
| | Vref_time-Long | - | - | 250 | ns | 9 |
| | Vref_time-weak | - | - | 1 | ms | 13,14 |
| Vref Valid tolerance | Vref_val_tol | -0.10% | 0.00% | 0.10% | VDDQ | 10 |

Notes

1. Vref DC voltage referenced to VDDQ_DC.
2. Vref stepsize increment/decrement range. Vref at DC level.
3. Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
4. The minimum value of Vref setting tolerance = Vref_new - 11mV.
   The maximum value of Vref setting tolerance = Vref_new + 11mV. For n>4.
5. The minimum value of Vref setting tolerance = Vref_new - 1.1mV.
   The maximum value of Vref setting tolerance = Vref_new + 1.1mV. For n≤4.
6. Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
7. Measured by recording the min and max values of the Vref output across 4 consectuive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
8. Time from MRS command to increment or decrement one step size for Vref.
9. Time from MRS command to increment or decrement Vrefmin to Vrefmax or Vrefmax to Vrefmin change across the VrefDQ Range in Vref voltage.
10. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
11. DRAM range 0 or 1 set by MR14 OP[6].
12. Time from MRS command to increment or decrement more than one step size up to a full range of Vref voltage withiin the same VrefDQ range.
13. Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.
14. Vref_time_weak covers all Vref(DQ) Range and Value change conditions are applied to Vref_time_Short/Middle/Long.

## 2.28. Command Bus Training

### 2.28.1. Command Bus Training for x16 mode

The LPDDR4-SDRAM command bus must be trained before enabling termination for high-frequency operation. LPDDR4 provides an internal VREF(CA) that defaults to a level suitable for un-terminated, low-frequency operation, but the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/ hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

Note: it is up to the system designer to determine what constitutes "low-frequency" and "high-frequency" based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the SDRAM before Command Bus Training is executed.

The LPDDR4-SDRAM die has a bond-pad (ODT-CA) for multi-rank operation. In a multi-rank system, the terminating rank should be trained first, followed by the non-terminating rank(s). See the ODT section for more information.

The LPDDR4-SDRAM uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1B (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4-SDRAM will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See note 6 in Figure 98 for more information on FSP-OP register sets). Upon training exit when CKE is driven HIGH, the LPDDR4-SDRAM will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the "known-good" state that was operating prior to training. The training values for VREF(CA) are not retained by the DRAM in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1B (Command Bus Training Mode Enabled).

2. After time tMRD, CKE may be set LOW, causing the LPDDR4-SDRAM to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode.
   A status of DQS_t, DQS_c, DQ and DMI are as follows, and DQ ODT state will be followed Frequency Set Point function except output pins.
   - DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by its toggling.
   - DQ[5:0] become input pins for setting VREF(CA) Level.
   - DQ[6] becomes a input pin for setting VREF(CA) Range.
   - DQ[7] and DMI[0] become input pins and their input level is Valid level or floating, either way is fine.
   - DQ[13:8] become output pins to feedback its capturing value via command bus by CS signal.
   - DQS_t[1], DQS_c[1],DMI[1] and DQ[15:14] become output pins or disable, it means that SDRAM may drive to a valid level or left floating.

3. At time tCAENT later, LPDDR4 SDRAM can accept to chage its VFREF(ca) Range and Value using input signals of DQS_t[0],

DQS_c[0] and DQ[6:0] from existing value that's setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQ signals is shown in the table below. At least one Vref CA setting is required before proceed to next training steps.

**Table 55 - Mapping of MR12 OP Code and DQ Numbers**

| | Mapping | | | | | | |
|---|---|---|---|---|---|---|---|
| MR12 OP code | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| DQ Number | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

4. The new VREF(CA) value must "settle" for time tVREF_LONG before attempting to latch CA information.

5. To verify that the receiver has the correct VREF(CA) setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

6. To exit Command Bus Training mode, drive CKE HIGH, and after time tVREF_LONG issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0B. After time tMRW the LPDDR4-SDRAM is ready for normal operation. After training exit the LPDDR4-SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training.

Command Bus Training may executed from IDLE, or Self Refresh states. When executing CBT within the Self Refresh state, the SDRAM must not be a power down state (i.e. CKE must be HIGH prior to training entry). Command Bus Training entry and exit is the same, regardless of the SDRAM state from which CBT is initiated.

### 2.28.1.1. Training Sequence for single-rank systems:

Note that an example shown here is assuming an initial low-frequency, no-terminating operating point, training a high-frequency, terminating operating point. The green text is low-frequency, magenta text is high-frequency. Any operating point may be trained from any known good operating point

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-OP[x], See note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
4. Drive CKE LOW, and change CK frequency to the high-frequency operating point.
5. Perform Command Bus Training ($V_{REF}$CA, CS, and CA).
6. Exit training, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
7. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained and you may proceed to other training or normal operation.

### 2.28.1.2. Training Sequence for multi-rank systems:

(Example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The green text is low-frequency, magenda text is high-frequency. Any operating point may be trained from any known good operating point)

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up highfrequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (VREFca, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (VREFca, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the SDRAM).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the highfrequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

### 2.28.1.3. Relation between CA input pin and DQ output pin

The relation between CA input pin and DQ out pin is shown in the following table.

**Table 56 - Mapping of CA input pin to DQ ouput pin**

| | Mapping | | | | | |
|---|---|---|---|---|---|---|
| CA Number | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |
| DQ Number | DQ13 | DQ12 | DQ11 | DQ10 | DQ9 | DQ8 |

### 2.28.1.4. Timing Diagram

The basic timing diagrams of Command Bus Training are shown in following figures.

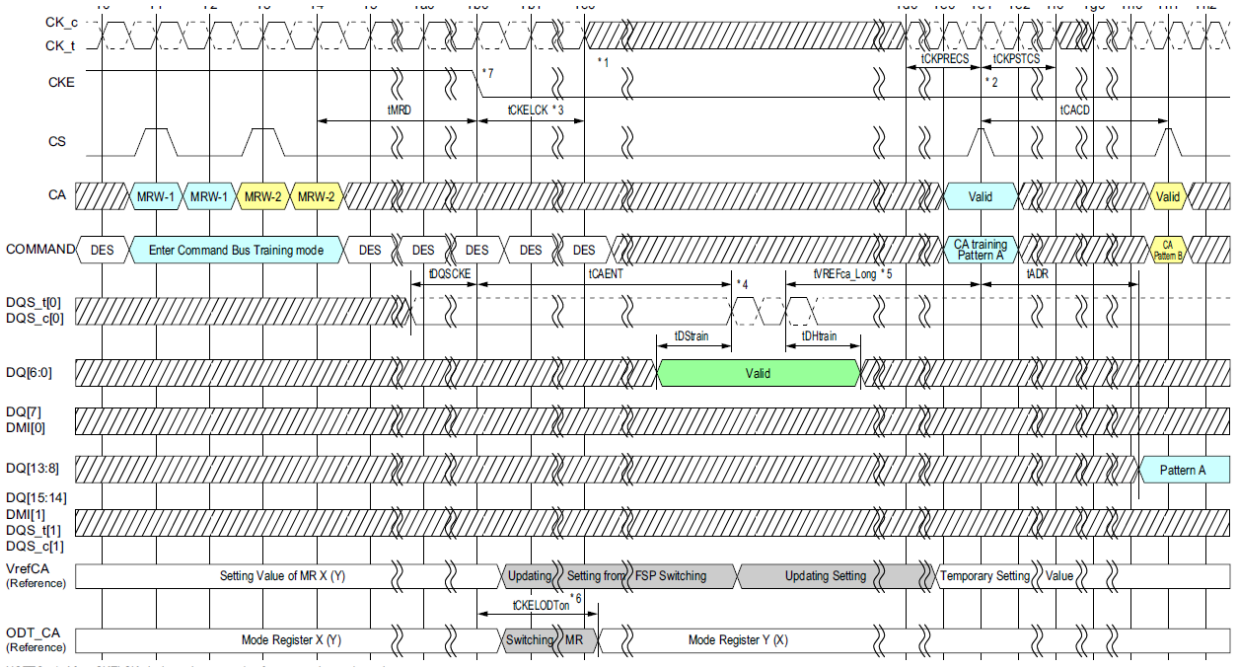



**Figure 98 - Entering Command Bus Training Mode and CA Training Pattern Input and Output**

Notes

1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS and tCKPSTCS.
3. Continue to Drive CK and Hold CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals. The captured value of DQ6:0 signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tVREFca_Long.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values.
   If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode. If the ODT_CA pad is bonded to Vss, ODT_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

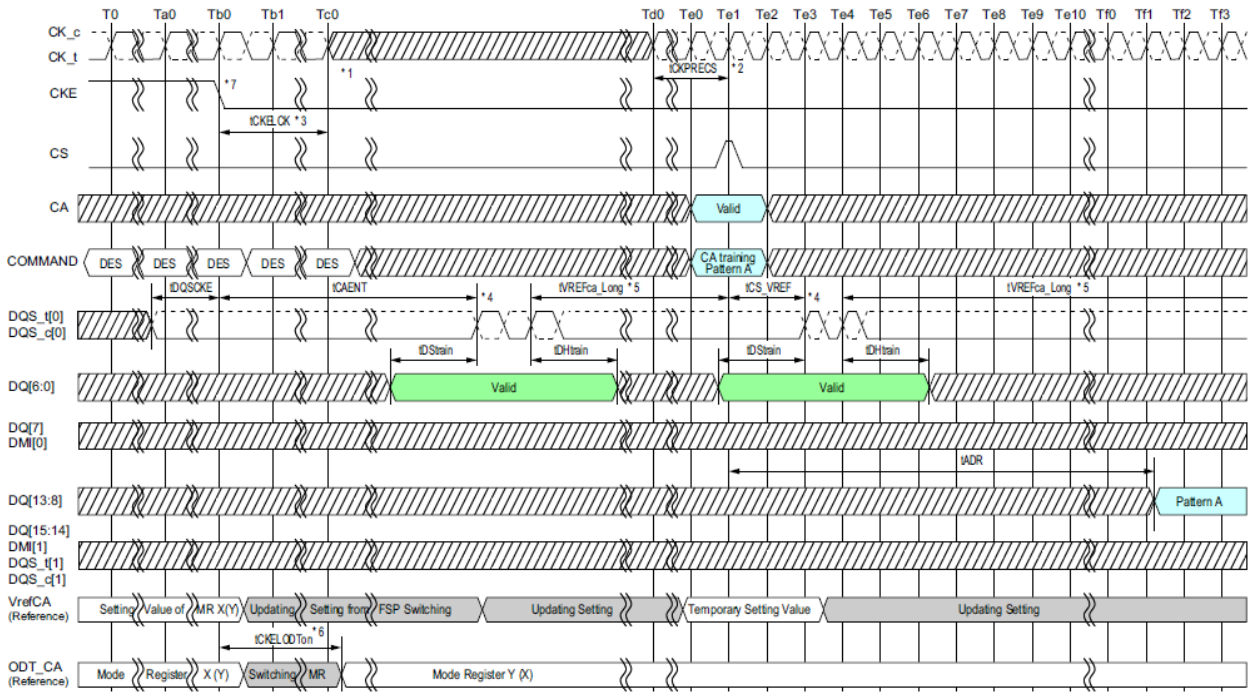



**Figure 99 - Consecutive VrefCA Value Update**

Notes

1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS.
3. Continue to Drive CK and Hold CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. DRAM may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals. The captured value of DQ6:0 signal level by each DQS edges are overwritten at any time and the DRAM updates its VREFca setting of MR12 temporary after time tVREFca_Long.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the SDRAM will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the SDRAM is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL/WL/nWR setting, etc., are set to the correct values.
   If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode. If the ODT_CA pad is bonded to Vss, ODT_CA termination will never enable for that die.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4-SDRAM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

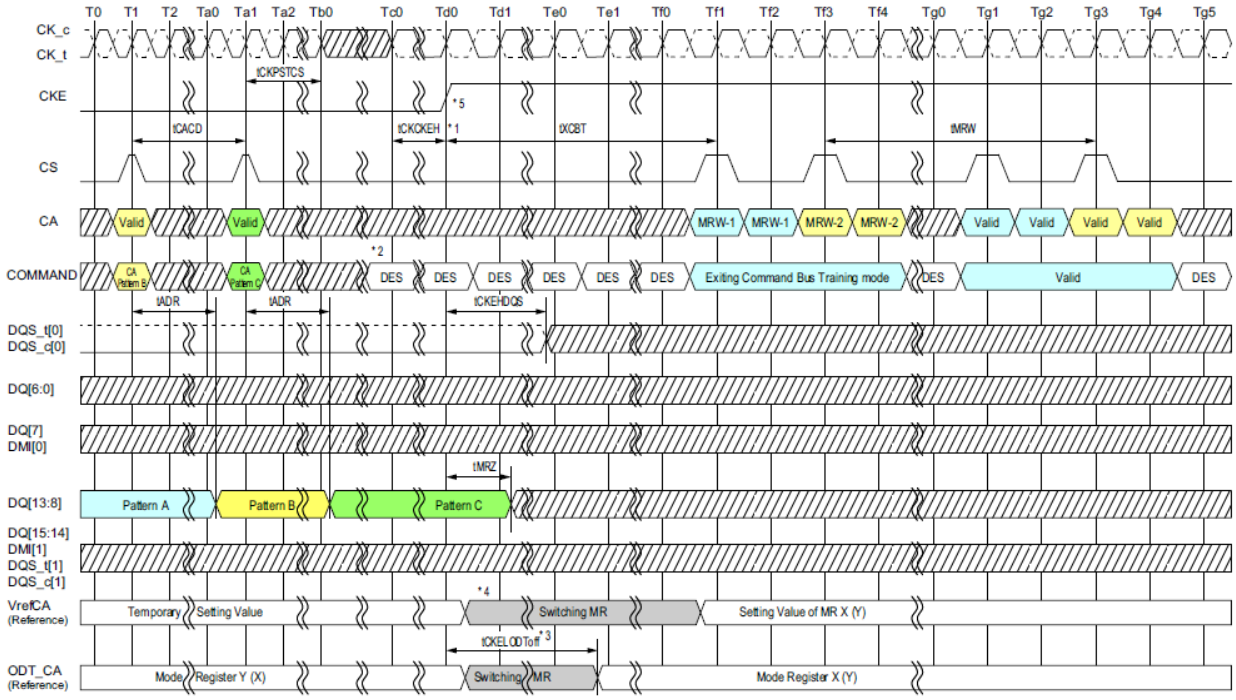



**Figure 100 - Exiting Command Bus Training Mode with Valid Command**

Notes

1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]). Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREF(CA) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

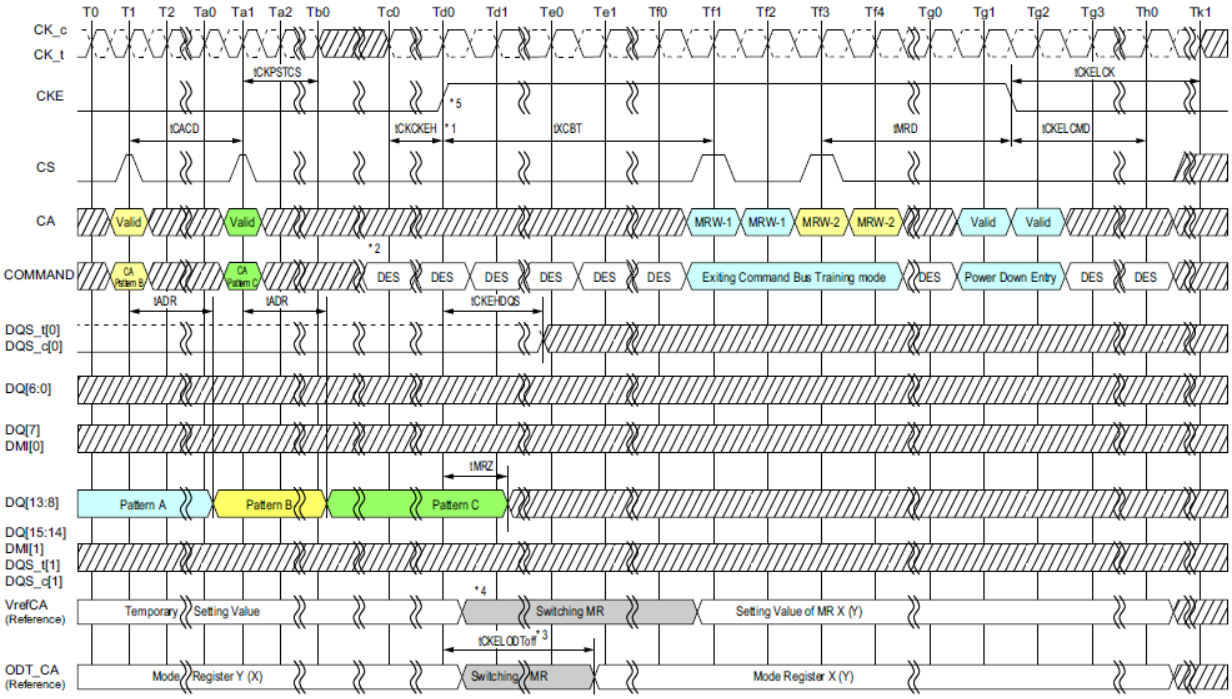



**Figure 101 - Exiting Command Bus Training Mode with Power Down Entry**

Notes

1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high. When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the SDRAM's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]). Example: If the SDRAM was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the SDRAM, and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREF(CA) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4-SDRAM will revert to the FSP in operation when Command Bus Training mode was entered.

### 2.28.1.5. Command Bus Training AC timing Table

**Table 57 - Command Bus Training Parameters**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Valid Clock Requirement after CKE Input low | tCKELCK | min | max(5ns, 5nCK) | | | | | | | | tCK | |
| Data Setup for $V_{REF}$ Training Mode | tDStrain | min | 2 | | | | | | | | ns | |
| Data Hold for$V_{REF}$ Training Mode | tDHtrain | min | 2 | | | | | | | | ns | |
| Asynchronous Data Read | tADR | max | 20 | | | | | | | | ns | |
| CA Bus Training Command to CA Bus Training Command Delay | tCACD | min | RU (tADR/tCK) | | | | | | | | tCK | 2 |
| Valid Strobe Requirement before CKE Low | tDQSCKE | min | 10 | | | | | | | | ns | 1 |
| First CA Bus Training Command Following CKE Low | tCAENT | min | 250 | | | | | | | | ns | |
| $V_{REF}$ Step Time – multiple steps | tVrefCA_long | max | 250 | | | | | | | | ns | |
| $V_{REF}$ Step Time – one step | tVrefCA_short | max | 80 | | | | | | | | ns | |
| Valid Clock Requirement before CS High | tCKPRECS | min | 2*tCK + tXP (tXP = max(7.5ns, 5nCK)) | | | | | | | | - | |
| Valid Clock Requirement after CS High | tCKPSTCS | min | max (7.5ns, 5nCK) | | | | | | | | - | |
| Minimum delay from CS to DQS toggle in command bus training | tCS_Vref | min | 2 | | | | | | | | tCK | |
| Minimum delay from CKE High to Strobe High Impedance | tCKEHDQS | min | 10 | | | | | | | | ns | |
| Valid Clock Requirement before CKE Input High | tCKCKEH | min | max(1.75ns,3nCK) | | | | | | | | tCK | |
| CA Bus Training CKE High to DQ Tri-state | tMRZ | min | 1.5 | | | | | | | | ns | |
| ODT turn-on Latency from CKE | tCKELODTon | min | 20 | | | | | | | | ns | |
| ODT turn-off Latency from CKE | tCKELODToff | min | 20 | | | | | | | | ns | |
| Exit Command Bus Training Mode to next valid command delay | tXCBT_Short | Min | Max(5nCK, 200ns) | | | | | | | | - | 3 |
| | tXCBT_Middle | Min | Max(5nCK, 200ns) | | | | | | | | - | 3 |
| | tXCBT_Long | Min | Max(5nCK, 200ns) | | | | | | | | - | 3 |

Notes

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

## 2.29. Frequency Set Point (FSP)

Frequency Set-Points allow the LPDDR4-SDRAM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an un-trained state which could result in a loss of communication to the DRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4-SDRAM's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include:

**Table 58 - Mode Register Function with two physical registers**

| MR# | Operand | Function | Note |
|---|---|---|---|
| MR1 | OP[2] | WR-PRE (WR Pre-amble Length) | 1 |
| | OP[3] | RD-PRE (RD Pre-amble Type) | |
| | OP[6:4] | nWR (Write-Recovery for Auto-Precharge commands) | |
| | OP[7] | PST (RD Post-Amble Length) | |
| MR2 | OP[2:0] | RL (Read latency) | |
| | OP[5:3] | WL (Write latency) | |
| | OP[6] | WLS (Write Latency Set) | |
| MR3 | OP[0] | PU-Cal (Pull-up Calibration Point) | 2 |
| | OP[1] | WR PST(WR Post-Amble Length) | |
| | OP[5:3] | PDDS (Pull-Down Drive Strength) | |
| | OP[6] | DBI-RD (DBI-Read Enable) | |
| | OP[7] | DBI-WR (DBI-Write Enable) | |
| MR11 | OP[2:0] | DQ ODT (DQ Bus Receiver On-Die-Termination) | |
| | OP[6:4] | CA ODT (CA Bus Receiver On-Die-Termination) | |
| MR12 | OP[5:0] | VREF(CA) (VREF(CA) Setting) | |
| | OP[6] | VR-CA (VREF(CA) Range) | |
| MR14 | OP[5:0] | VREF(dq) (VREF(dq) Setting) | |
| | OP[6] | VR(dq) (VREF(dq) Range) | |
| MR22 | OP[2:0] | SoC ODT (Controller ODT Value for VOH calibration) | |
| | OP[3] | ODTE-CK (CK ODT enabled for non terminating rank) | |
| | OP[4] | ODTE-CS (CS ODT enable for non-terminating rank) | |
| | OP[5] | ODTD-CA (CA ODT termination disable) | |

Notes
1. Supporting the two physical registers for Burst Length: MR1 OP[1:0] is optional.
   Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.
2. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.

See Mode Register Definition for more details.

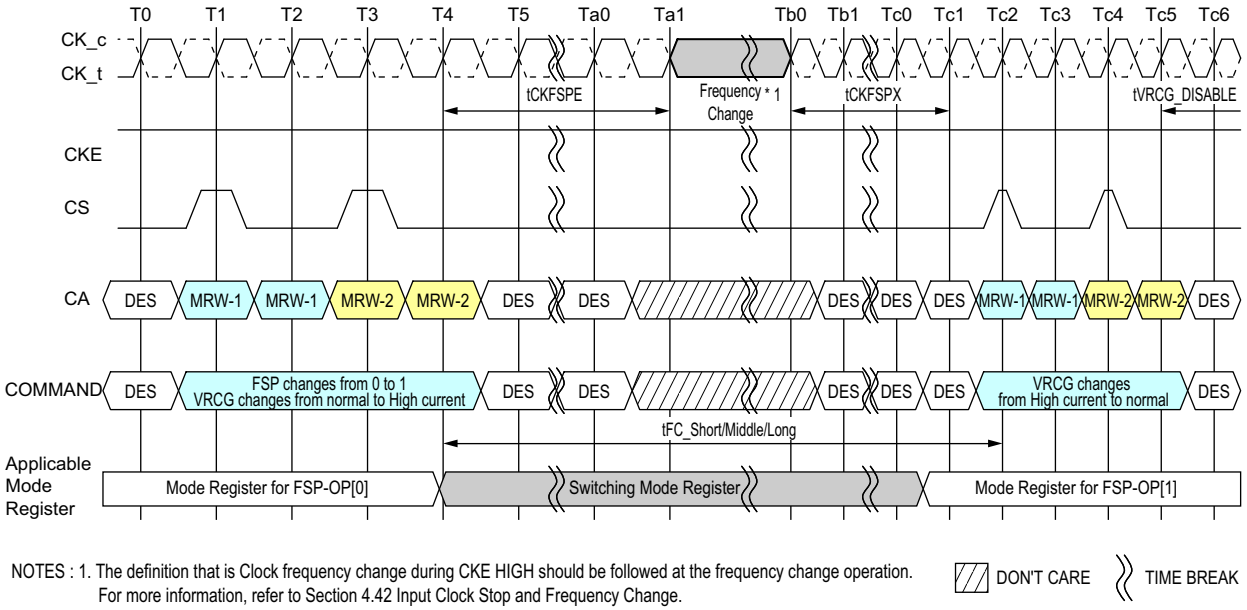
Following table shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

| Function | MR# & Operand | Data | Operation | Note |
|---|---|---|---|---|
| FSP-WR | MR13 OP[6] | 0 (Default) | Data write to Mode Register N for FSP-OP[0] by MRW Command.<br>Data read from Mode Register N for FSP-OP[0] by MRR Command. | 1 |
| | | 1 | Data write to Mode Register N for FSP-OP[1] by MRW Command.<br>Data read from Mode Register N for FSP-OP[1] by MRR Command. | |
| FSP-OP | MR13 OP[7] | 0 (Default) | DRAM operates with Mode Register N for FSP-OP[0] setting. | 2 |
| | | 1 | DRAM operates with Mode Register N for FSP-OP[1] setting. | |

Notes
1. FSP-WR stands for Frequency Set Point Write/Read.
2. FSP-OP stands for Frequency Set Point Operating Point.

### 2.29.1. Frequency Set Point update timing

The Frequency set point update timing is shown in the timing diagram below. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time(tFC) is satisfied. VRCG can be changed into Normal Operation mode via MR13 OP[3].




NOTES : 1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to Section 4.42 Input Clock Stop and Frequency Change.

**Figure 102 - Frequency Set Point Switching Timing**

**Table 59 - Frequency Set Point AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Frequency Set Point Switching Time | tFC_Short | min | 200 | | | | | | | | ns | 1 |
| | tFC_Middle | min | 200 | | | | | | | | ns | 1 |
| | tFC_Long | min | 250 | | | | | | | | ns | 1 |
| Valid Clock Requirement after entering FSP change | tCKFSPE | min | max(7.5ns, 4nCK) | | | | | | | | - | |
| Valid Clock Requirement before 1st valid command after FSP change | tCKFSPX | min | max(7.5ns, 4nCK) | | | | | | | | - | |

Notes

1. Frequency Set Point Switching Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table "tFC value maping". Additionally change of Frequency Set Point may affect VREF(DQ) setting. Setting time of VREF(DQ) level is same as VREF(CA) level.

**Table 60 - tFC value mapping**

| Application | Step size | | Range | |
|---|---|---|---|---|
| | From FSP-OP0 | To FSP-OP1 | From FSP-OP0 | To FSP-OP1 |
| tFC_Short | Base | A single step increment/decrement | Base | No Change |
| tFC_Middle | Base | Two or more steps increment/decrement | Base | No Change |
| tFC_Long | - | - | Base | Change |

Notes

1. As well as from FSP-OP1 to FSP-OP0

**Table 61 - tFC value mapping example**

| Case | From/To | FSP-OP MR13 OP[7] | VREF(CA) setting: MR12: OP[5:0] | VREF(CA) Range: MR12 OP[6] | Application | Note |
|---|---|---|---|---|---|---|
| 1 | From | 0 | 001100 | 0 | tFC_Short | 1 |
| | To | 1 | 001101 | 0 | | |
| 2 | From | 0 | 001100 | 0 | tFC_Middle | 2 |
| | To | 1 | 001110 | 0 | | |
| 3 | From | 0 | Don't care | 0 | tFC_Long | 3 |
| | To | 1 | Don't care | 1 | | |

Notes

1. A single step size increment/decrement for VREF(CA) Setting Value.
2. Two or more step size increment/decrement for VREF(CA) Setting Value.
3. VREF(CA) Range is changed. In tis case changing VREF(CA) Setting doesn't affect tFC value.

The LPDDR4-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4-SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure Figure 103). See the section Command Bus Training for more details on this training mode.

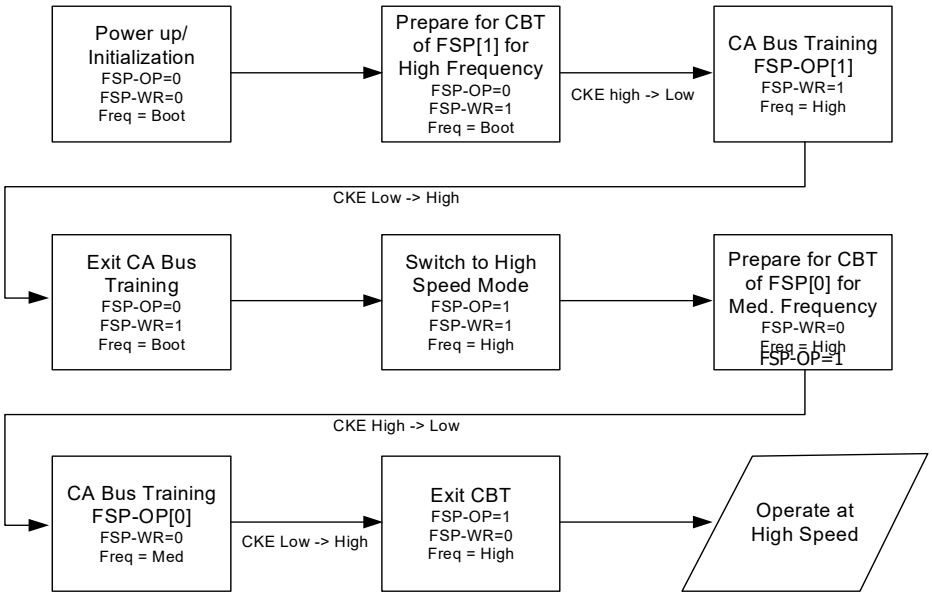



**Figure 103 - Training Two Frequency Set Points**

Once both Frequency Set Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (figure below)

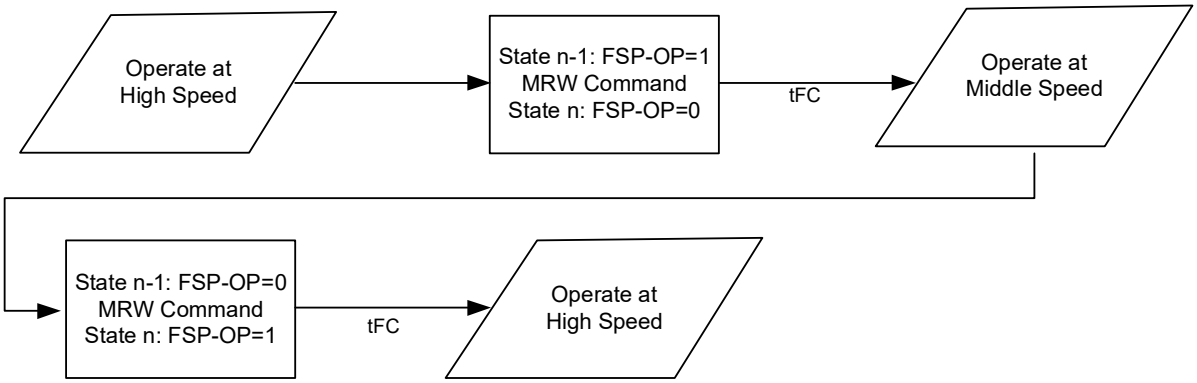



**Figure 104 - Switching between two trained Frequency Set Points**

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the Vref-CA calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure below).

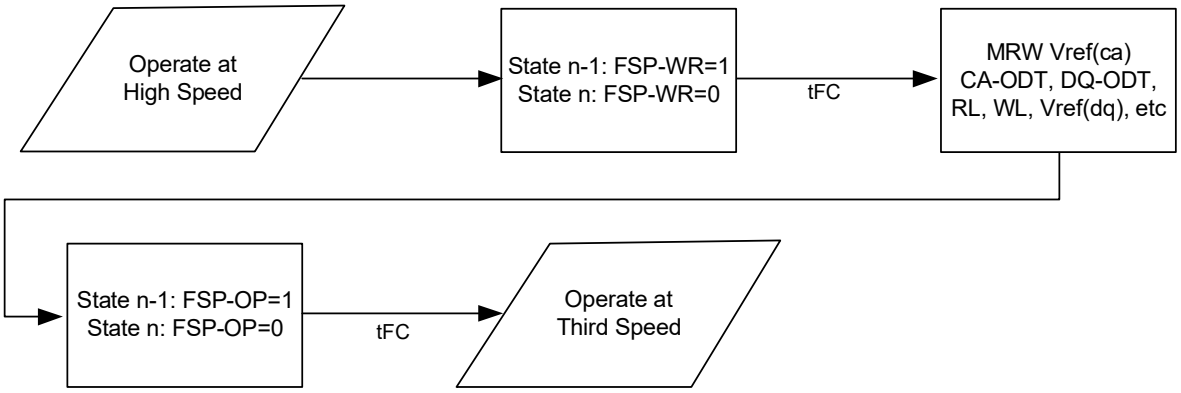



**Figure 105 - Switching to a third trained Frequency Set Point**

## 2.30. Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the LPDDR4 SDRAM provides a write-leveling feature to compensate CK-to-DQS timing skew affecting timing parameters such as tDQSS, tDSS, and tDSH. The DRAM samples the clock state with the rising edge of DQS signals, and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS_t/DQS_c[0], and DQ[15:8] for DQS_t/DQS_c[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write-leveling entry/exit is independent between channels.

The LPDDR4 SDRAM enters into write-leveling mode when mode register MR2-OP[7] is set HIGH. When entering write-leveling mode, the state of the DQ pins is undefined. During write-leveling mode, only DESELECT commands are allowed, or a MRW command to exit the write-leveling operation. Depending on the absolute values of tQSL and tQSH in the application, the value of tDQSS may have to be better than the limits provided in the chapter "AC Timing Parameters" in order to satisfy the tDSS and tDSH specification. Upon completion of the write-leveling operation, the DRAM exits from write-leveling mode when MR2-OP[7] is reset LOW.

Write Leveling should be performed before Write Training (DQS2DQ Training).

Note 1 As of publication of this document, under discussion by the formulating committee.

### 2.30.1. Write Leveling Procedure

1. Enter into Write-leveling mode by setting MR2-OP[7]=1,
2. Once entered into Write-leveling mode, DQS_t must be driven LOW and DQS_c HIGH after a delay of tWLDQSEN.
3. Wait for a time tWLMRD before providing the first DQS signal input. The delay time tWLMRD(MAX) is controller-dependent.
4. DRAM may or may not capture first rising edge of DQS_t due to an unstable first risign edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal during Write Training Mode.
   The captured clock level by each DQS edges are overwritten at any time and the DRAM provides asynchronous feedback on all the DQ bits after time tWLO.
5. The feedback provided by the DRAM is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat step 4 through step 5 until the proper DQS_t/DQS_c delay is established.
7. Exit from Write-leveling mode by setting MR2-OP[7]=0.

A Write Leveling timing example is shown in figure below.

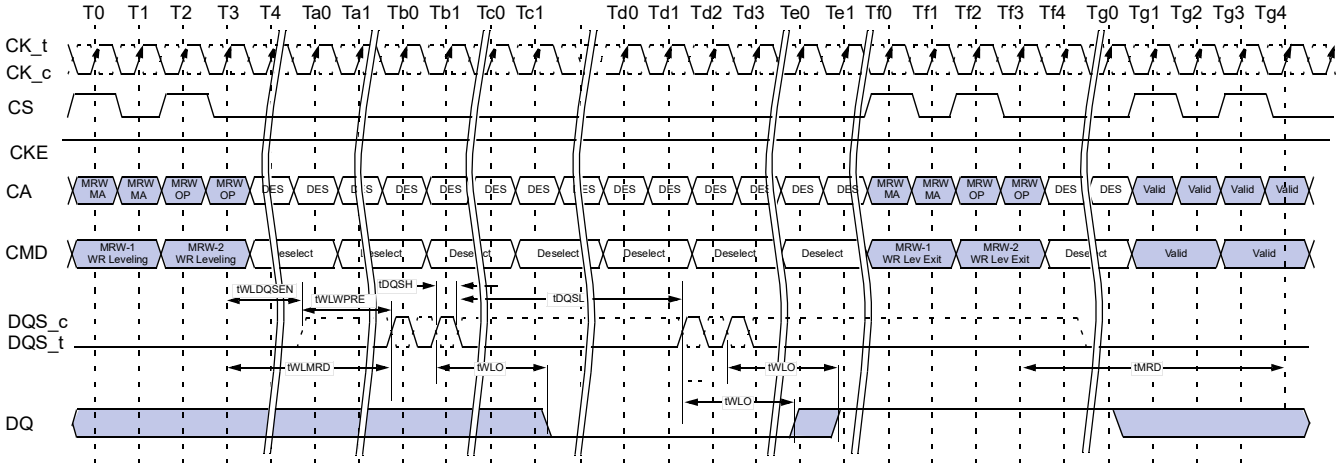



**Figure 106 - Write Leveling Timing, tDQSL(max)**

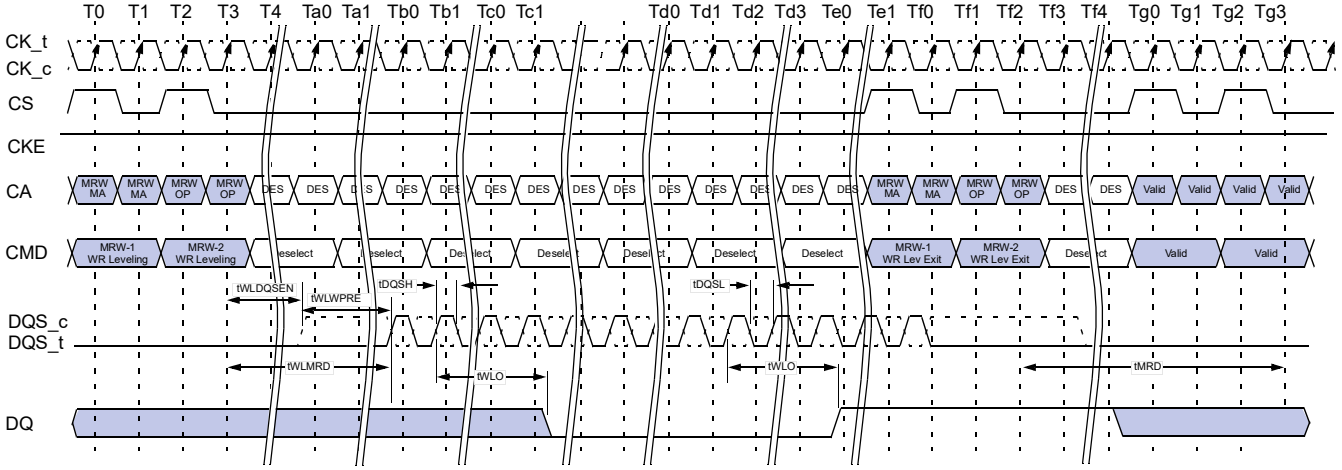
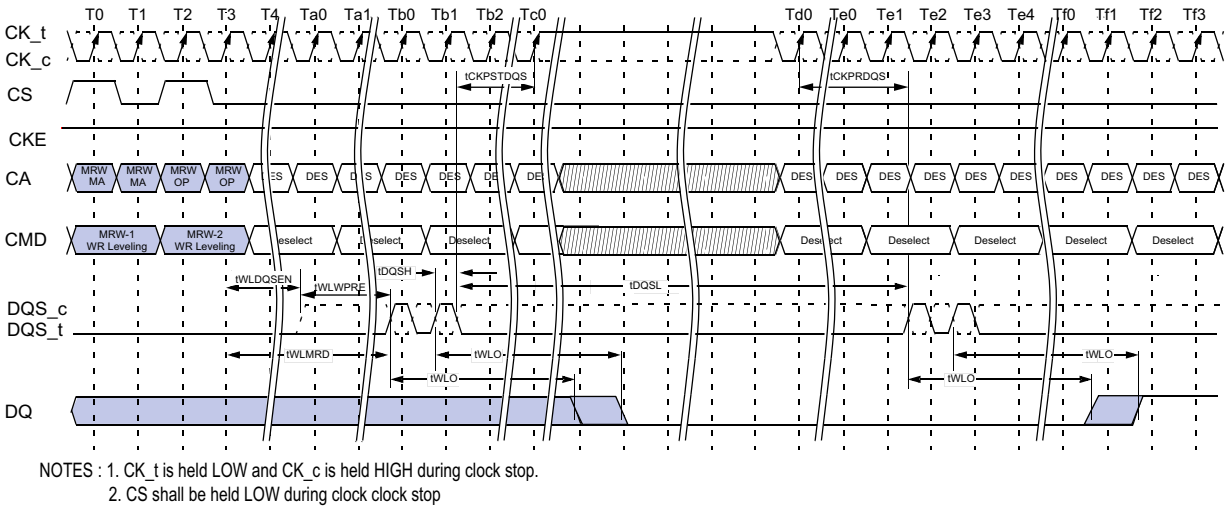



**Figure 107 - Write Leveling Timing, tDQSL(min)**

### 2.30.2. Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during Write Leveling mode.
The Frequency stop or change timing is shown in Figure below




NOTES : 1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. CS shall be held LOW during clock clock stop

**Figure 108 - Clock Stop and Timing during Write Leveling**

**Table 62 - Write Leveling Timing Parameters**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQS_t/DQS_c delay after write leveling mode is programmed | tWLDQSEN | min | 20 | | | | | | | | tCK | |
| Write preamble for Write Leveling | tWLWPRE | min | 20 | | | | | | | | tCK | |
| First DQS_t/DQS_c edge after write leveling mode is programmed | tWLMRD | min | 40 | | | | | | | | tCK | |
| Write leveling output delay | tWLO | min | 0 | | | | | | | | ns | |
| | | max | 20 | | | | | | | | | |
| Mode register set command delay | tMRD | min | max(14ns, 10nCK) | | | | | | | | ns | |
| Valid Clock Requirement before DQS Toggle | tCKPRDQS | min | max(7.5ns, 4nCK) | | | | | | | | - | |
| Valid Clock Requirement after DQS Toggle | tCKPSTDQS | min | max(7.5ns, 4nCK) | | | | | | | | - | |

### 2.30.3. Write Leveling Setup and Hold Time

**Table 63 - Write Leveling Setup and Hold Time**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Write leveling hold time | tWLH | min | 150 | 150 | 150 | 100 | 100 | 75 | 75 | 50 | ps |
| Write leveling setup time | tWLS | min | 150 | 150 | 150 | 100 | 100 | 75 | 75 | 50 | ps |
| Write leveling invalid window | tWLIVW | min | 240 | 240 | 240 | 160 | 160 | 120 | 120 | 90 | ps |

Notes
1. In addition to the traditional setup and hold time specifications above, there is value in a input valid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
2. tWLIVW is defined in a similar manner to tdIVW_Total, except that here it is a DQS input valid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling input valid window.

The DQS input mask for timing with respect to CK is shown in the following figure. The "total" mask (TdiVW_total) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

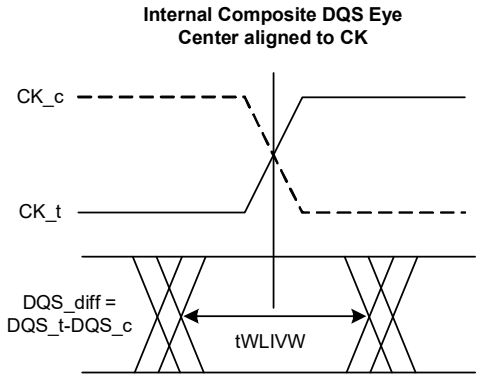



**Figure 109 - DQS_t/DQS_c and CK_t/CK_c at DRAM Latch**

## 2.31. RD DQ Calibration

### 2.31.1. RD DQ Calibration for x16 mode

LPDDR4 devices feature a RD DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. RD DQ Calibration is initiated by issuing a MPC [RD DQ Calibration] command followed by a CAS-2 command, cause the LPDDR4-SDRAM to drive the contents of MR32 followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

#### 2.31.1.1. RD DQ Calibration Training Procedure

The procedure for executing RD DQ Calibration is:

- Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1)
  o Optionally this step could be skipped to use the default patterns
  - MR32 default = 5Ah
  - MR40 default = 3Ch
  - MR15 default = 55h
  - MR20 default = 55h

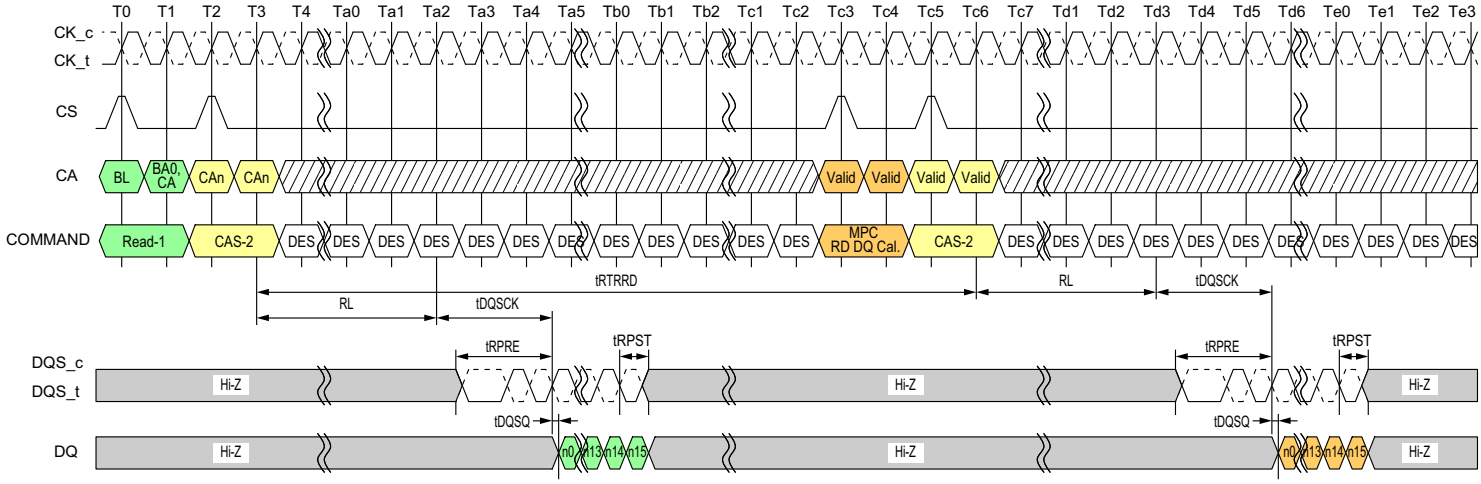
- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command
  o Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins
  o The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit (see Tabel Below)
  o Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
  o The MPC-1 [RD DQ Calibration] command can be issued every tCCD seamlessly, and tRTRRD delay is required between Array Read command and the MPC-1 [RD DQ Calibration] command as well the delay required between the MPC-1 [RD DQ Calibration] command and an array read.
  o The operands received with the CAS-2 command must be driven LOW

- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF with CKE high

**Table 64 - Invert Mask Assignments**

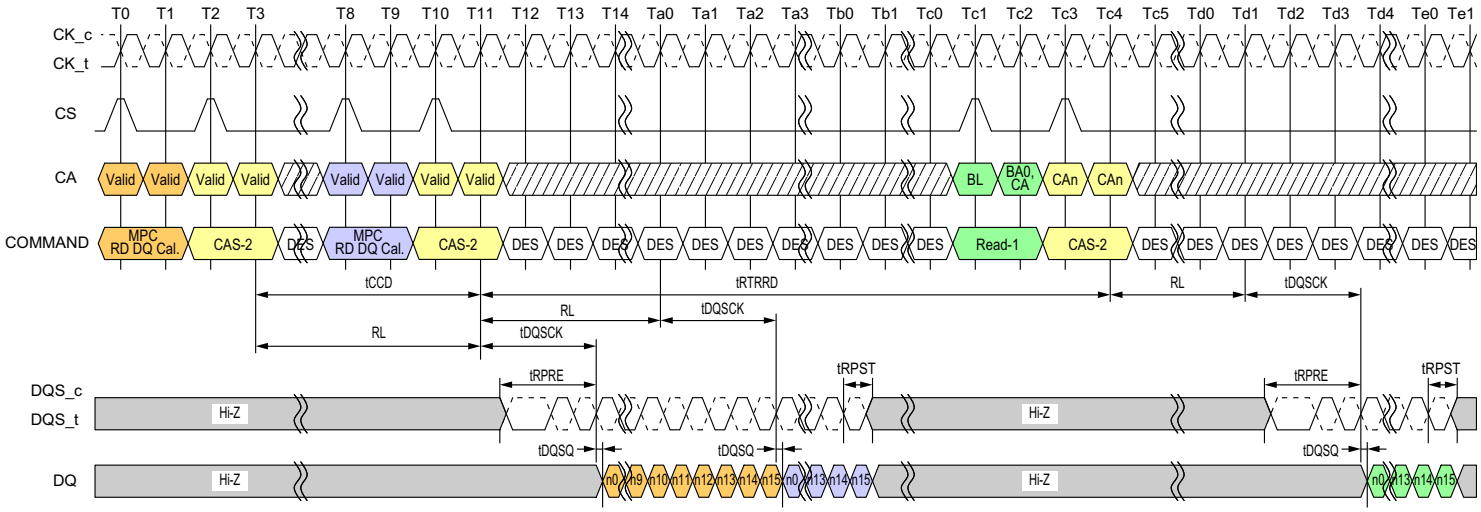
| Pin | DQ0 | DQ1 | DQ2 | DQ3 | DMI0 | DQ4 | DQ5 | DQ6 | DQ7 |
|---|---|---|---|---|---|---|---|---|---|
| MR15 | OP0 | OP1 | OP2 | OP3 | N/A | OP4 | OP5 | OP6 | OP7 |

| Pin | DQ8 | DQ9 | DQ10 | DQ11 | DMI1 | DQ12 | DQ13 | DQ14 | DQ15 |
|---|---|---|---|---|---|---|---|---|---|
| MR20 | OP0 | OP1 | OP2 | OP3 | N/A | OP4 | OP5 | OP6 | OP7 |




NOTES : 1. Read-1 to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.
Timing from Read-1 to MPC [RD DQ Calibration] command is tRTRRD.
2. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
3. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 110 - DQ Read Training Timing: Read to Read DQ Calibration**




NOTES : 1. MPC [RD DQ Calibration] to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.
2. MPC [RD DQ Calibration] to Read-1 Operation is shown as an example of command-to-command timing.
3. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
4. Seamless MPC [RD DQ Calibration] commands may be executed by repeating the command every tCCD time.
5. Timing from MPC [RD DQ Calibration] command to Read-1 is tRTRRD.
6. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
7. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 111 - DQ Read Training Timing: Read DQ Cal. to Read DQ Cal. / Read**

### 2.31.1.2. DQ Read Training Example

An example of MPC [RD DQ Calibration] output is shown in Table "MPC [RD DQ Calibration] Bit Ordering and Inversion Example". This shows the 16-bit data pattern that will be driven on each DQ when one DQ Read Training command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

**Table 65 - MPC [RD DQ Calibration] Bit Ordering and Inversion Example**

| Pin | | Bit sequence -> | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Invert? | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DQ0 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ1 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ2 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ3 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI0 | Never | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ4 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ5 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ6 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ7 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ8 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ9 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ10 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ11 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI1 | Never | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ12 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ13 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ14 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ15 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

Notes

1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when RD DQ Calibration is initiated via a MPC-1 [RD DQ Calibration] command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111 ®.
2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.3. DMI[1:0] outputs status follows Table below.
3. DMI [1:0] outputs status follows Table 66.
4. No Data Bus Inversion (DBI) function is enacted during RD DQ Calibration, even if DBI is enabled in MR3-OP[6].

**Table 66 - MR Setting vs. DMI Status**

| DM Function MR13 OP[5] | Write DBIdc Function MR3 OP[7] | Read DBIdc Function MR3 OP[6] | DMI Status |
|---|---|---|---|
| 1: Disable | 0: Disable | 0: Disable | Hi-Z |
| 1: Disable | 1: Enable | 0: Disable | The data pattern is transmitted |
| 1: Disable | 0: Disable | 1: Enable | The data pattern is transmitted |
| 1: Disable | 1: Enable | 1: Enable | The data pattern is transmitted |
| 0: Enable | 0: Disable | 0: Disable | The data pattern is transmitted |
| 0: Enable | 1: Enable | 0: Disable | The data pattern is transmitted |
| 0: Enable | 0: Disable | 1: Enable | The data pattern is transmitted |
| 0: Enable | 1: Enable | 1: Enable | The data pattern is transmitted |

### 2.31.1.3. MPC of Read DQ Calibration after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the MPC of Read DQ Calibration command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the Read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

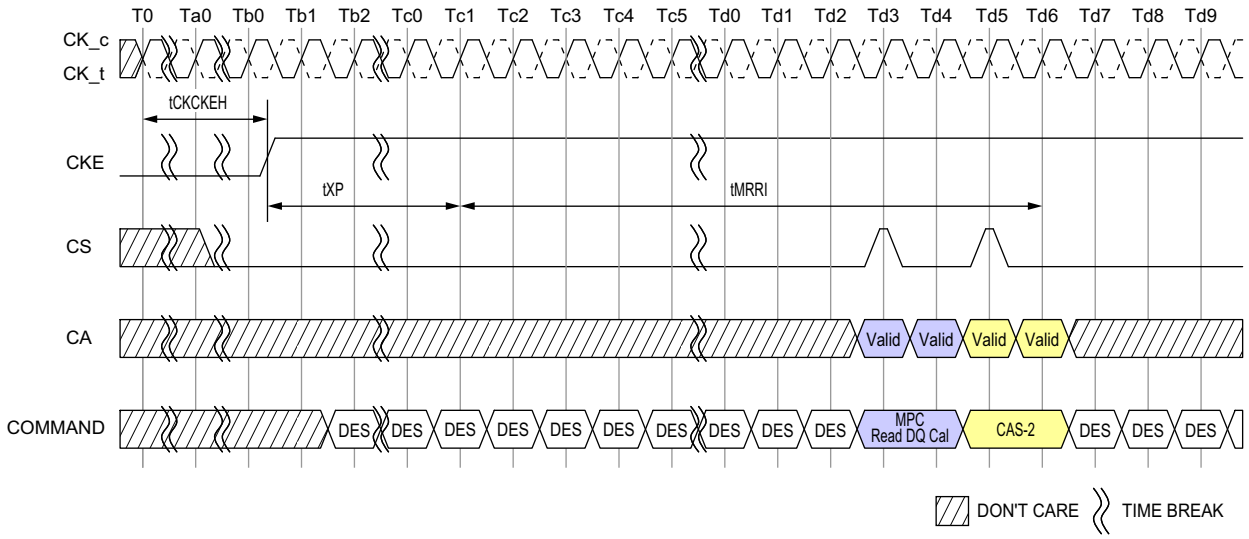



**Figure 112 - MPC Read DQ Calibration Following Power-Down State**

## 2.32. DQS-DQ Training

The LPDDR4-SDRAM uses an un-matched DQS-DQ path to enable high speed performance and save power in the DRAM. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the Data eye. The SDRAM DQ receiver is located at the DQ pad, and has a shorter internal delay in the SDRAM than does the DQS signal. The SDRAM DQ receiver will latch the data present on the DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the Data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available in LPDDR4:

- Command-based FIFO WR/RD with user patterns
- A internal DQS clock-tree oscillator, to determine the need for, and the magnitude of, required training.

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if OP6 is set LOW then the DRAM will perform a NOP command. When OP6 is set HIGH, then OP5:0 enable training functions or are reserved for future use (RFU). MPC commands that initiate a Read FIFO, READ DQ Calibration or Write FIFO to the SDRAM must be followed immediately by a CAS-2 command. See "Multi Purpose Command (MPC) Definition" for more information.

To perform Write Training, the controller can issue a MPC [Write DQ FIFO] command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a Write DQ FIFO. Timings for MPC [Write DQ FIFO] are identical to a Write command, with WL (Write Latency) timed from the 2nd rising clock edge of the CAS-2 command. Up to 5 consecutive MPC [Write DQ FIFO] commands with user defined patterns may be issued to the SDRAM to store up to 80 values (BL16 x5) per pin that can be read back via the MPC [Read DQ FIFO] command. Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the MPC [Write DQ FIFO] command, the data can be read back with the MPC [Read DQ FIFO] command and results compared with "expect" data to see if further training (DQ delay) is needed. MPC [Read DQ FIFO] is initiated by issuing a MPC command with OP[6:0] set as described in the MPC Definition section, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC [Read DQ FIFO] command are identical to a Read command, with RL (Read Latency) timed from the 2nd rising clock edge of the CAS-2 command.

Read DQ FIFO is non-destructive to the data captured in the FIFO, so data may be read continuously until it is either overwritten by a Write DQ FIFO command or disturbed by CKE LOW or any of the following commands; Write, Masked Write, Read, Read DQ Calibration and a MRR. If fewer than 5 Write DQ FIFO commands were executed, then unwritten registers will have un-defined (but valid) data when read back.

The following command about MRW is only allowed from MPC [Write DQ FIFO] command to MPC [Read DQ FIFO].
Allowing MRW command is for OP[7]:FSP-OP, OP[6]:FSP-WR and OP[3]:VRCG of MR13 and MR14. And the rest of MRW command is prohibited.

For example: If 5 Write DQ FIFO commands are executed sequentially, then a series of Read DQ FIFO commands will read valid data from FIFO[0], FIFO[1]….FIFO[4], and will then wrap back to FIFO[0] on the next Read DQ FIFO.

On the other hand, if fewer than 5 Write DQ FIFO commands are executed sequentially (example=3), then a series of Read DQ FIFO

commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two Read DQ FIFO commands will return un-defined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

### 2.32.1. FIFO Pointer Reset and Synchronism

The Write DQ FIFO pointer is reset under the following conditions:

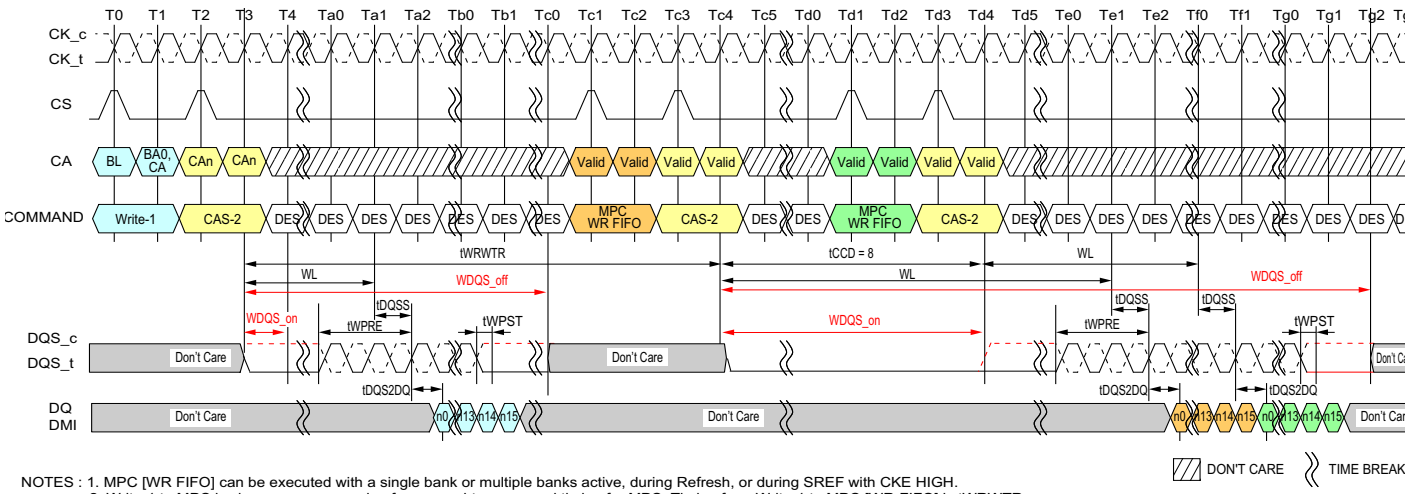
- Power-up initialization
- RESET_n asserted
- Power-down entry
- Self Refresh Power-Down entry

The MPC [Write DQ FIFO] command advances the WR-FIFO pointer, and the MPC [Read DQ FIFO] advances the RD-FIFO pointer. Also any normal (non-FIFO) Read Operation (RD, RDA) advances both WR-FIFO pointer and RD-FIFO pointer. Issuing (non-FIFO) Read Operation command is inhibited during Write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

**b=a+(n*c)**

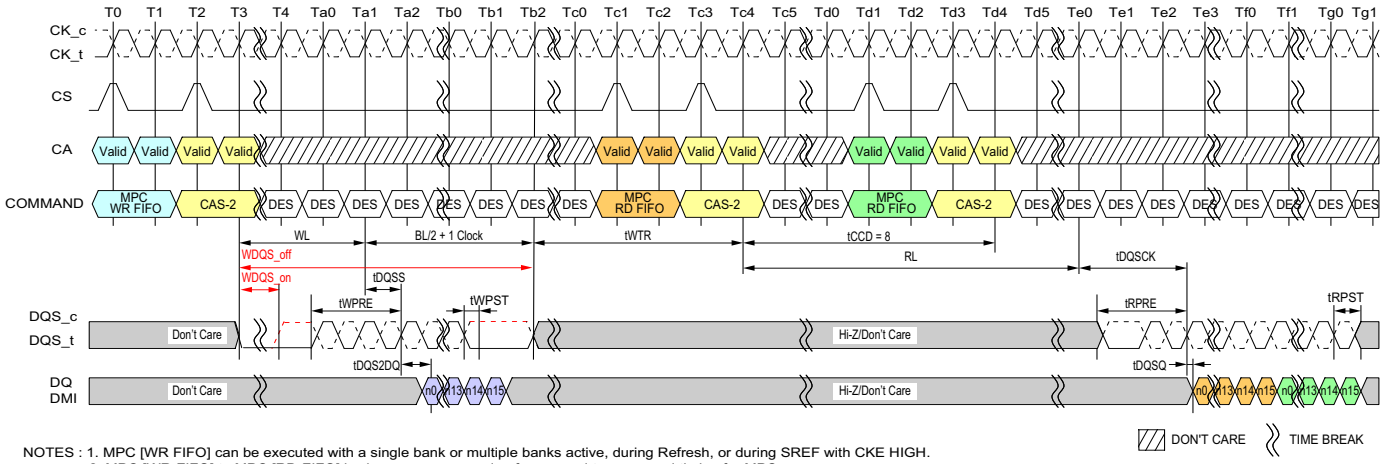
Where:

'a' is the number of MPC [Write DQ FIFO] commands
'b' is the number of MPC [Read DQ FIFO] commands
'c' is the FIFO depth (=5 for LPDDR4)
'n' is a positive integer, ≥ 0



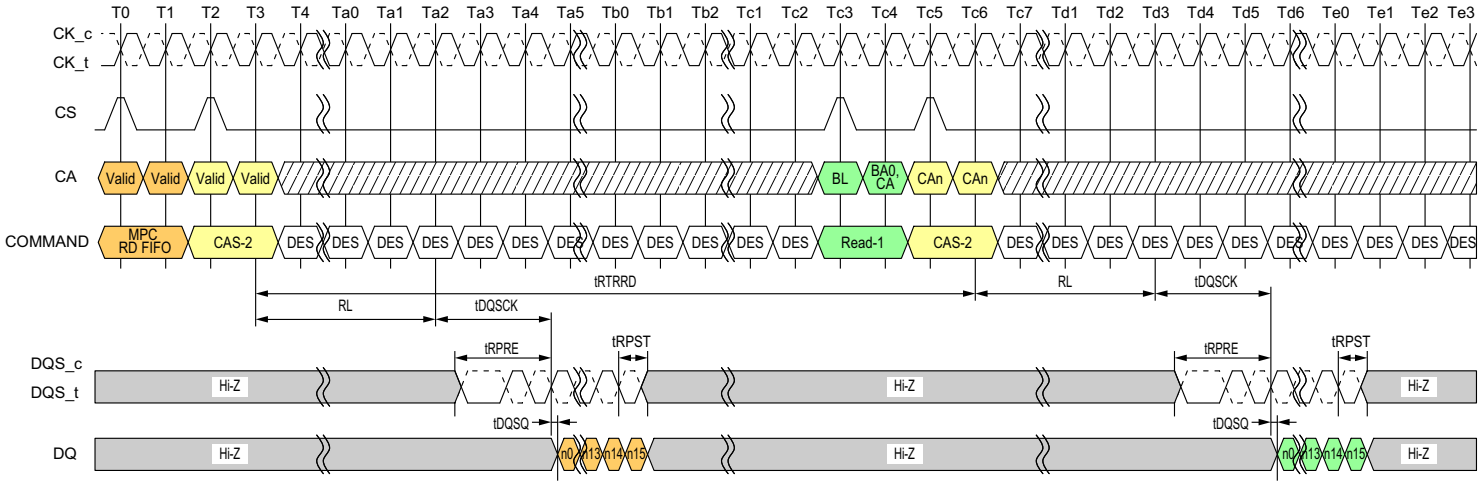

NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.
The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
7. To avoid corrupting the FIFO contents, MPC [RD-FIFO] must immediately follow MPC [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR.
8. BL = 16, Write Postamble = 0.5nCK
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 113 - Write to MPC [Write FIFO] Operation Timing**



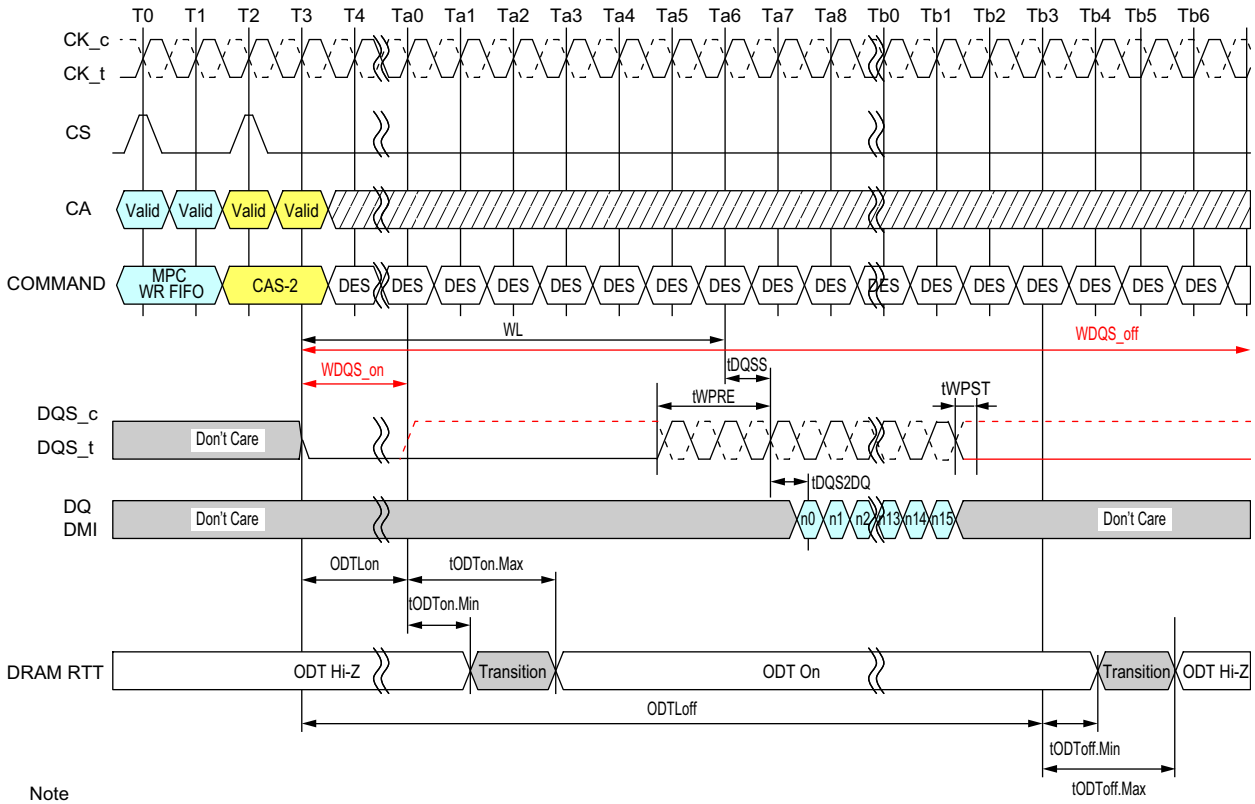

NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR-FIFO] to MPC [RD-FIFO] is shown as an example of command-to-command timing for MPC.
Timing from MPC [WR-FIFO] to MPC [RD-FIFO] is specified in the command-to-command timing table.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
8. BL = 16, Write Postamble = 0.5nCK, Read Preamble: Toggle, Read Postamble: 0.5nCK
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 114 - MPC [Write FIFO] to MPC [Read FIFO] Timing**



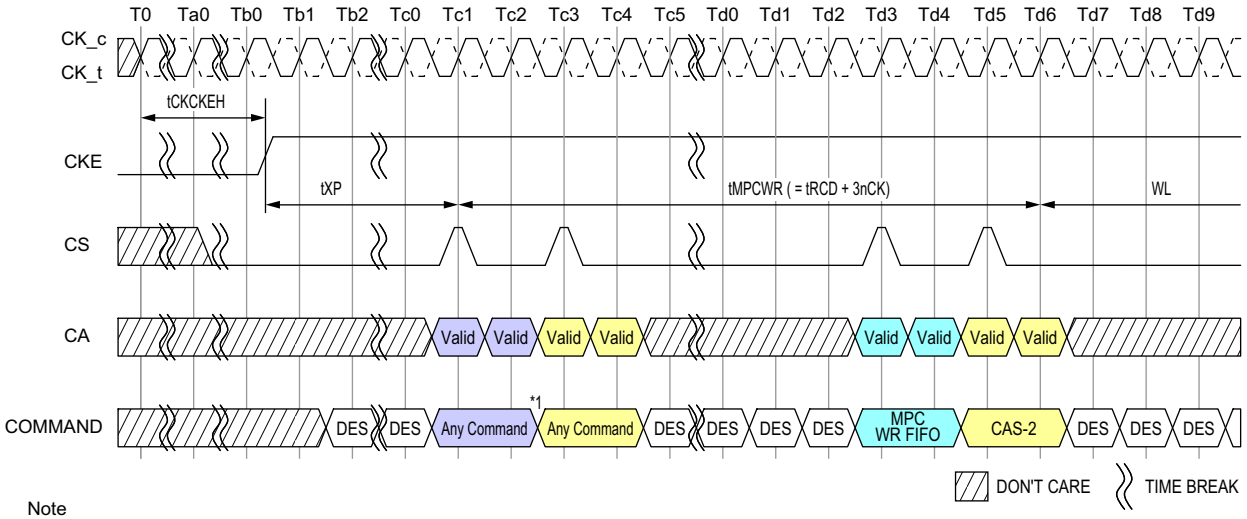

NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC [RD-FIFO] command to Read is tRTRRD.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
8. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK
9. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 115 - MPC [Read FIFO] to Read Timing**




Note
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [WR-FIFO] uses the same command-to-data/ODT timing relationship (WL, tDQSS, tDQS2DQ, ODTLon, ODTLoff, tODTon, tODToff) as a Write-1 command.
3. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven “LOW.”
4. BL = 16, Write Postamble = 0.5nCK
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 116 - MPC [Write FIFO] with DQ ODT Timing**




Note
1. Any commands except MPC WR FIFO and other exception commands defined other section in this document (i.e. MPC Read DQ Cal).
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 117 - Power Down Exit to MPC [Write FIFO] Timing**

**Table 67 - MPC [Write FIFO] AC Timing**

| Parameter | Symbol | Min Max | Data Rate | Unit | Note |
|---|---|---|---|---|---|
| Additional time After tXP has expired until MPC[Write FIFO] CMD may be issued | tMPCWR | Min | tRCD+3nCK | - | |

## 2.33. DQS Interval Oscillator

As voltage and temperature change on the SDRAM die, the DQS clock tree delay will shift and may require re-training. The LPDDR4-SDRAM includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error.

The DQS Interval Oscillator is started by issuing a MPC [Start DQS Osc] command with OP[6:0] set as described in the MPC Operation section, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS Oscillator may be stopped by issuing a MPC [Stop DQS Osc] command with OP[6:0] set as described in the MPC Operation section, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS Oscillator, then the MPC [Stop DQS Osc] command should not be used (illegal). When the DQS Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

**DQS Oscillator Granularity Error = 2 * (DQS delay) / run time**

Where:

Run Time = total time between start and stop commands

DQS delay = the value of the DQS clock tree delay (tDQS2DQ min/max)

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific.

Therefore, the total accuracy of the DQS Oscillator counter is given by:

**DQS Oscillator Accuracy = 1 - Granularity Error - Matching Error**

**For example**: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

**DQS Oscillator Granularity Error = 2*(0.8ns) / 100ns = 1.6%**

This equates to a granularity timing error or 12.8ps.
Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

**DQS Oscillator Accuracy = 1 - [(12.8+5.5) / 800] = 97.7%**

**For example**: running the DQS oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 500ns, and the maximum DQS clock tree delay is 800ps (tDQS2DQ max), then the DQS Oscillator Granularity Error is:

**DQS Oscillator Granularity Error = 2*(0.8ns) / 500ns = 0.32%**

This equates to a granularity timing error or 2.56ps.
Assuming a circuit Matching Error of 5.5ps across voltage and temperature, then the accuracy is:

**DQS Oscillator Accuracy = 1 - [(2.56+5.5) / 800] = 99.0%**

The result of the DQS Interval Oscillator is defined as the number of DQS Clock Tree Delays that can be counted within the "run time," determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0]. MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC-1 [Stop DQS Osc] command is received. The SDRAM counter will count to its maximum value (=2^16) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

**Longest Run Time Interval = $2^{16}$ * tDQS2DQ(min) = $2^{16}$ * 0.2ns = 13.1us**

### 2.33.1. Interval Oscillator matching error

The interval oscillator matching error is defined as the difference between the DQS training ckt(interval oscillator) and the actual DQS clock tree across voltage and temperature.

**Parameters:**

- tDQS2DQ: Actual DQS clock tree delay
- tDQSOSC: Training ckt(interval oscillator) delay
- OSCOffset: Average delay difference over voltage and temp (shown in the figure below)
- OSCMatch: DQS oscillator matching error

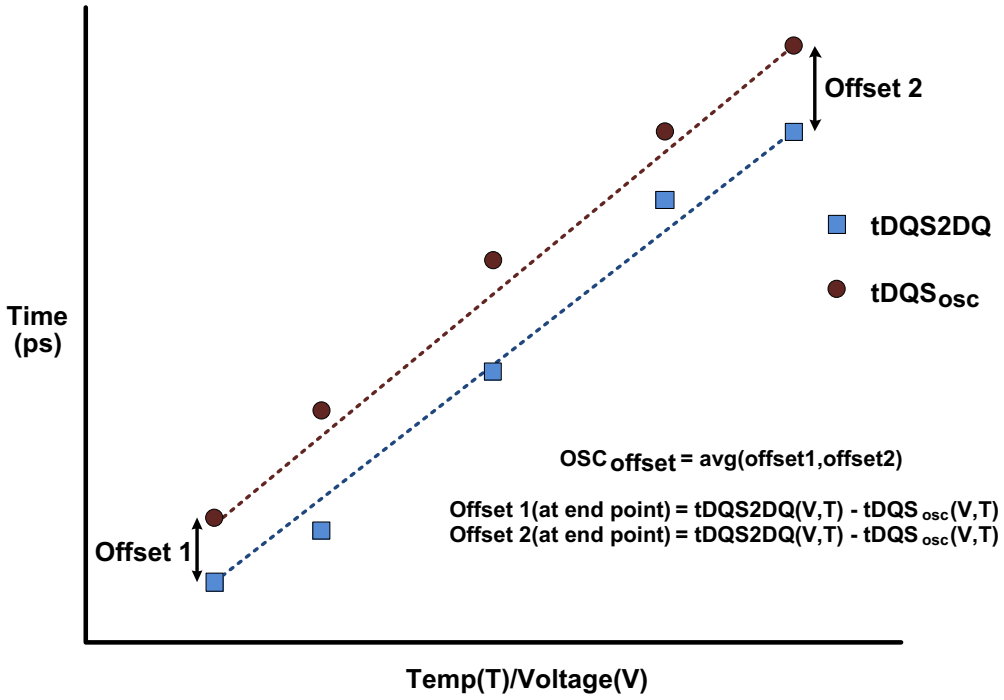



**Figure 118 - Interval oscillator offset ($OSC_{offset}$)**

$OSC_{Match}$ :

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

$tDQS_{OSC}$ :

$$tDQS_{OSC(V,T)} = Runtime / 2 * Count$$

**Table 68 - DQS Oscillator Matching Error Specification**

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DQS Oscillator Matching Error | $OSC_{Match}$ | -20 | 20 | ps | 1,2,3,4,5,6,7 |
| DQS Oscillator Offset | $OSC_{offset}$ | -100 | 100 | ps | 2,4,7 |

Note

1. The $OSC_{Match}$ is the matching error per between the actual DQS and DQS interval oscillator over voltage and temp.
2. This parameter will be characterized or guaranteed by design.
3. The $OSC_{Match}$ is defined as the following:

$$OSC_{Match} = [tDQS2DQ_{(V,T)} - tDQS_{OSC(V,T)} - OSC_{offset}]$$

Where $tDQS2DQ_{(V,T)}$ and $tDQS_{OSC(V,T)}$ are determined over the same voltage and temp conditions.

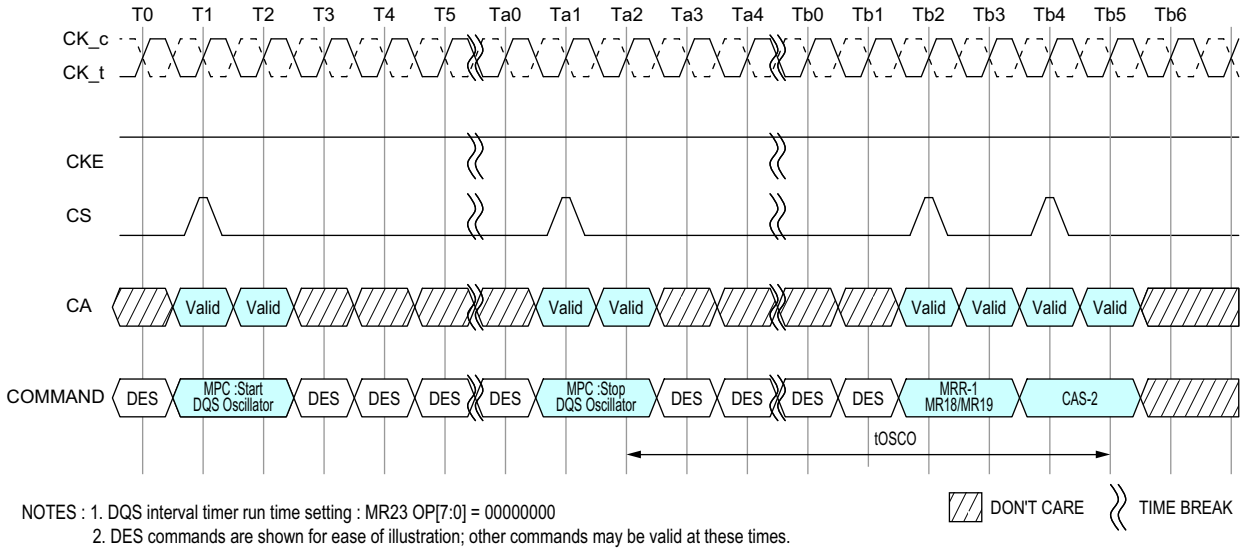
4. The runtime of the oscillator must be at least 200ns for determining $tDQS_{OSC(V,T)}$

$$tDQS_{OSC(V,T)} = Runtime / 2 * Count$$

5. The input stimulus for tDQS2DQ will be consistent over voltage and temp conditions.
6. The OSCoffset is the average difference of the endpoints across voltage and temp.
7. These parameters are defined per channel.
8. tDQS2DQ(V,T) delay will be the average of DQS to DQ delay over the runtime period.

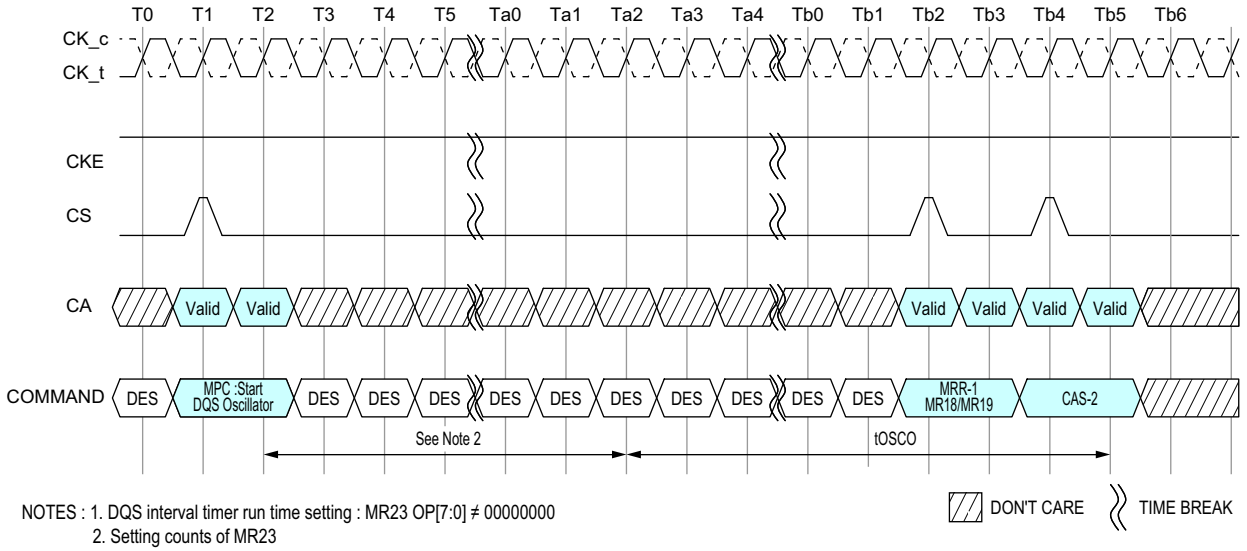
### 2.33.2. DQS Interval Oscillator Readout Timing

OSC Stop to its counting value readout timing is shown in following figures.




NOTES : 1. DQS interval timer run time setting : MR23 OP[7:0] = 00000000
2. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 119 - In case of DQS Interval Oscillator is stopped by MPC Command**




NOTES : 1. DQS interval timer run time setting : MR23 OP[7:0] ≠ 00000000
2. Setting counts of MR23
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 120 - In case of DQS Interval Oscillator is stopped by DQS interval timer**

**Table 69 - DQS interval Oscillator AC timing**

| Parameter | Symbol | Min Max | Data Rate | Unit | Note |
|---|---|---|---|---|---|
| Delay time from OSC stop to Mode Register Readout | tOSCO | Min | Max (40ns, 8nCK) | tCK | |

Notes
1. Start DQS OSC command is prohibited until tOSCO(Min) is satisfied.

## 2.34. Read Preamble Training

LPDDR4 READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13[OP1] = 1, the LPDDR4 DRAM will drive DQS_t LOW, DQS_c HIGH within tSDO and remain at these levels until an MPC DQ READ Training command is issued.

During READ Preamble Training the DQS preamble provided during normal operation will not be driven by the DRAM. Once the MPC DQ READ Training command is issued, the DRAM will drive DQS_t/DQD_c like a normal READ burst after RL. DRAM may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Calibration commands may be issued.

- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command.
- Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4 SDRAM, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
- Note that the pattern is driven on the DMI pins, but no data bus inversion function is enabled, even if Read DBI is enabled in the DRAM mode register.
- This command can be issued every tCCD seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

READ Preamble Training is exited within tSDO after setting MR13[OP1] = 0.

LPDDR4 supports the READ Preamble Training as optional feature. Refer to vendor specific datasheets.

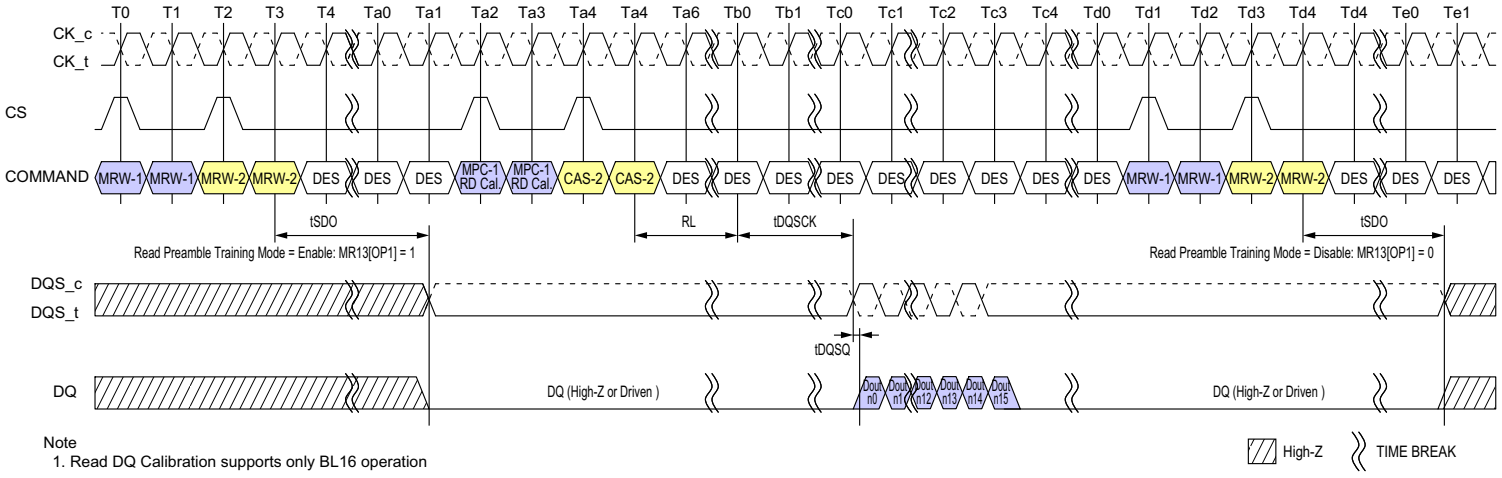



**Figure 121 - Read Preamble Training**

**Table 70 - Read Preamble Training Timings**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Delay from MRW command to DQS Driven | tSDO | max | max(12nCK,20ns) | | | | | | | | - | |

## 2.35. Multi Purpose Command (MPC)

LPDDR4-SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW. The following MPC commands must be followed by a CAS-2 command:

- Write FIFO
- Read FIFO
- Read DQ Calibration

All other MPC commands do not require a CAS-2 command, including:

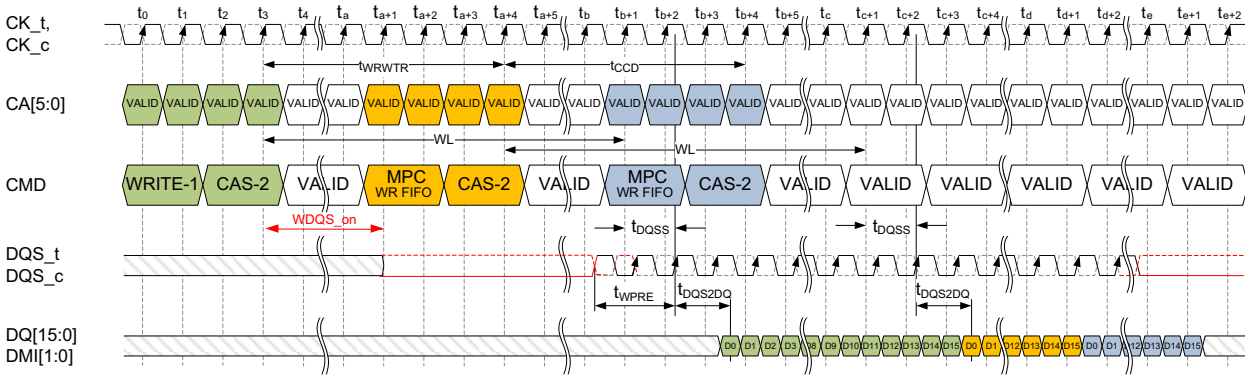
- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

**Table 71 - MPC Command Definition**

| Command | SDR Command Pins (2) | | | SDR CA Pins (6) | | | | | | CK_t edge | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CKE | | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| | CK_t(n-1) | CK_t(n) | | | | | | | | | |
| MPC (Train, NOP) | H | H | H | L | L | L | L | L | OP6 | R1 | 1,2 |
| | | | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |

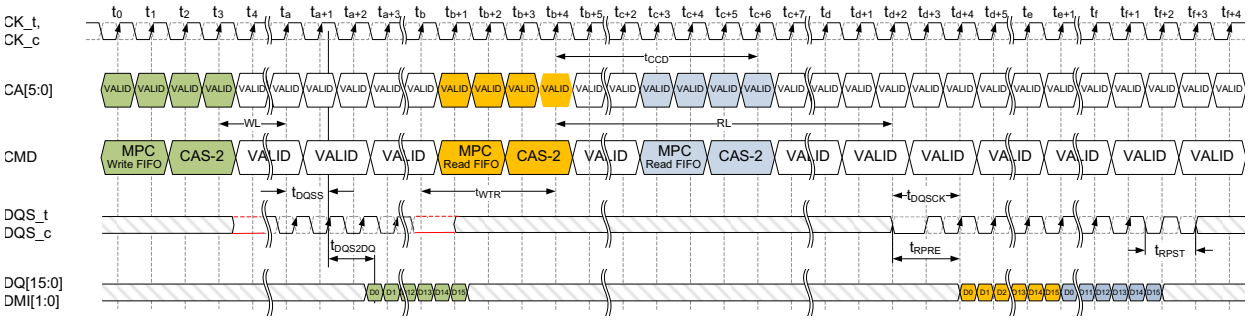
| Function | Operand | Data | Notes |
|---|---|---|---|
| Training Modes | OP[6:0] | 0XXXXXXB: NOP<br>1000001B: RD FIFO (only supports BL16 operation)<br>1000011B: RD DQ Calibration (MR32/MR40)<br>1000101B: RFU<br>1000111B: WR FIFO (only supports BL16 operation)<br>1001001B: RFU<br>1001011B: Start DQS Osc<br>1001101B: Stop DQS Osc<br>1001111B: ZQCal Start<br>1010001B: ZQCal Latch<br>All Others: Reserved | 1,2,3 |

Notes
1. See command truth table for more information
2. MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in between. MPC command must be issued first before issuing the CAS-2 command.
3. Write FIFO and Read FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].



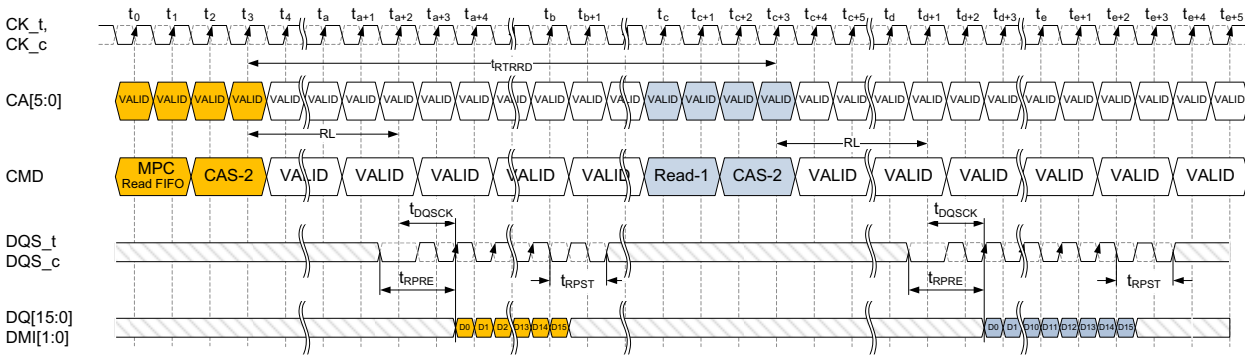

NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.
The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR.
See Write Training session for more information on FIFO pointer behavior.

**Figure 122 - MPC [WR FIFO] Operation :WPRE =2nCK, tWPST = 0.5nCK**




NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC-1 [WR-FIFO] is tWRWTR.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 123 - MPC [RD FIFO] Read Operation**
**(Shown with tWPRE=2nCK, tWPST=0.5nCK, tRPRE=toggling, tRPST=1.5nCK)**




NOTES : 1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC-1 [RD-FIFO] command to Read is tRTRRD.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data. See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven “LOW.”
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

**Figure 124 - MPC [RD FIFO] Operation (Shown with tRPRE=toggling, tRPST=1.5nCK)**

**Table 72 - Timing Constraints for Training Commands**

| Previous Command | Next Command | Minimum Delay | Unit | Notes |
|---|---|---|---|---|
| WR/MWR | MPC [WR FIFO] | tWRWTR | nCK | 1 |
| | MPC [RD FIFO] | Not Allowed | - | 2 |
| | MPC [RD DQ Calibration] | WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK) | nCK | |
| RD/MRR | MPC [WR FIFO] | tRTRRD | nCK | 3 |
| | MPC [RD FIFO] | Not Allowed | - | 2 |
| | MPC [RD DQ Calibration] | tRTRRD | nCK | 3 |
| MPC [WR FIFO] | WR/MWR | Not Allowed | - | 2 |
| | MPC [WR FIFO] | tCCD | nCK | |
| | RD/MRR | Not Allowed | - | 2 |
| | MPC [RD FIFO] | WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK) | nCK | |
| | MPC [RD DQ Calibration] | Not Allowed | - | 2 |
| MPC [RD FIFO] | WR/MWR | tRTRRD | nCK | 3 |
| | MPC [WR FIFO] | tRTW | nCK | 4 |
| | RD/MRR | tRTRRD | nCK | 3 |
| | MPC [RD FIFO] | tCCD | nCK | |
| | MPC [RD DQ Calibration] | tRTRRD | nCK | 3 |
| MPC [RD DQ Calibration] | WR/MWR | tRTRRD | nCK | 3 |
| | MPC [WR FIFO] | tRTRRD | nCK | 3 |
| | RD/MRR | tRTRRD | nCK | 3 |
| | MPC [RD FIFO] | Not Allowed | - | 2 |
| | MPC [RD DQ Calibration] | tCCD | nCK | |

Notes
1. tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + max(RU(7.5ns/tCK), 8nCK)
2. No commands are allowed between MPC [WR FIFO] and MPC [RD FIFO] except MRW commands related to training parameters.
3. tRTRRD = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) + max(RU(7.5ns/tCK),8nCK)
4. **tRTW (DQ ODT Disabled case; MR11 OP[2:0]=000b)** = RL + RU(tDQSCK(max)/tCK) + BL/2 - WL + tWPRE + RD(tRPST)
   **tRTW (DQ ODT Enabled case; MR11 OP[2:0]≠000b)** = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon,min/tCK) + 1

## 2.36. Thermal offset

Because of their tight thermal coupling with the LPDDR4 device, hot spots on an SOC can induce thermal gradients across the LPDDR4 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR4(6:5) to either or to both the channels. This temperature offset may modify refresh behavior for the channel to which the offset is provided. It will take a max of 200us to have the change reflected in MR4(2:0) for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 degrees C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR4 memory controller.

Support of thermal offset function is optional. Please refer to vendor datasheet to figure out if the function is supported or not.

## 2.37. Temperature Sensor

LPDDR4 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR4 devices shall monitor device temperature and update MR4 according to tTSI. Upon assertion of CKE (Low to High transition), the device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in Self Refresh state with CKE HIGH.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85°C when MR4[2:0] equals 'b011. LPDDR4 devices shall allow for 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$TempGradient \times (ReadInterval + tTSI + SysRespDelay) \leq 2°C$$

**Table 73 - Temperature Sensor**

| Parameter | Symbol | Max/Min | Value | Unit | Notes |
|---|---|---|---|---|---|
| System Temperature Gradient | TempGradient | Max | System Dependent | $^{o}$C/s | |
| MR4 Read Interval | ReadInterval | Max | System Dependent | ms | |
| Temperature Sensor Interval | tTSI | Max | 32 | ms | |
| System Response Delay | SysRespDelay | Max | System Dependent | ms | |
| Device Temperature Margin | TempMargin | Max | 2 | $^{o}$C | |

For example, if TempGradient is 10$^{o}$C/s and the SysRespDelay is 1 ms: (10'C/s) x (ReadInterval + 32ms + 1ms) <= 2'C

In this case, ReadInterval shall be no greater than 167ms.

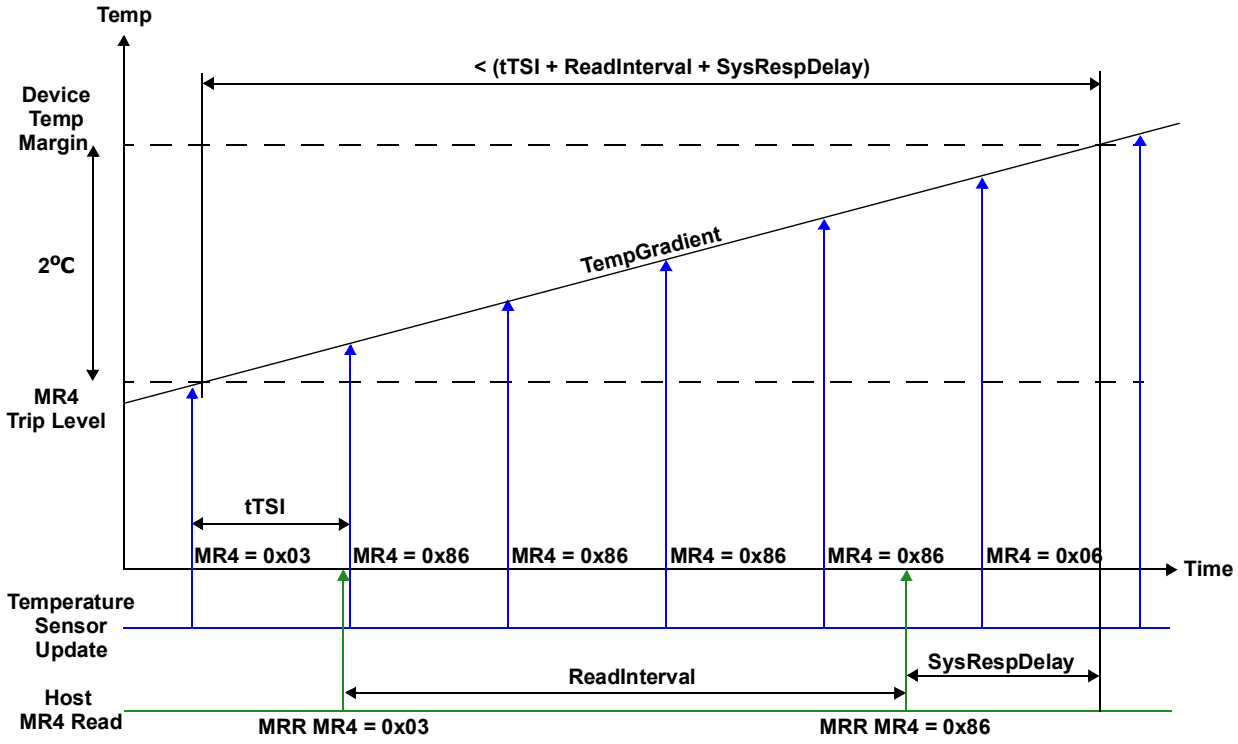



**Figure 125 - Temp sensor Timing**

## 2.38. ZQ Calibration

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation, and is designed to eliminate any need for coordination between channels (i.e. it allows for channel independence).

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the SDRAM's calibration procedure, and ZQCal Latch captures the result and loads it into the SDRAM's drivers.

A ZQCal Start command may be issued anytime the LPDDR4-SDRAM is not in a power-down state. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated. The following mode register fields that modify I/O parameters cannot be changed following a ZQCal Start command and before tZQCAL has expired:

- PU-Cal (Pull-up Calibration VOH Point)
- PDDS (Pull Down Drive Strength and Rx Termination)
- DQ-ODT (DQ ODT Value)
- CA-ODT (CA ODT Value)

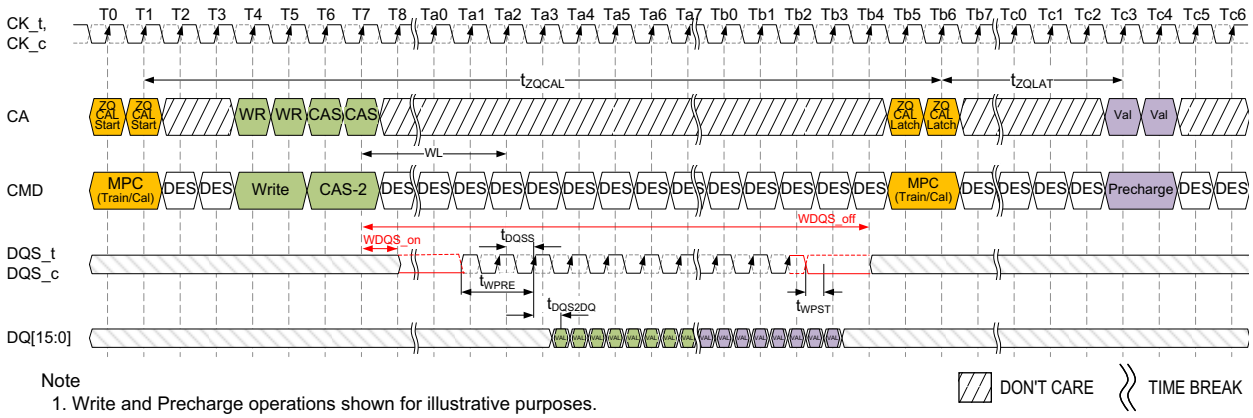
### 2.38.1. ZQCal Reset

The ZQCal Reset command resets the output impedance calibration to a default accuracy of +/- 30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/- 30% when ZQCal Start and ZQCal Latch commands are not used.

The ZQCal Reset command is executed by writing MR10-OP[0]=1B.

**Table 74 - ZQCal Timing Parameters**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ZQ Calibration Time | tZQCAL | min | 1 | | | | | | | | us | |
| ZQ Calibration Latch Time | tZQLAT | min | max(30ns, 8nCK) | | | | | | | | ns | |
| ZQ Calibration Reset Time | tZQRESET | min | max(50ns, 3nCK) | | | | | | | | ns | |




Note

1. Write and Precharge operations shown for illustrative purposes.
   Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
2. Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed.
   Write commands with DQ Termination must be given enough time to turn off the DQ-ODT before issuing the ZQ-Latch command.
   See the ODT section for ODT timing.

**Figure 126 - ZQCal Timing**

### 2.38.2. Multi-Channel Considerations

The LPDDR4-SDRAM includes a single ZQ pin and associated ZQ Calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

1. ZQCal Start commands may be issued to either or both channels.
2. ZQCal Start commands may be issued when either or both channels are executing other commands and other commands may be issued during tZQCAL.
3. ZQCal Start commands may be issued to both channels simultaneously.
4. The ZQCal Start command will begin the calibration unless a previously requested ZQ calibration is in progress.
5. If a ZQCal Start command is received while a ZQ calibration is in progress on the SDRAM, the ZQCal Start command will be ignored and the in-progress calibration will not be interrupted.
6. ZQCal Latch commands are required for each channel.
7. ZQCal Latch commands may be issued to both channels simultaneously.
8. ZQCal Latch commands will latch results of the most recent ZQCal Start command provided tZQCAL has been met.
9. ZQCal Latch commands which do not meet tZQCAL will latch the results of the most recently completed ZQ calibration.
10. ZQ Reset MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCal Start and ZQCal Latch commands as needed without regard to the state of the other channel.

### 2.38.3. ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and VDDQ.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel shall use a separate ZQCal resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQ Cal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF.

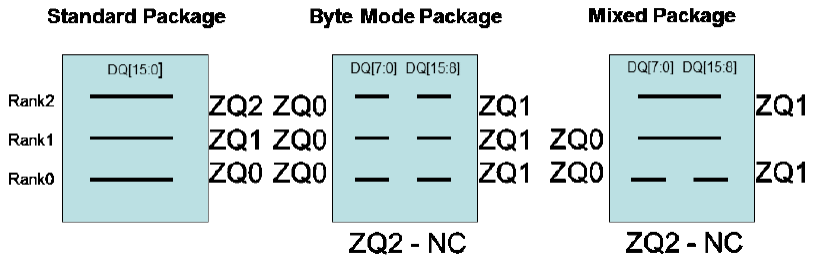
Example: If a system configuration shares a CA bus between 'n' channels to form a n * 16 wide bus, and no means are available to control the ZQCal separately for each channel (i.e. separate CS, CKE, or CK), then each x16 channel must have a separate ZQCal resistor.

Example: For a x32, two rank system, each x16 channel must have its own ZQCal resistor, but the ZQCal resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCal commands for Rank[0] and Rank[1] don't overlap.

### 2.38.3.1. ZQ Wiring for Byte-mode PKG including mixed configuration

Standard LPDDR4 package ballmpas allocate one ZQ ball per die. Byte-mode packages potentially support more die for higher package memory density. In order to use ballmapes developed for Standard LPDDR4, an alternate ZQ ball wiring strategy is employed when packages contain Byte-mode devices as shown in Figure below.
Since this wiring strategy for Byte-Mode and Mixed packages shares a single ZQ resistor between ranks and channels, applications must ensure that the ZQCal's do not overlap between the dies sharing the resistor.

- Applications shall ensure that ZQCal_Start commands to one rank on any dies sharing a ZQ resistor must complete (tZQCal satisfied) prior to issuing a ZQCal_Start command to a different rank tied to the resistor. (Applications can satisfy this requirement, for example, by either:
  - Issuing ZQCal_Start commands simultaneously to both DRAM channels
  - Issuing ZQCal_Start commands to one DRAM channel only)
- DRAM shall ensure that ZQCal_Start can be sent independently to the two channels on a die.
  If a ZQCal_Start command is received while a ZQ calibration is in progress on the die, the second ZQCal_Start command will be ignored and the in progress calibration will not be interrupted.
  (See Section 2.38.3. "ZQ External Resistor, Tolerance, and Capacitive Loading")




Below are specific wiring notes for LPDDR4 packages

1. For packages using only standard devices
   - ZQ0 is connected to rank 0 DRAM
   - ZQ1 is connected to rank 1 DRAM (if present)
   - ZQ2 is connected to rank 2 DRAM (if present)
2. For packages using only byte-mode devices
   - ZQ0 is connected to all lower byte[7:0] or upper byte [15:8] DRAM(s)
   - ZQ1 is connected to opposite byte of all DRAM(s) from those connected to ZQ0
   - ZQ2 is NC
3. For packages using both standard and byte-mode devices
   - ZQ0 is connected to all lower byte[7:0] or upper byte [15:8] DRAM(s)
   - ZQ1 is connected to opposite byte of all DRAM(s) from those connected to ZQ0
   - Standard DRAM(s) may be connected to either ZQ0 or ZQ1
   - ZQ2 is NC.

Multi-rank packages containing Byte-mode devices place additional loading on the I/O and power topologies and therefore may not be appropriate for all application environments.

## 2.39. Pull-down and Pull-up Driver Characteristics and Calibration

**Table 75 - Pull-down Driver Characteristics, with ZQ Calibration**

| $R_{ONPD}$,nom | Resistor | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| 40 Ohm | $R_{ON40PD}$ | 0.9 | 1.0 | 1.1 | RZQ/6 |
| 48 Ohm | $R_{ON48PD}$ | 0.9 | 1.0 | 1.1 | RZQ/5 |
| 60 Ohm | $R_{ON60PD}$ | 0.9 | 1.0 | 1.1 | RZQ/4 |
| 80 Ohm | $R_{ON80PD}$ | 0.9 | 1.0 | 1.1 | RZQ/3 |
| 120 Ohm | $R_{ON120PD}$ | 0.9 | 1.0 | 1.1 | RZQ/2 |
| 240 Ohm | $R_{ON240PD}$ | 0.9 | 1.0 | 1.1 | RZQ/1 |

Notes
1. All values are after ZQ calibration. Without ZQ Calibration RONPD values are +/- 30%

**Table 76 - Pull-up Driver Characteristics, with ZQ Calibration**

| $VOH_{PU}$,nom | VOH,nom(mV) | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| VDDQ*0.5 | 300 | 0.9 | 1.0 | 1.1 | VOH,nom |
| VDDQ*0.6 | 360 | 0.9 | 1.0 | 1.1 | VOH,nom |

Notes
1. All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%.
2. VOH,nom (mV) values are based on a nominal VDDQ = 0.6 V.

**Table 77 - Valid Calibration Points**

| $VOH_{PU}$,nom | ODT Values | | | | | |
|---|---|---|---|---|---|---|
| | 240 | 120 | 80 | 60 | 48 | 40 |
| VDDQ*0.5 | Valid | Valid | Valid | Valid | Valid | Valid |
| VDDQ*0.6 | DNU | Valid | DNU | Valid | DNU | DNU |

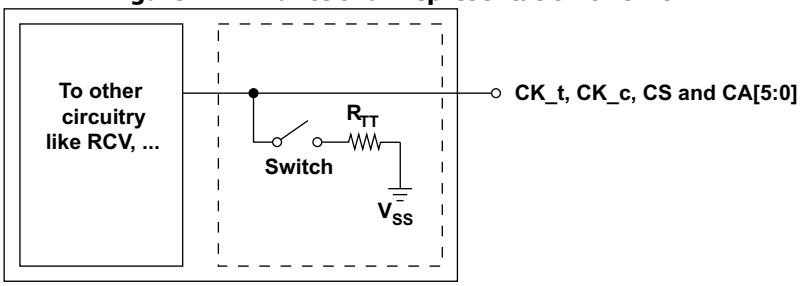
Notes
1. Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2. If the VOH(nom) calibration point is changed, then re-calibration is required.
3. DNU = Do Not Use

## 2.40. On Die Termination Command/Address Bus

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the SDRAM to turn on/off termination resistance for CK_t, CK_c, CS and CA[5:0] signals without the ODT control pin.
The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting.

A simple functional representation of the DRAM ODT feature is shown in the Figure below

**Figure 127 - Functional Representation of CA ODT**



### 2.40.1. ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_C, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS and CA[5:0] signals. Generally, only one termination load will be present even if multiple devices are sharing the command signals. In contrast to LPDDR4 where the ODT_CA input is used in combination with mode registers, LPDDR4X uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In a multi rank system, the terminating rank should be trained first, followed by the nonterminating rank(s).

**Table 78 - Command Bus ODT State**

| ODTE-CA MR11[6:4] | ODTD-CA MR22[5] | ODTE-CK MR22[3] | ODTE-CS MR22[4] | ODT State for CA | ODT State for CK_t/CK_c | ODT State for CS |
|---|---|---|---|---|---|---|
| Disabled[1] | Valid[2] | Valid[2] | Valid[2] | Off | Off | Off |
| Valid[2] | 0 | 0 | 0 | On | On | On |
| Valid[2] | 0 | 0 | 1 | On | On | Off |
| Valid[2] | 0 | 1 | 0 | On | Off | On |
| Valid[2] | 0 | 1 | 1 | On | Off | Off |
| Valid[2] | 1 | 0 | 0 | Off | On | On |
| Valid[2] | 1 | 0 | 1 | Off | On | Off |
| Valid[2] | 1 | 1 | 0 | Off | Off | On |
| Valid[2] | 1 | 1 | 1 | Off | Off | Off |

Notes
1. Default value
2. "Valid" means "0 or 1"

### 2.40.2. ODT Mode Register and ODT characteristics

A functional representation of the on-die termination is shown in the figure below.

$$RTT = Vout / |Iout|$$

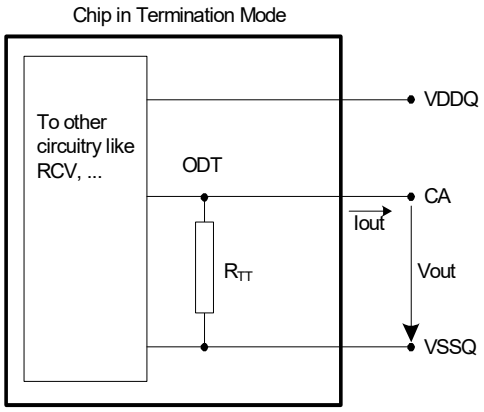



**Figure 128 - On Die Termination for CA**

**Table 79 - ODT DC Electrical Characteristics**
**(assuming RZQ=240Ω +/- 1% over the entire operating temperature range after a proper ZQ calibration)**

| MR11 OP[6:4] | RTT | Vout | Min | Nom | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 001 | 240Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.3 | | 1,2 |
| 010 | 120Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.2 | | 1,2 |
| 011 | 80Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.2 | | 1,2 |
| 100 | 60Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.2 | | 1,2 |
| 101 | 48Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.2 | | 1,2 |
| 110 | 40Ω | VOLdc=0.20*VDD2 | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2 |
| | | VOMdc=0.50*VDD2 | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDD2 | 0.9 | 1.0 | 1.2 | | 1,2 |
| Mismatch CA-CA within clk group | | 0.50*VDD2 | - | | 2 | % | 1,2,3 |

Notes
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 3.4 on voltage and temperature sensitivity.
2. Pull-dn ODT resistors are recommended to be calibrated at 0.50*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75*VDDQ and 0.2*VDDQ.
3. CA to CA mismatch within clock group (CA,CS) variation for a given component including CK_t and CK_c (characterized).

$$CA - CAmismatch = \frac{RODT(max) - RODT(min)}{RODT(avg)}$$

### 2.40.3. ODT for Command/Address update time

ODT for Command/Address update time after Mode Register set are shown in the figure below

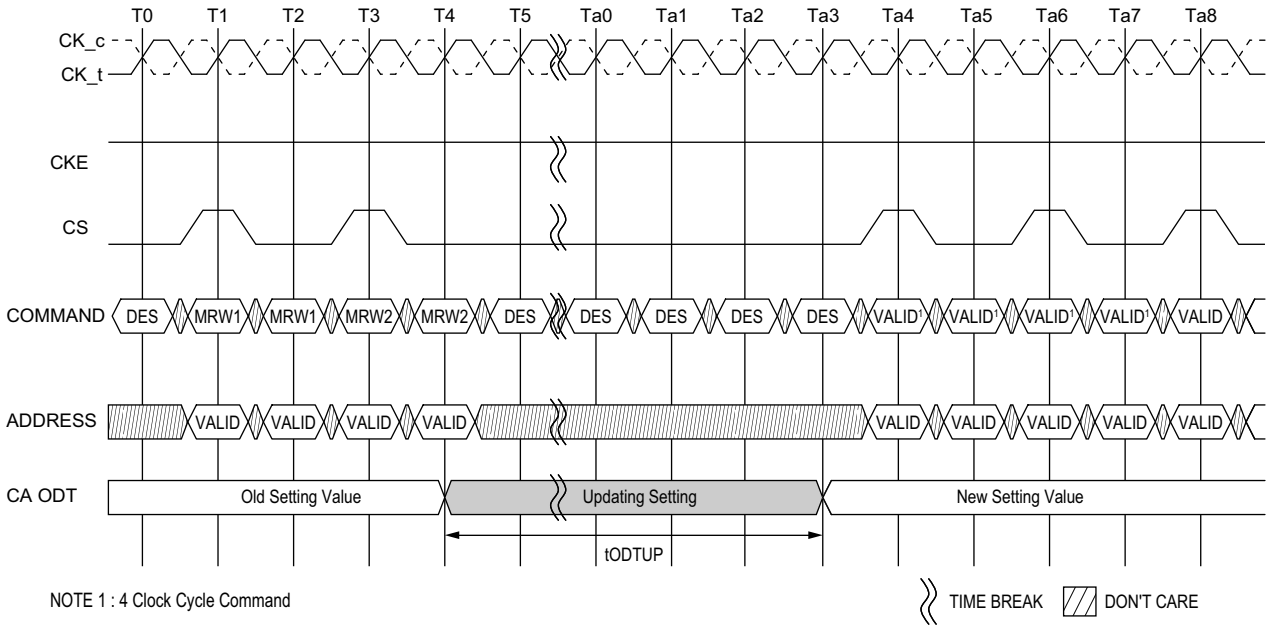



**Figure 129 - CA ODT setting update timing in 4 Clock Cycle Command**

**Table 80 - ODT CA AC timing**

| Parameter | Symbol | min max | LPDDR4-1600/1866/2133/2400/3200/3733/4266 | Units | Note |
|---|---|---|---|---|---|
| ODT CA Value Update Time | tODTUP | Min | RU (tbd ns/tCK(avg)) | | |

## 2.41. On-die Termination

ODT (On-Die Termination) is a feature of the LPDDR4 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS_t, DQS_c and DMI signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during Write operation.

The ODT feature is off and cannot be supported in Power Down and Self-Refresh modes.

A simple functional representation of the DRAM ODT feature is shown in following Figure.

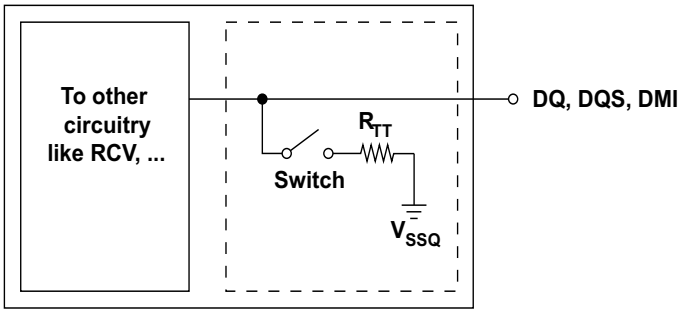



**Figure 130 - Functional Representation of DQ ODT**

The switch is enabled by the internal ODT control logic, which uses the Write-1 or Mask Wirte-1command and other mode register control information. The value of RTT is determined by the settings of Mode Register bits.

### 2.41.1. ODT Mode Register

The ODT Mode is enabled if MR11 OP[3:0] are non zero. In this case, the value of RTT is determined by the settings of those bits.

The ODT Mode is disabled if MR11 OP[3] = 0.

### 2.41.2. Asynchronous ODT

When ODT Mode is enabled in MR11 OP[3:0], DRAM ODT is always Hi-Z. DRAM ODT feature is automatically turned ON asynchronously based on the Write-1 or Mask Write-1 command that DRAM samples. After the write burst is complete, DRAM ODT featured is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled:

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODToff,min, tODToff,max

ODTLon is a synchronous parameter and it is the latency from CAS-2 command to tODTon reference.

ODTLon latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLon latency.

Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum RTT turn on time (tODTon,max) is the point in time when the ODT resistance is fully on.

tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from CAS-2 command.

ODTLoff is a synchronous parameter and it is the latency from CAS-2 command to tODToff reference.

ODTLoff latency is a fixed latency value for each speed bin. Each speed bin has a different ODTLoff latency.

Minimum RTT turn-off time (tODToff,min) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (tODToff,max) is the point in time when the on-die termination has reached high impedance.

tODToff,min and tODToff,max are measured once ODTLoff latency is satisfied from CAS-2 command.

**Table 81 - ODTLon and ODTLoff Latency Values**

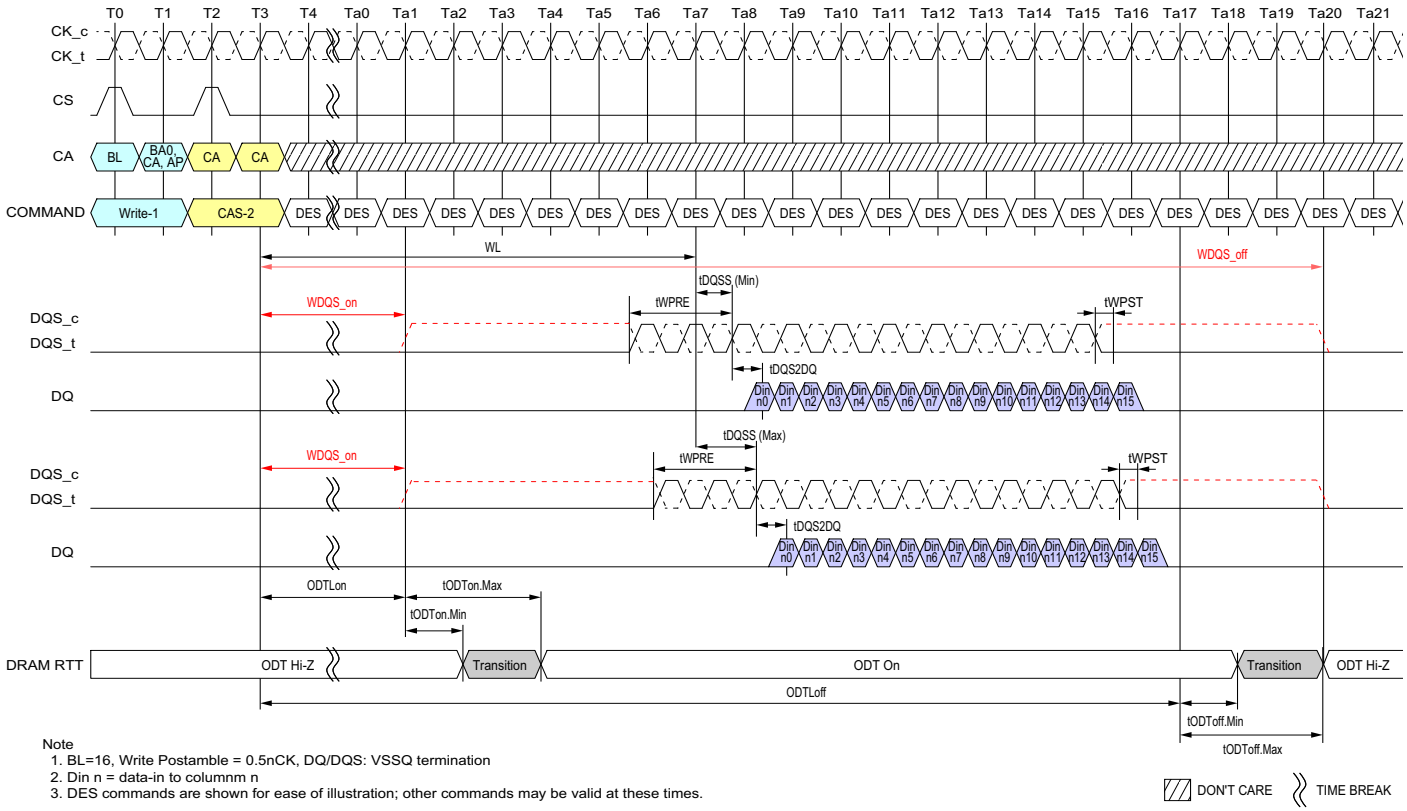
| ODTLon Latency [a] | | ODTLoff Latency [b] | | Lower Frequency Limit (>) | Upper Frequency Limit (≤) |
|---|---|---|---|---|---|
| WL Set "A" | WL Set "B" | WL Set "A" | WL Set "B" | | |
| N/A | N/A | N/A | N/A | 10 | 266 |
| N/A | N/A | N/A | N/A | 266 | 533 |
| N/A | 6 | N/A | 22 | 533 | 800 |
| 4 | 12 | 20 | 28 | 800 | 1066 |
| 4 | 14 | 22 | 32 | 1066 | 1333 |
| 6 | 18 | 24 | 36 | 1333 | 1600 |
| 6 | 20 | 26 | 40 | 1600 | 1866 |
| 8 | 24 | 28 | 44 | 1866 | 2133 |
| nCK | nCK | nCK | nCK | MHz | MHz |

Notes

1. ODTLon is referrenced from CAS-2 command. See timing diagram examples below.
2. ODTLoff is shown in table assumes BL=16. For BL32, 8 tCK should be added.

**Table 82 - Asynchronous ODT turn on and turn off timing**

| Parameter | 800~2133MHz | Unit |
|---|---|---|
| tODTon,min | 1.5 | ns |
| tODTon,max | 3.5 | ns |
| tODToff,min | 1.5 | ns |
| tODToff,max | 3.5 | ns |




Note
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to columnn n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 131 - Asynchronous ODTon/ODToff Timing**

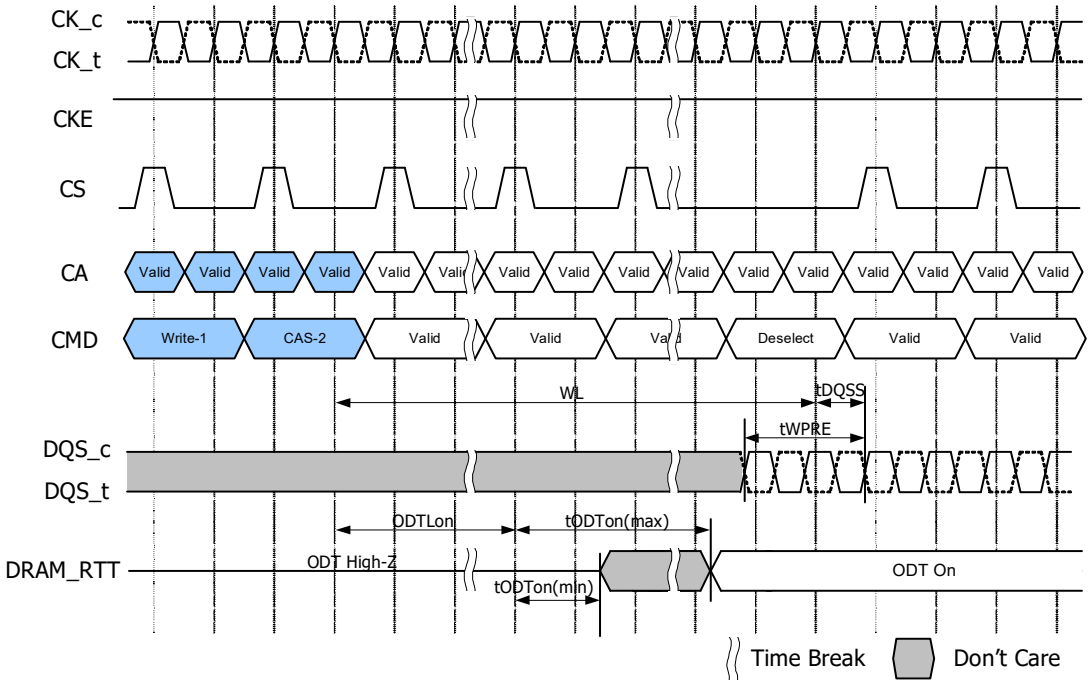



**Figure 132 - Asynchronous $ODT_{ON}$ Timing Example; tWPRE = 2 tCK, tDQSS = Nominal**

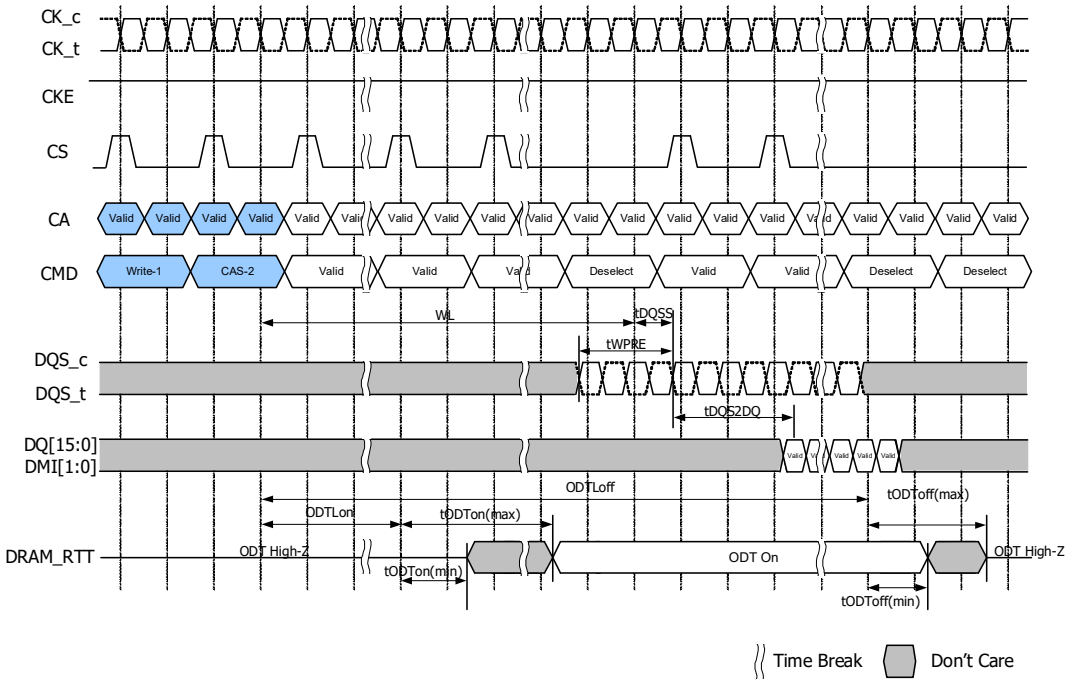



**Figure 133 - Asynchronous $ODT_{OFF}$ Timing Example, tWPRE = 2 nCK, tDQSS = Nominal**

### 2.41.3. ODT during Write Leveling

If ODT is enabled in MR11 OP[3:0], in Write Leveling mode, DRAM always provides the termination on DQS_t/DQS_c signals. DQ termination is always off in Write Leveling mode regardless.

**Table 83 - DRAM Termination Function in Write Leveling Mode**

| ODT Enabled in MR11 | DQS_t/DQS_c termination | DQ termination |
|---|---|---|
| Disabled | OFF | OFF |
| Enabled | ON | OFF |

## 2.42. On Die Termination for DQ, DQS and DMI

On-Die Termination effective resistance RTT is defined by MR bits MR11 OP[2:0].

ODT is applied to the DQ, DMI, DQS_t and DQS_c pins.

A functional representation of the on-die termination is shown in the figure below.

**RTT = Vout / |Iout|**

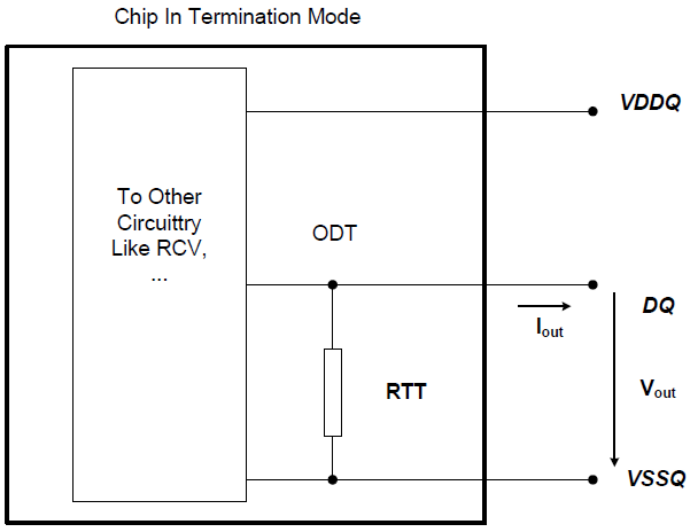



**Figure 134 - On Die Termination for DQ**

**Table 84 - ODT DC Electrical Characteristics**
**(assuming RZQ=240Ω +/- 1% over the entire operating temperature range after a proper ZQ calibration)**

| MR11 OP[2:0] | RTT | Vout | Min | Nom | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 001 | 240Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| 010 | 120Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/2 | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| 011 | 80Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/3 | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| 100 | 60Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/4 | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| 101 | 48Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/5 | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| 110 | 40Ω | VOLdc=0.20*VDDQ | 0.8 | 1.0 | 1.1 | RZQ/6 | 1,2 |
| | | VOMdc=0.50*VDDQ | 0.9 | 1.0 | 1.1 | | 1,2 |
| | | VOHdc=0.75*VDDQ | 0.9 | 1.0 | 1.3 | | 1,2 |
| Mismatch DQ-DQ within byte | | 0.50*VDDQ | - | | 2 | % | 1,2,3 |

Notes
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see 3.4 on voltage and temperature sensitivity.
2. Pull-dn ODT resistors are recommended to be calibrated at 0.75*VDDQ and 0.2*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75*VDDQ and 0.1*VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).

$$DQ-DQmismatch = \frac{RODT(max)-RODT(min)}{RODT(avg)}$$

## 2.43. Output Driver and Termination Register Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

**Table 85 - Output Driver and Termination Register Sensitivity Definition**

| Resistor | Definition Point | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $R_{ONPD}$ | 0.50 x VDDQ | 90-($dR_{on}dT$ x \|ΔT\|)-($dR_{on}dV$ x \|ΔV\|) | 110+($dR_{on}dT$ x \|ΔT\|)+($dR_{on}dV$ x \|ΔV\|) | % | 1,2 |
| $VOH_{PU}$ | 0.50 x VDDQ | 90-(dVOHdT x \|ΔT\|)-(dVOHdV x \|ΔV\|) | 110+(dVOHdT x \|ΔT\|)+(dVOHdV x \|ΔV\|) | % | 1,2 |
| $R_{TT(I/O)}$ | 0.50 x VDDQ | 90-($dR_{on}dT$ x \|ΔT\|)-($dR_{on}dV$ x \|ΔV\|) | 110+($dR_{on}dT$ x \|ΔT\|)+($dR_{on}dV$ x \|ΔV\|) | % | 1,2,3 |
| $R_{TT(In)}$ | 0.50 x VDDQ | 90-($dR_{on}dT$ x \|ΔT\|)-($dR_{on}dV$ x \|ΔV\|) | 110+($dR_{on}dT$ x \|ΔT\|)+($dR_{on}dV$ x \|ΔV\|) | % | 1,2,4 |

Notes
1. DT = T - T(@ Calibration), DV = V - V(@ Calibration)
2. dRONdT, dRONdV, dVOHdT, dVOHdV, dRTTdV, and dRTTdT are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI and the input pins such as CK, CA, and CS.
4. Refer to 2.39. "Pull-down and Pull-up Driver Characteristics and Calibration".

**Table 86 - Output Driver and Termination Register Temperature and Voltage Sensitivity**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $dR_{ON}dT$ | $R_{ON}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{ON}dV$ | $R_{ON}$ Voltage Sensitivity | 0.00 | 0.20 | %/mV |
| dVOHdT | VOH Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| dVOHdV | VOH Voltage Sensitivity | 0.00 | 0.35 | %/mV |
| $dR_{TT}dT$ | $R_{TT}$ Temperature Sensitivity | 0.00 | 0.75 | %/°C |
| $dR_{TT}dV$ | $R_{TT}$ Voltage Sensitivity | 0.00 | 0.20 | %/mV |

## 2.44. Single-ended mode for Clock and Strobe

LPDDR4X SDRAM supports the function of single-ended mode for Clock and Strobe independently to reduce power consumption at low frequency operation. The clock frequency applied by this function is equal or less than 800MHz and each ODT state (CK/CA, DQS/DQ) is required to be unterminated.
This function is optional. Refer to MR0 OP[5] whether this function is support or not.
The entering and exiting single-ended mode for Clock and Strobe is controlled by MR51 OP[3:1] setting.
The Single-ended mode for Strobe affects to the following commands.

- Write-1
- Mask Write-1**
- Read-1
- Mode Register Read-1*
- MPC Write FIFO**
- MPC Read FIFO*
- MPC Read DQ calibration: regardless of the setting of Read Preamble Training Mode: MR13 OP[1]*

*: Read equivalent operations

**: Write equivalent operations

### 2.44.1. Combination of Mode Register setting and ODT termination

Single-ended mode for Clock and Strobe MR setting:MR51 [OP3:1] can be independently. It means that the all setting i.e. OP[3:1] = 000, 001, 010 .... 110,111 is available. And ODT behavior for each MR51 OP[3:1] setting, to refer the following table.

**Table 87 - ODT status for Single-ended mode for Clock and Strobe**

| Function | MR#/Operand | Data | SDRAM ODT |
|---|---|---|---|
| Single ended RDQS | MR51[OP1] | 0B: Differential | Don't Care |
| | | 1B: Single-ended | Don't Care |
| Single ended WDQS | MR51[OP2] | 0B: Differential | DQ/DQS ODT Supports both enable and disable |
| | | 1B: Single-ended | DQ/DQS ODT Supports disable only |
| Single ended Clock | MR51[OP3] | 0B: Differential | CK ODT Supports both enable and disable |
| | | 1B: Single-ended | CK ODT Supports disable only |

### 2.44.2. Restriction of Single-ended mode

The following restriction applies under Single-ended mode

MR51 [OP1] = 1B: Single ended RDQS is enabled.

- The output level of DQS_c is always "LOW or Hi.Z " during read or equivalent operations

MR51 [OP2] = 1B: Single ended WDQS is enabled.

- DQS_c should be Valid (LOW or High) for WRITE or equivalent operations.
- DQS_t will be referenced to VREFDQ.
- The VREFDQ lower limit: MR14 OP[5:0] range is TBD thru 110010B: for MR14 OP[6]=0B or 1B.
- MR51 OP[2] has been set 1B (Enable) for either physical register. DQS_c input level is required to "High" during tDQSCKE and tCAENT period at CBT operation.

MR51 [OP3] = 1B: Single ended Clock is enabled.

- CK_c should be Valid (LOW or High)
- CK_t will be referenced to VREFCA.
- The VREFCA lower limit: MR12 OP[5:0] range is TBD thru 110010B: for MR12 OP[6]=0B or 1B.
- MR51 OP[3] has been set 1B (Enable) for either or both physical register. Additional timing period is needed after MRW command of changing the FSP status. VRCG status change to high current mode also is the same situation as FSP change.

### 2.44.3. Switching sequence between Differential and Single-ended

Switching only Read DQS functionality from differential to single ended and vice versa, Single Ended Read DQS Enable: MR51 OP[1] can be written by Mode Register Write command regardless FSP OP setting.

Switching the Write DQS and CK functionality from differential to single ended and vice versa is done only via frequency set point switching. Therefore the setting of FSP-OP: MR13 OP[7] and MR13 OP[6] need to be different at setting MR51 OP[3:2].

To support operation with Single-ended Clock and Strobe enabled, MR51 supports two physical registers and are included in the configuration changes supported with set points 0 and 1 during FSP switching.

The frequency set point update timing for Differential/Single-ended mode switching is shown below. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into VREF fast response (high current) mode at the same time. After frequency change time (tFC) is satisfied. VRCG can be changed into normal operation mode via MR13 OP[3].

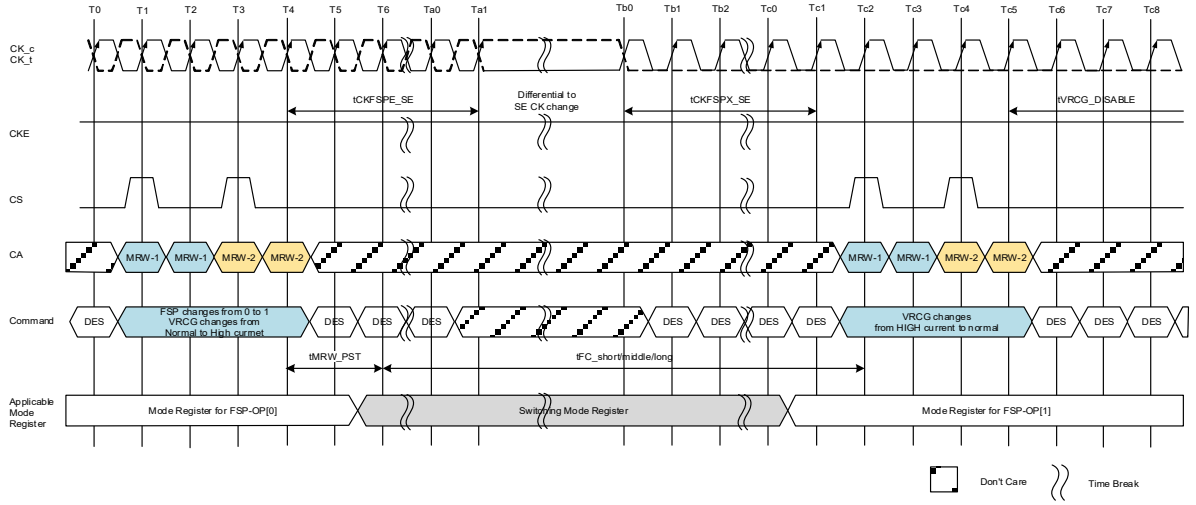



**Figure 135 - Differential to SE CK and Write DQS -FSP Switching Timing CKE=High**

Notes

1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to Section Input Clock Stop and Frequency Change.
2. Clock input level after Tb0 is an example. The stable high to the clock input is also allowed.
3. Mode Register Setting
   FSP-OP MR13 [OP7] =0B
   Single ended Clock MR51 [OP3] = 0B (Disabled)
   FSP-OP MR13 [OP7] =1B
   Single ended Clock: MR51 [OP3] = 1B (Enabled)

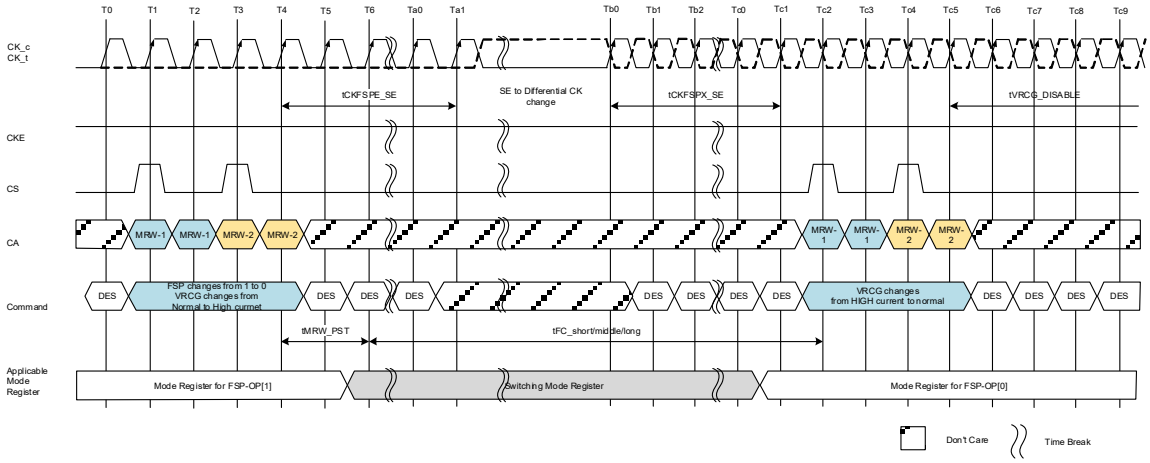



**Figure 136 - SE to Differential CK and Write DQS -FSP Switching Timing CKE=High**

Notes

1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to Section Input Clock Stop and Frequency Change.
2. Clock input level before Ta1 is an example. The stable high to the clock input is also allowed.
3. Mode Register Setting
   FSP-OP MR13 [OP7] =0B
   Single ended Clock MR51 [OP3] = 0B (Disabled)
   FSP-OP MR13 [OP7] =1B
   Single ended Clock: MR51 [OP3] = 1B (Enabled)

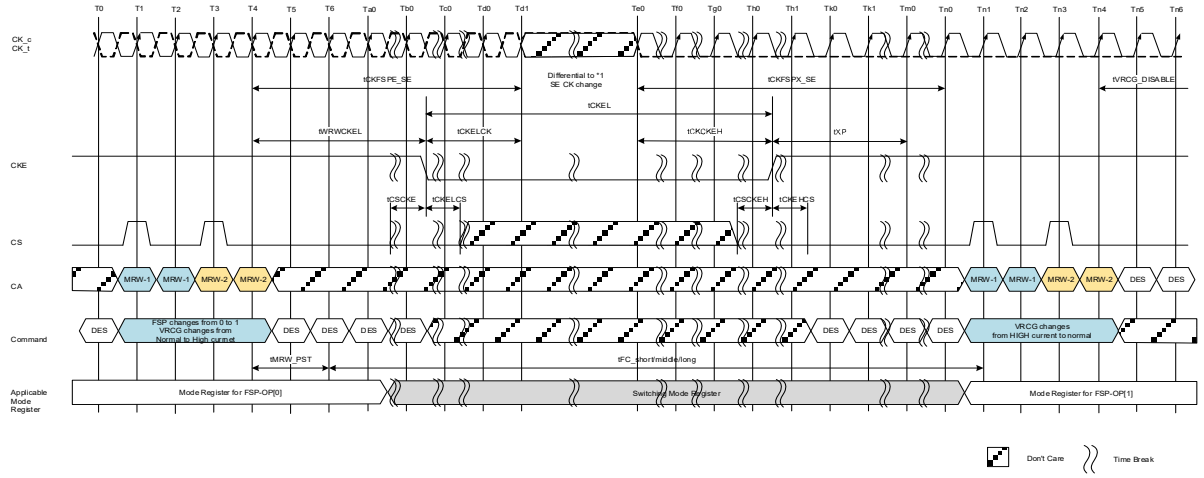



**Figure 137 - Differential to SE CK and Write DQS -FSP Switching Timing CKE=Low**

Notes

1. The input clock frequency can be changed, stopped, or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and that the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Clock input level after Te0 is an example. The stable high to the clock input is also allowed.
3. The CKE is able to move to LOW without satisfying tVRCG enable period.
4. Mode Register Setting
   FSP-OP MR13 [OP7] = 0B
   Single ended Clock MR51 [OP3] = 0B (Disabled)
   FSP-OP MR13 [OP7] = 1B
   Single ended Clock MR51 [OP3] = 1B (Enabled)

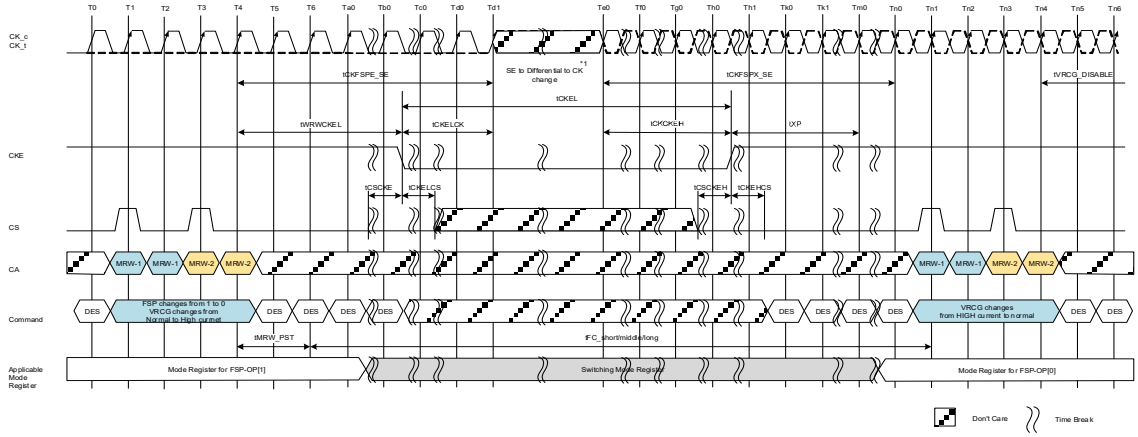



**Figure 138 - SE to Differential CK and Write DQS -FSP Switching Timing CKE=Low**

Notes

1. The input clock frequency can be changed, stopped, or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and that the clock frequency is between the minimum and maximum frequency for the speed grade in use.
2. Clock input level after Te0 is an example. The stable high to the clock input is also allowed.
3. The CKE is able to move to LOW without satisfying tVRCG enable period.
4. Mode Register Setting
   FSP-OP MR13 [OP7] = 0B
   Single ended Clock MR51 [OP3] = 0B (Disabled)
   FSP-OP MR13 [OP7] = 1B
   Single ended Clock MR51 [OP3] = 1B (Enabled)

### 2.44.4. VRCG Enable timing

The VRCG Enable timing when MR51 OP[3]: Single ended Clock has been set 1B (Enable) for either or both physical register is shown below.

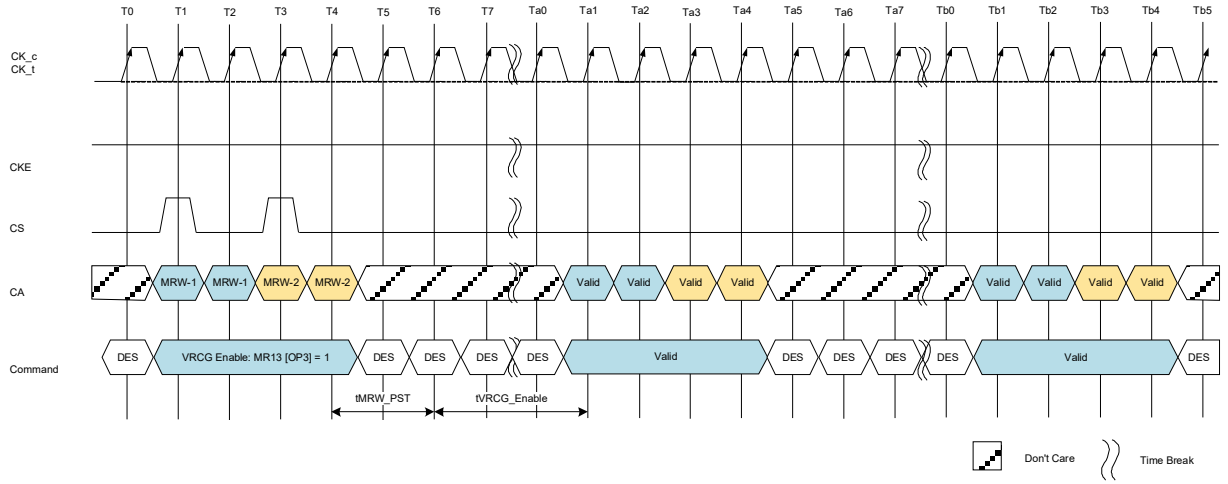



**Figure 139 - VRCG status change to high current mode: Single-ended Clock case**

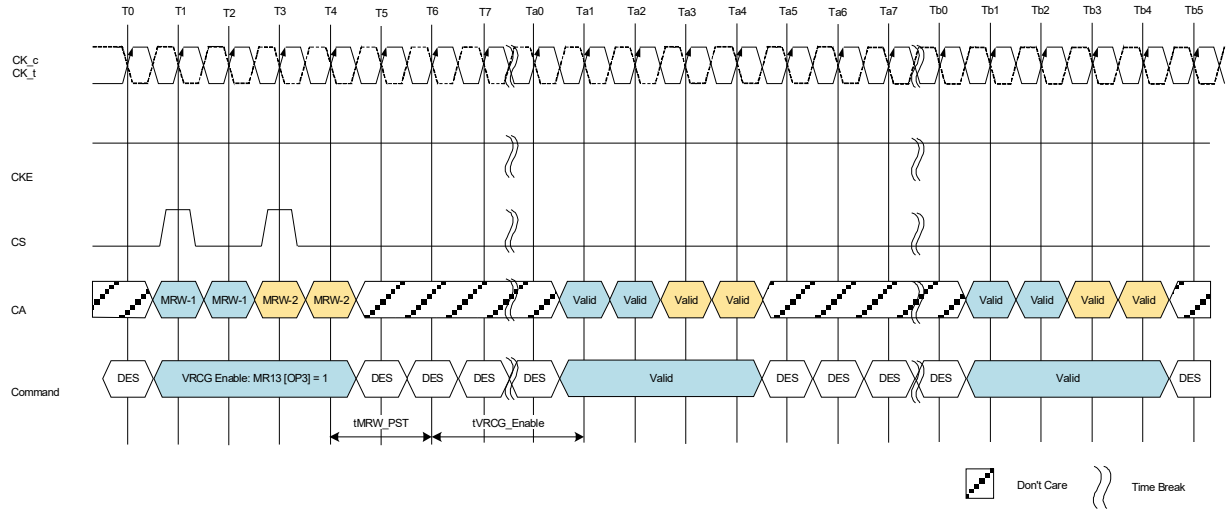



**Figure 140 - VRCG status change to high current mode : Differential Clock Case**

Notes

1. When Single-ended Clock is enabled on inactive mode register: MR51 OP[3].

**Table 88 - SE from/to Differential FSP and additional period for MRW AC timing**

| Parameter | Symbol | Min/Max | Data Rate (Equal to or less than 1600Mbps) | Unit | Note |
|---|---|---|---|---|---|
| Frequency Set Point Parameters for Switching Single-ended from/to Differential Clock/Strobe | | | | | |
| Valid Clock Requirement after entering FSP when changing between SE/Differential modes | tCKFSPE_SE | Min | Max(15ns, 8nCK) | - | |
| Valid Clock Requirement before first valid command after an FSP change between SE/ Differential modes | tCKFSPX_SE | Min | Max(15ns, 8nCK) | - | |
| Additional period for after MRW command | | | | | |
| Post Clock for MRW | tMRW_PST | Min | 2 | nCK | |

### 2.44.5. Command bus training procedure

DQS_c input level is required to "High" during tDQSCKE and CAENT period when the MR51 OP[2] : Single ended WDQS has been set 1B (Enable) for either physical register. This restriction is to prevent capturing unexpected DQS edge when SOC mode is moving from Diff. DQS mode to SE DQS mode and vice versa. The command bus training timing is shown below.

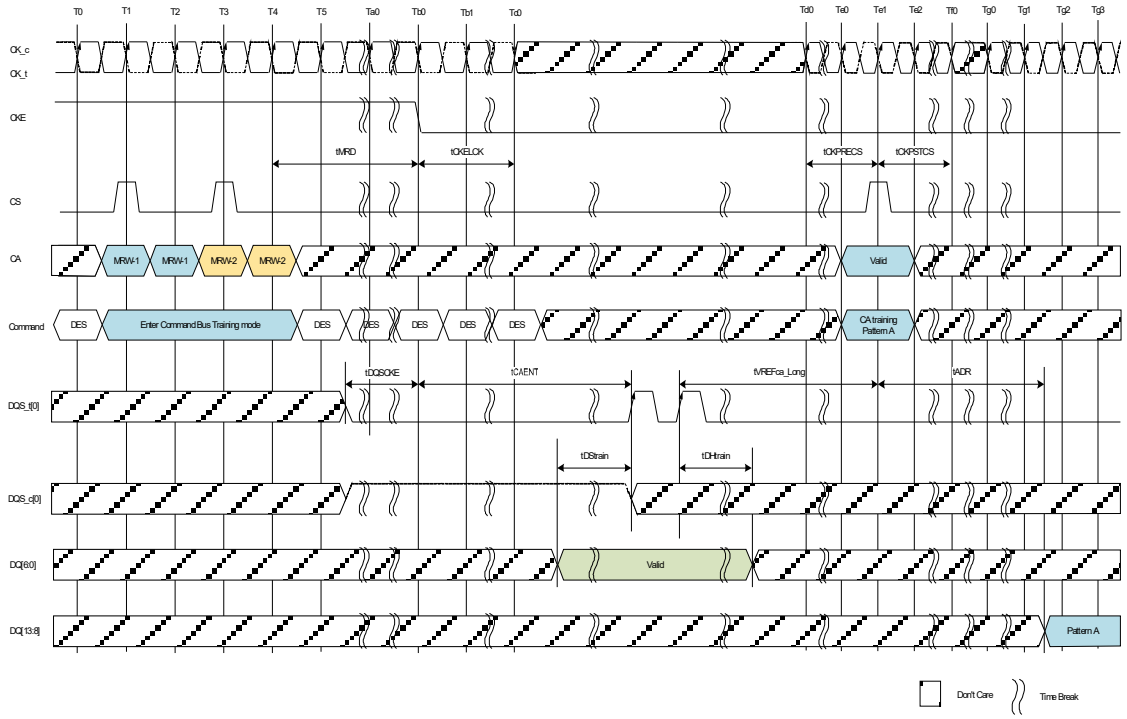



**Figure 141 - Write DQS mode changes from Differential to Single-ended for x16 device**

Notes

1. The status of following pins are don't care from T0 to Tg3: DQ[7], DQ[15:14], DMI[1:0], DQS_t[1] and DQS_c[1].

### 2.44.6. Mode Register Function with two physical registers

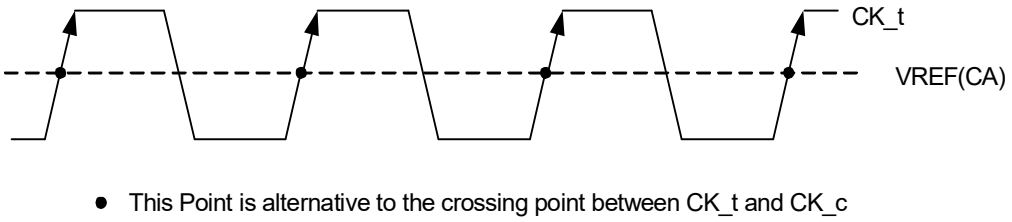
Parameters which have two physical registers controlled by FSP-WR and FSP-OP are shown in the following table with the exception as outlined in Note 1.

| MR# | Operand | Function | Note |
|---|---|---|---|
| MR1 | OP[2] | WR-PRE (WR Pre-amble Length) | |
| | OP[3] | RD-PRE (RD Pre-amble Type) | |
| | OP[6:4] | nWR (Write-Recovery for Auto-Pre-charge commands) | |
| | OP[7] | PST (RD Post-Amble Length) | |
| MR2 | OP[2:0] | RL (Read latency) | |
| | OP[5:3] | WL (Write latency) | |
| | OP[6] | WLS (Write Latency Set) | |
| MR3 | OP[0] | PU-Cal (Pull-up Calibration Point) | 1 |
| | OP[1] | WR PST(WR Post-Amble Length) | |
| | OP[5:3] | PDDS (Pull-Down Drive Strength) | |
| | OP[6] | DBI-RD (DBI-Read Enable) | |
| | OP[7] | DBI-WR (DBI-Write Enable) | |
| MR11 | OP[2:0] | DQ ODT (DQ Bus Receiver On-Die-Termination) | |
| | OP[6:4] | CA ODT (CA Bus Receiver On-Die-Termination) | |
| MR12 | OP[5:0] | VREF(ca) (VREF(ca) Setting) | |
| | OP[6] | VR-CA (VREF(ca) Range) | |
| MR14 | OP[5:0] | VREF(dq) (VREF(dq) Setting) | |
| | OP[6] | VR(dq) (VREF(dq) Range) | |
| MR21 | OP[5] | Low Speed CA buffer (Optional) | |
| MR22 | OP[2:0] | SoC ODT (Controller ODT Value for VOH calibration) | |
| | OP[3] | ODTE-CK (CK ODT enabled for nonterminating rank) | |
| | OP[4] | ODTE-CS (CS ODT enable for non terminating rank) | |
| | OP[5] | ODTD-CA (CA ODT termination disable) | |
| MR51 | OP[1] | SE_QE_RD (Single Ended Read DQS Enable) | |
| | OP[2] | SE_QE_WR (Single Ended Write DQS Enable) | |
| | OP[3] | SE_CE (Single Ended CK Enable) | |

Notes
1. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.

### 2.44.7. Reference level for Single-ended mode

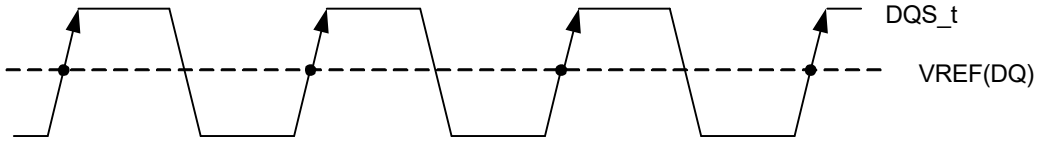
When Single-ended mode is enabled for Clock and Strobe, Each reference level is as follows. CK_t is referenced to VREF(CA) as the same as the command and the chip select and DQS_t is referenced to VREF(DQ) as the same as DQ and DMI.




- This Point is alternative to the crossing point between CK_t and CK_c

**Figure 142 - Reference point of CK_t**

Notes
1. VREFCA is calculated value based on VDD2 and MR12.
2. VrefCA must be set in following Opcode.
   MR12 OP[6] = 0, MR12 OP[5:0]= TBD through 110010B
   MR12 OP[6] = 1, MR12 OP[5:0]= TBD through 110010B




- This Point is alternative to the crossing point between DQS_t and DQS_c

**Figure 143 - Reference point of DQS_t**

Notes
1. VREFCA is calculated value based on VDDQ and MR14.
2. VrefCA must be set in following Opcode.
   MR12 OP[6] = 0, MR12 OP[5:0]= TBD through 110010B
   MR12 OP[6] = 1, MR12 OP[5:0]= TBD through 110010B

### 2.44.8. AC parameters for Single Ended (SE)

The AC timing is shown in Table is applied under conditions of Single ended mode.

**Table 89 - Delta CK and DQS Specification**

| Parameter | Symbol | Min/ Max | Data Rate Equal to or less than 1600Mbps | Unit | Note |
|---|---|---|---|---|---|
| CK single-ended input voltage | \|Vinse_CK_High - Vinse_CK_low\| | Min | 210 | mV | 1 |
| Rx timing window | tCIVW | Min | 0.35 | UI | 1,5 |
| Average High pulse width | tCH(avg) | Min | TBD | tCK(avg) | 1 |
| | | Max | TBD | tCK(avg) | 1 |
| Average Low pulse width | tCL(avg) | Min | TBD | tCK(avg) | 1 |
| | | Max | TBD | tCK(avg) | 1 |
| Absolute High clock pulse width | tCH(abs) | Min | TBD | tCK(avg) | 1 |
| | | Max | TBD | tCK(avg) | 1 |
| Absolute Low clock pulse width | tCL(abs) | Min | TBD | tCK(avg) | 1 |
| | | Max | TBD | tCK(avg) | 1 |
| Input Slew Rate for Clock | SRIN_CK | Min | TBD | V/ns | 1 |
| | | Max | TBD | V/ns | 1 |
| DQS single-ended input voltage | \|Vinse_DQS_High - Vinse_DQS_low\| | Min | 210 | mV | 2 |
| Input Slew Rate for DQS | SRIN_DQS | Min | 1 | V/ns | 2 |
| | | Max | 7 | V/ns | 2 |
| Rx timing window total | tDIVW | Min | 0.35 | UI | 2,6 |
| DQS Single-ended output high time (DBI-Disabled) | tQSH | Min | tCH-0.10 | tCK(avg) | 1,3 |
| DQS Single-ended output low time (DBI-Disabled) | tQSL | Min | tCL-0.10 | tCK(avg) | 1,3 |
| DQ output window time total, per pin (DBI-Disabled) | tQW | Min | 0.65 | UI | 6 |
| Write leveling setup time | tWLS | Min | 250 | ps | 4 |
| Write leveling hold time | tWLH | Min | 250 | ps | 4 |
| DQS falling edge to CK setup time | tDSS | Min | 0.3 | tCK(avg) | 4 |
| DQS falling edge hold time from CK | tDSH | Min | 0.3 | tCK(avg) | 4 |

Notes
1. This spec is applied when MR51 OP[3]=1B (single ended CK enabled)
2. This spec is applied when MR51 OP[2]=1B (single ended Write DQS enabled)
3. This spec is applied when MR51 OP[1]=1B (single ended Read DQS enabled)
4. This spec is applied when MR51 OP[3]=1B and MR51 OP[2]=0B or MR51 OP[3]=0B and MR51 OP[2]=1B.
5. UI=tCK
6. UI=tCK/2

## 2.45. Power Down Mode

### 2.45.1. Power Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOW while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- VREF(CA) Range and Value setting via MRW
- VREF(DQ) Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

And the LPDDR4 DRAM cannot be placed in power-down state during "Start DQS Interval Oscillator" operation.

CKE can go LOW while any other operations such as row activation, Precharge, Auto-Precharge, or Refresh are in progress. The power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 137.

Entering power-down deactivates the input and output buffers, excluding CKE and Reset_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable Low level and CA input level is don't care after CKE is driven LOW, this timing period is defined as tCKELCS. Clock input is required after CKE is driven LOW, this timing period is defined as tCKELCK. CKE LOW will result in deactivation of all input receivers except Reset_n after tCKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except Reset_n are "Don't Care". CKE LOW must be maintained until tCKE,min is satisfied.

No refresh operations are performed in power-down mode except Self Refresh power-down. The maximum duration in non-Self Refresh power-down mode is only limited by the refresh requirements outlined in the Refresh command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

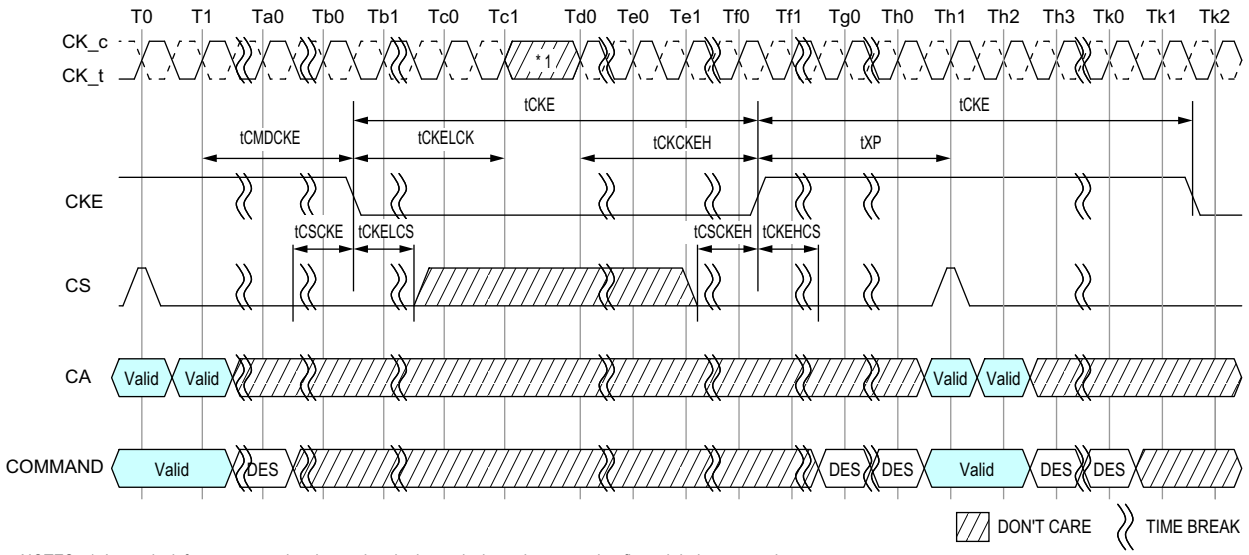
Clock frequency change or Clock Stop is inhibited during tCMDCKE, tCKELCK, tCKCKEH, tXP, tMRWCKEL and tZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down. if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And If power-down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh power-down in which the internal refresh is continuing in the same way as Self Refresh mode.

VDDQ may be turned off during power-down after tCKELCK(Max(5ns,5nCK)) is satisfied(Refer to Figure 137 about tCKELCK). Prior to

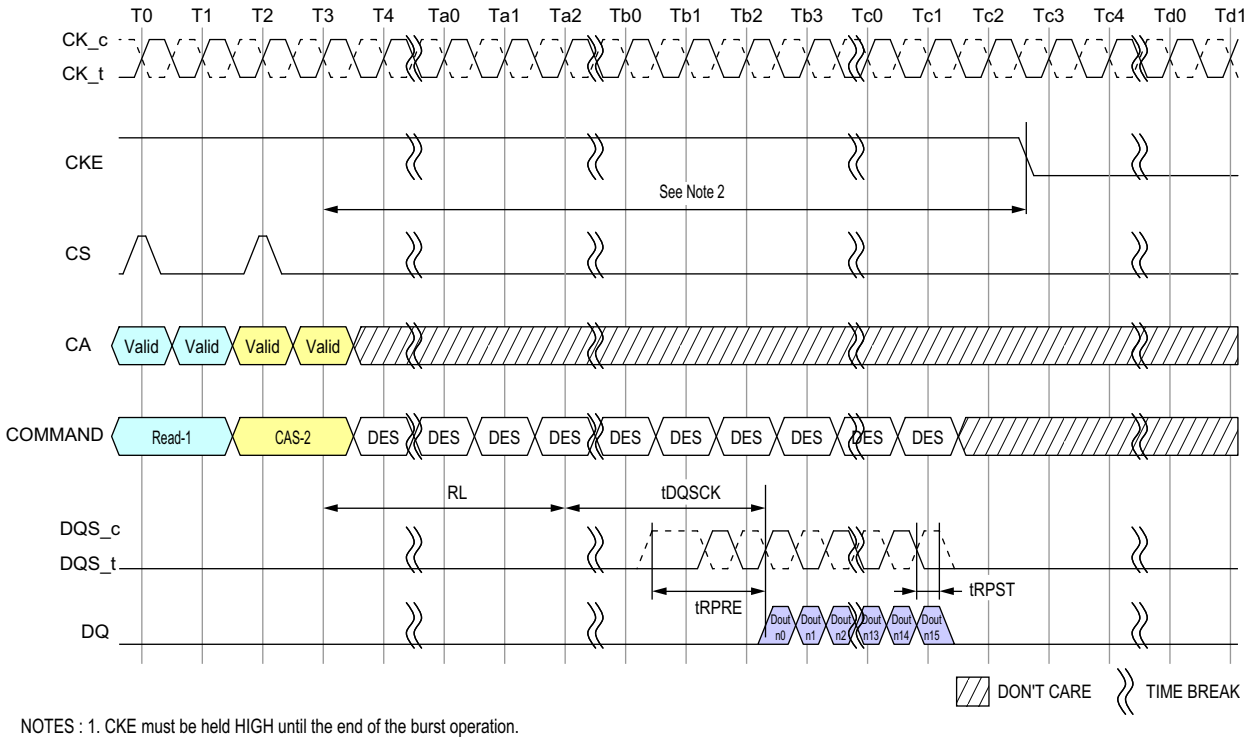
exiting power-down, $V_{DDQ}$ must be within its minimum/maximum operating range.

When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including power-down when VDDQ is stable and within its minimum/maximum operating range.




NOTES : 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

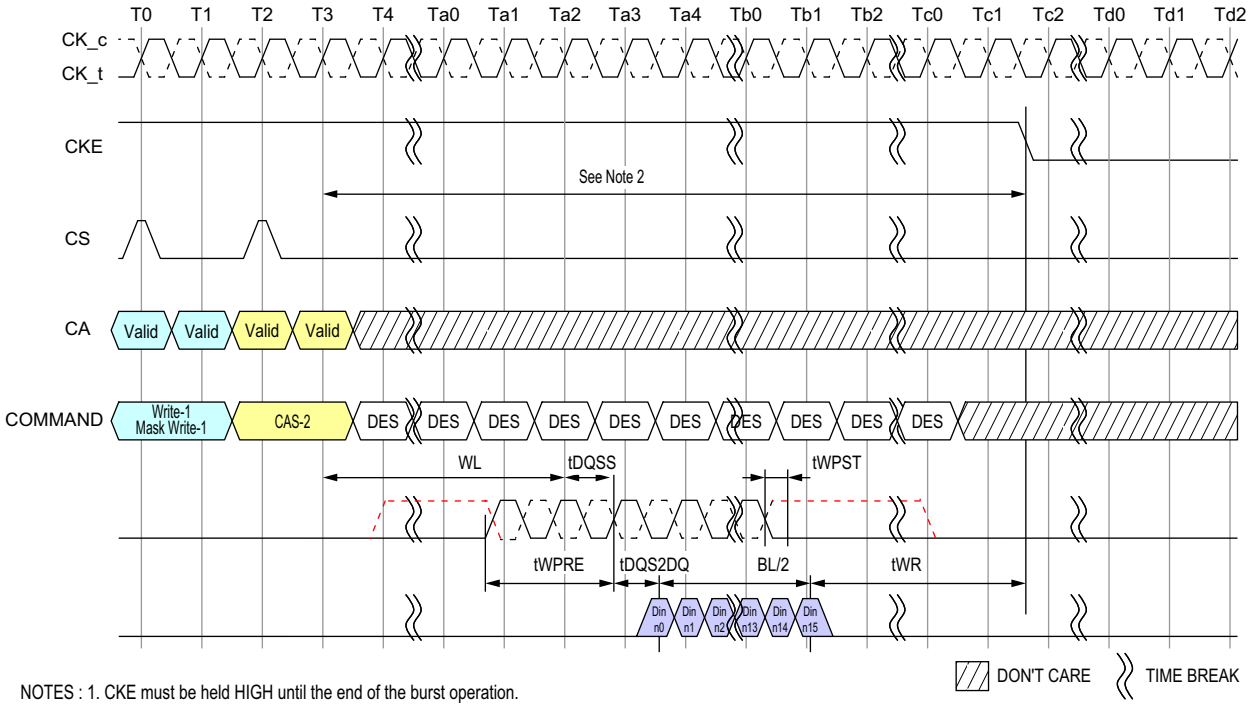
**Figure 144 - Basic Power-down Entry and Exit Timing**




NOTES : 1. CKE must be held HIGH until the end of the burst operation.

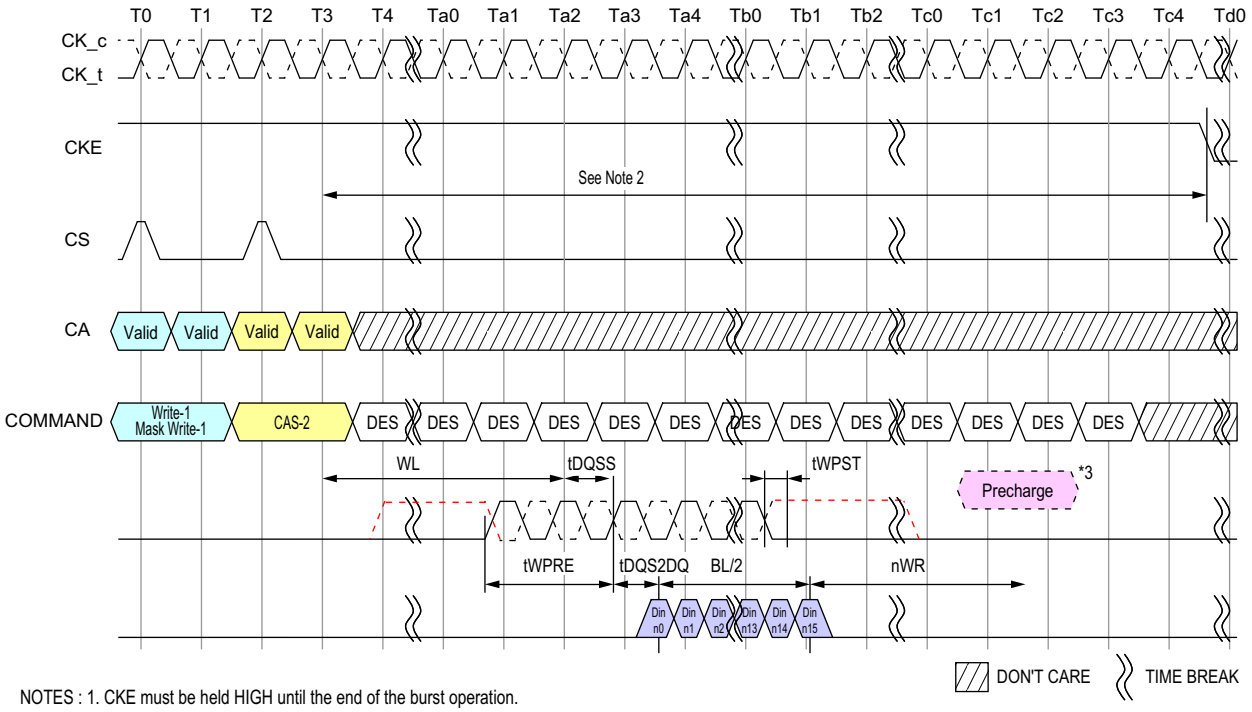
2. Minimum Delay time from Read Command or Read with Auto-Precharge Command to falling edge of CKE signal is as follows.
   Read Post-amble = 0.5nCK : MR1 OP[7]=[0] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 1tCK
   Read Post-amble = 1.5nCK : MR1 OP[7]=[1] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 2tCK

**Figure 145 - Read and Read with Auto-precharge to Power-Down Entry**



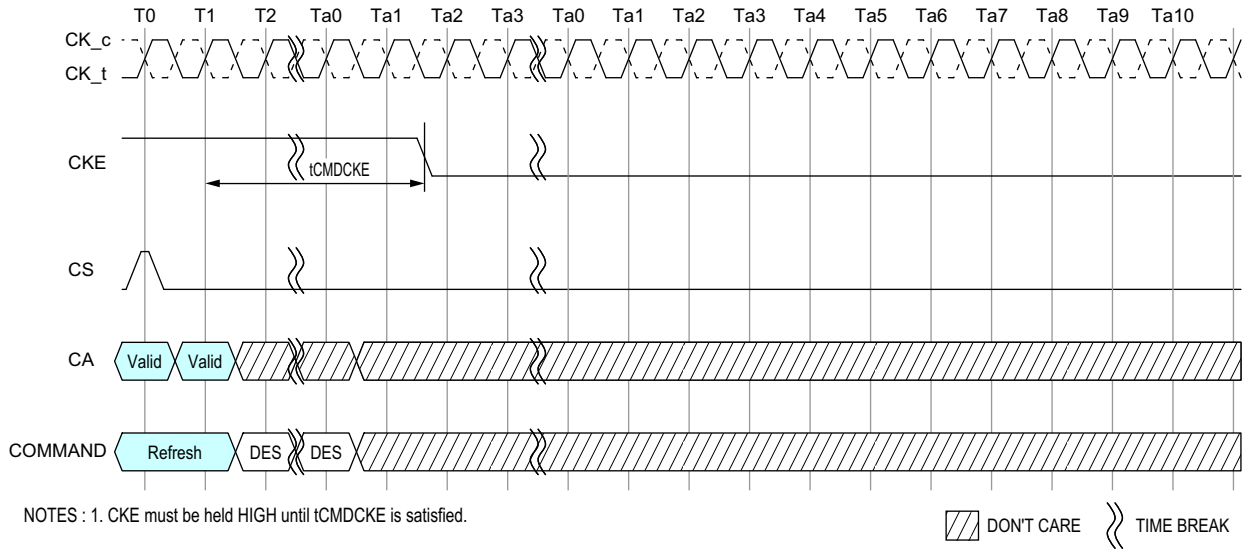

NOTES : 1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Write Command or Mask Write Command to falling edge of CKE signal is as follows.
(WL x tCK) + tDQSS(Max) + tDQS2DQ(Max) + ((BL/2) x tCK) + tWR
3. This timing is applied regardless of DQ ODT Disable/Enable setting: MR11[OP2:0].
4. This timing diagram only applies to the Write and Mask Write Commands without Auto-Precharge.

**Figure 146 - Write and Mask Write to Power-Down Entry**




NOTES : 1. CKE must be held HIGH until the end of the burst operation.
2. Delay time from Write with Auto-Precharge Command or Mask Write with Auto-Precharge Command to falling edge of CKE signal is more than (WL x tCK) + tDQSS(Max) + tDQS2DQ(Max) + ((BL/2) x tCK) + (nWR x tCK) + (2 x tCK)
3. Internal Precharge Command
4. This timing is applied regardless of DQ ODT Disable/Enable setting: MR11[OP2:0].

**Figure 147 - Write and Masked Write with Auto Precharge to Power-Down Entry**




NOTES : 1. CKE must be held HIGH until tCMDCKE is satisfied.

**Figure 148 - Refresh entry to Power-Down Entry**

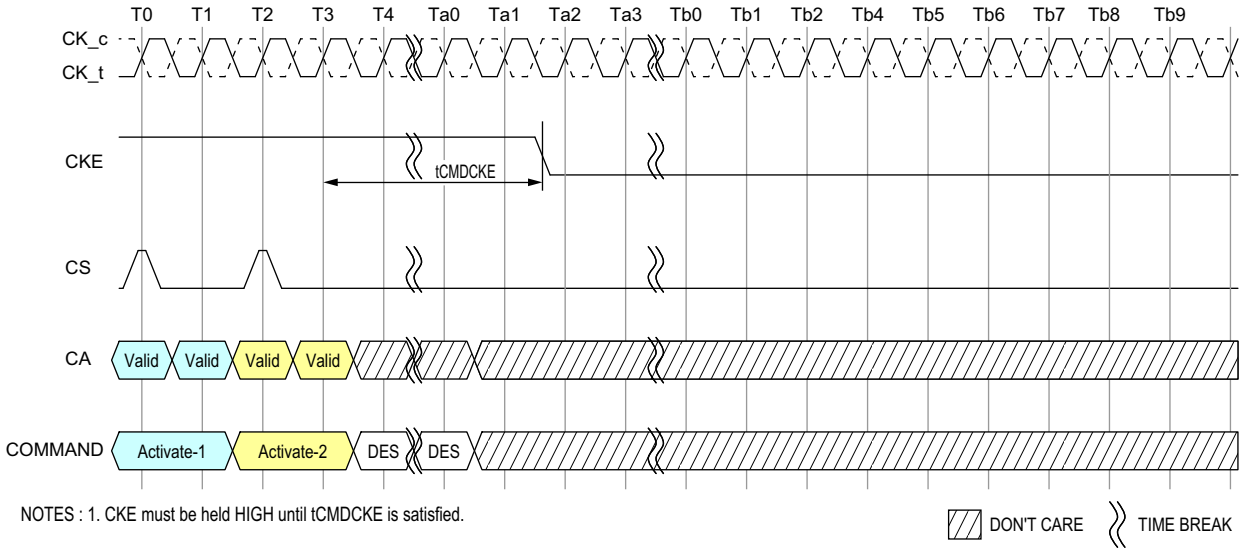



**Figure 149 - Activate Command to Power-Down Entry**

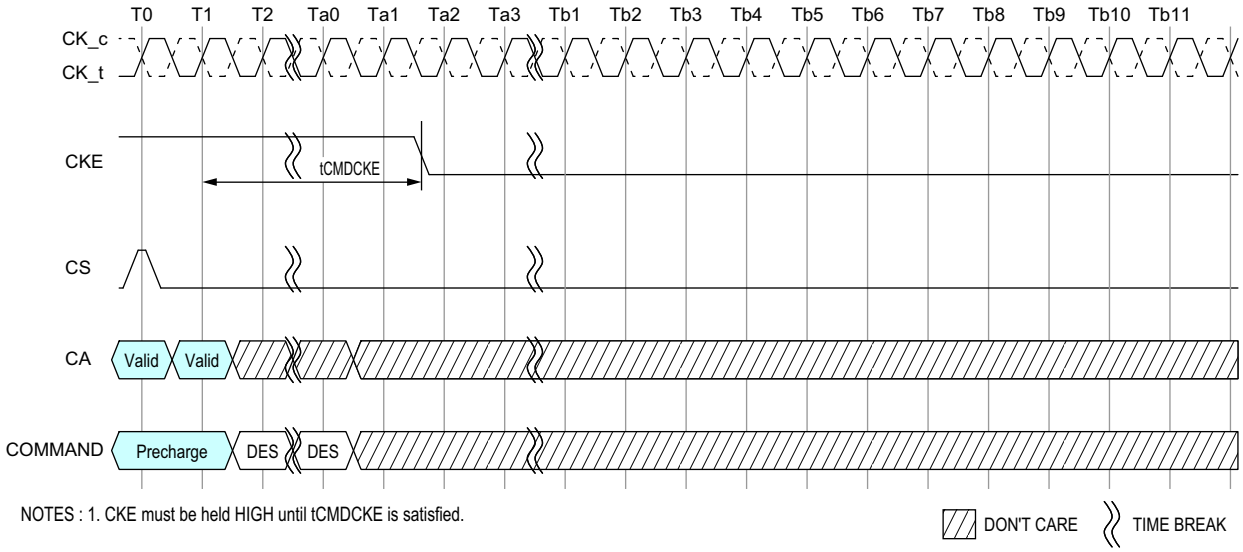
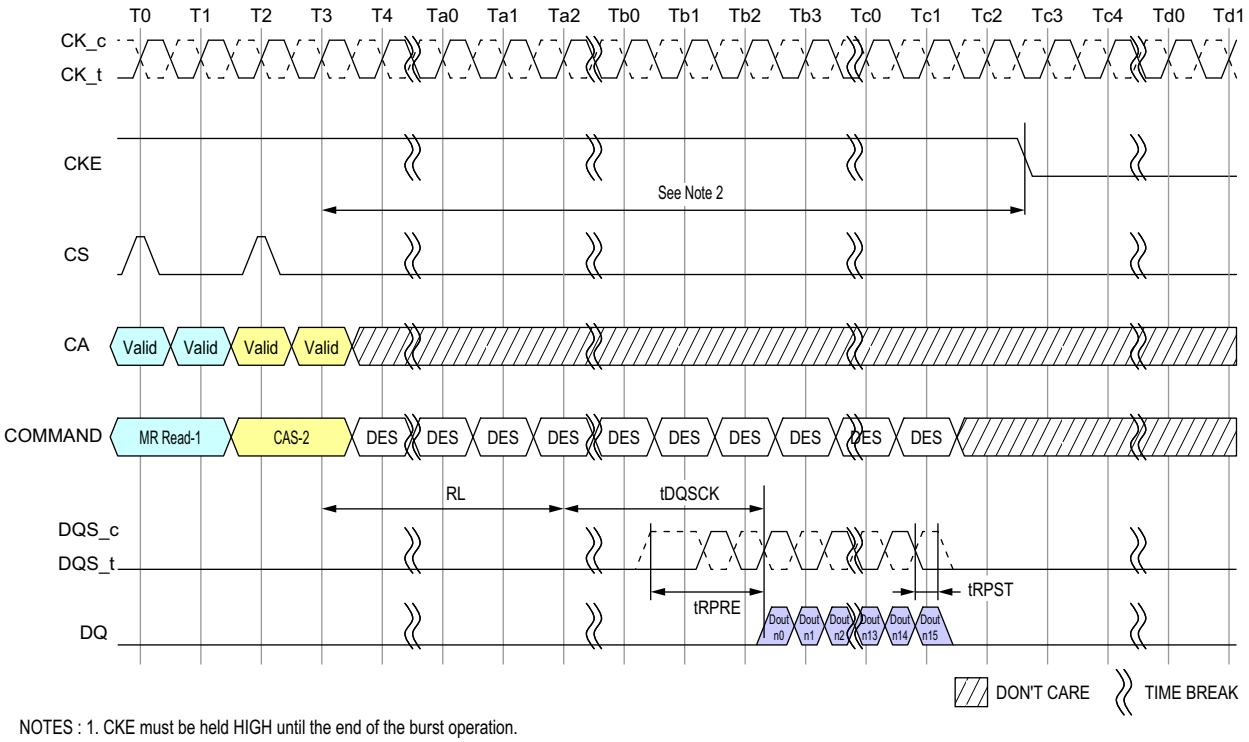
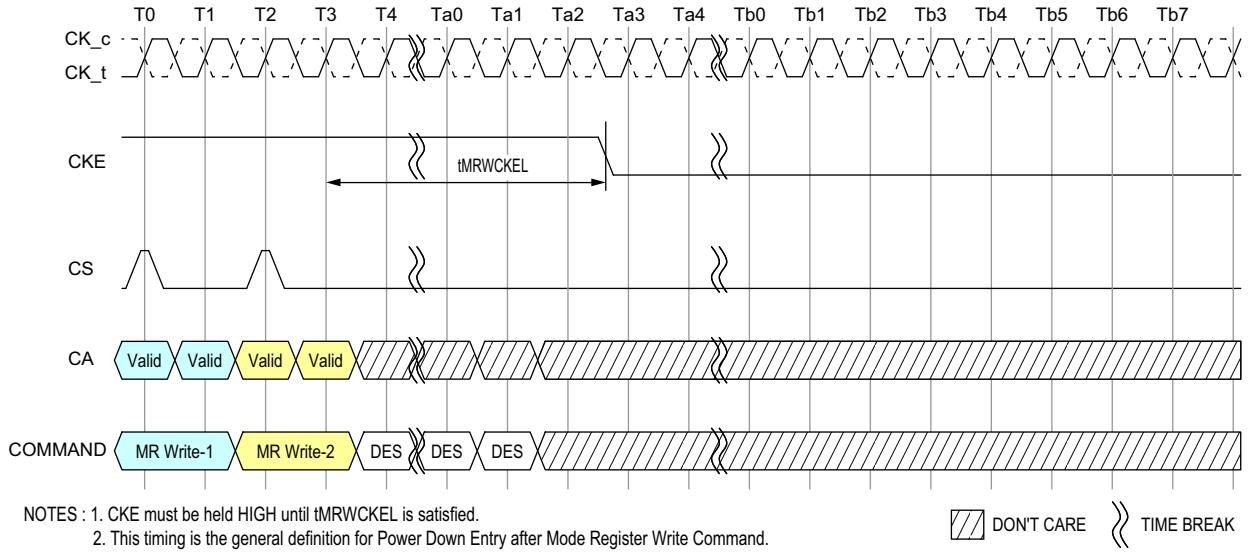



**Figure 150 - Precharge Command to Power-Down Entry**




NOTES : 1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Mode Register Read Command to falling edge of CKE signal is as follows:
Read Post-amble = 0.5nCK : MR1 OP[7]=[0] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 1tCK
Read Post-amble = 1.5nCK : MR1 OP[7]=[1] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 2tCK

**Figure 151 - Mode Register Read to Power-Down Entry**




NOTES : 1. CKE must be held HIGH until tMRWCKEL is satisfied.
2. This timing is the general definition for Power Down Entry after Mode Register Write Command.
When a Mode Register Write Command changes a parameter or starts an operation that requires special timing longer than tMRWCKEL, that timing must be satisfied before CKE is driven low.
Changing the Vref(DQ) value is one example, in this case the appropriate Vref_time-Short/Middle/Long must be satisfied.

**Figure 152 - MRW to Power-Down Entry**

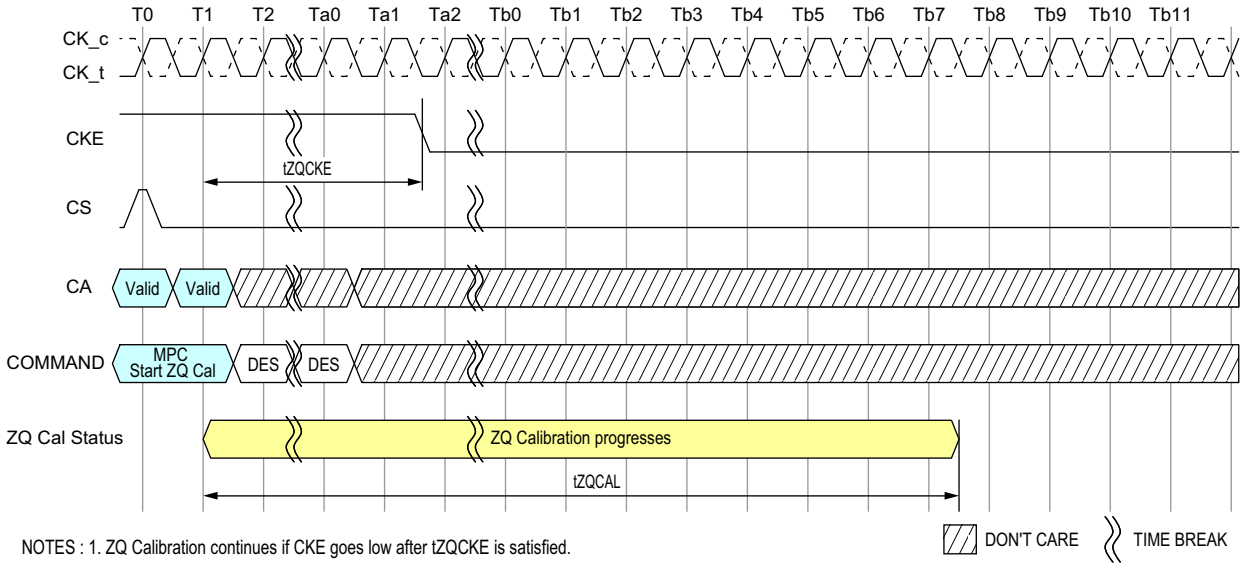



**Figure 153 - MPC ZQCAL_start to Power-Down Entry**

**Table 90 - Power Down AC Timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CKE minimum pulse width (HIGH and LOW pulse width) | tCKE | min | Max(7.5ns,4nCK) | | | | | | | | - | |
| Delay from valid command to CKE input LOW | tCMDCKE | min | Max(1.75ns,3nCK) | | | | | | | | ns | 1 |
| Valid Clock Requirement after CKE Input low | tCKELCK | min | Max(5ns,5nCK) | | | | | | | | ns | 1 |
| Valid CS Requirement before CKE Input Low | tCSCKE | min | 1.75 | | | | | | | | ns | |
| Valid CS Requirement after CKE Input low | tCKELCS | min | Max(5ns, 5nCK) | | | | | | | | ns | |
| Valid Clock Requirement before CKE Input High | tCKCKEH | min | Max(1.75ns, 3nCK) | | | | | | | | ns | 1 |
| Exit power- down to next valid command delay | tXP | min | Max(7.5ns, 5nCK) | | | | | | | | ns | 1 |
| Valid CS Requirement before CKE Input High | tCSCKEH | min | 1.75 | | | | | | | | ns | |
| Valid CS Requirement after CKE Input High | tCKEHCS | min | Max(7.5ns, 5nCK) | | | | | | | | ns | |
| Valid Clock and CS Requirement after CKE Input low after MRW Command | tMRWCKEL | min | Max(14ns, 10nCK) | | | | | | | | ns | 1 |
| Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command | tZQCKE | min | Max(1.75ns, 3nCK) | | | | | | | | ns | 1 |

Notes

1. Delay time has to satisfy both analog time(ns) and clock count(nCK).
   For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.
   The case which 3nCK is applied to is shown below.

For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown In Figure below.

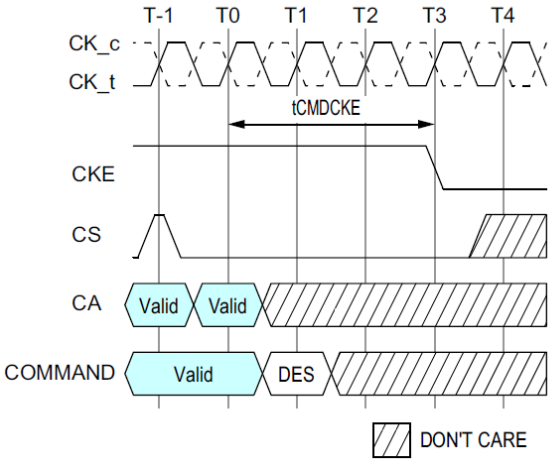



**Figure 154 - tCMDCKE Timing**

## 2.46. Input clock stop and frequency change

LPDDR4 SDRAMs support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of tCKELCK after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of tCKCKEH prior to CKE going HIGH

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE LOW under the following conditions:

- CK_t and CK_c are don't care during clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate or Precharge commands have executed to completion prior to stopping the clock;
- The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of tCKELCK after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of tCKCKEH prior to CKE going HIGH

LPDDR4 devices support input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Refresh requirements apply during clock frequency change;
- Any Activate, Read, Read with auto Precharge, Write, Write with auto Precharge, MPC(WRFIFO,RDFIFO, RDDQCAL), Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- CS shall be held LOW during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- The LPDDR4 SDRAM is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4 devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;

- CS shall be held LOW during clock clock stop;
- Refresh requirements apply during clock stop;
- During clock stop, only REFab or REFpb commands may be executing;
- Any Activate, Read, Write, MPC(WRFIFO,RDFIFO,RDDQCAL), Precharge, Mode Register Write or Mode Register Read commands must have executed to completion, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock;
- The related timing conditions (tRCD, tWR, tRP, tMRW, tMRR, tZQLAT, etc.) have been met prior to stopping the clock;
- Read with auto pre-charge and write with auto pre-charge commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations.
- REFab, REFpb, SRE, SRX and MPC(Zqcal Start)commands are required to have 4 additional clocks prior to stopping the clock same as CKE=L case.
- The LPDDR4 SDRAM is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

## 2.47. Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4 device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held High when the commands listed in the command truth table input.

### 2.47.1. Command Truth Table

| Command | SDR Command Pins | SDR CA Pins (6) | | | | | | CK_t edge | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| Deselect (DES) | L | X | | | | | | R1 | 1,2 |
| Multi Purpose Command (MPC) | H | L | L | L | L | L | OP6 | R1 | 1,9 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |
| Precharge (Per Bank, All Bank) | H | L | L | L | L | H | AB | R1 | 1,2,3,4 |
| | L | BA0 | BA1 | BA2 | V | V | V | R2 | |
| Refresh (Per Bank, All Bank) | H | L | L | L | H | L | AB | R1 | 1,2,3,4,14, 15 |
| | L | BA0 | BA1 | BA2 | RFM | V | V | R2 | |
| Self Refresh Entry | H | L | L | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Write-1 | H | L | L | H | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| Self Refresh Exit | H | L | L | H | L | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Mask Write-1 | H | L | L | H | H | L | L | R1 | 1,2,3,5,6,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| RFU | H | L | L | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Read-1 | H | L | H | L | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| CAS-2 (Write-2, Mask Write-2 , Read-2 or MRR-2, MPC) | H | L | H | L | L | H | C8 | R1 | 1,8,9 |
| | L | C2 | C3 | C4 | C5 | C6 | C7 | R2 | |
| RFU | H | L | H | L | H | L | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| RFU | H | L | H | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| MRW-1 | H | L | H | H | L | L | OP7 | R1 | 1,11 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| MRW-2 | H | L | H | H | L | H | OP6 | R1 | 1,11 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |

| Command | SDR Command Pins | SDR CA Pins (6) | | | | | | CK_t edge | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| MRR-1 | H | L | H | H | H | L | V | R1 | 1,2,12 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| RFU | H | L | H | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Activate-1 | H | H | L | R12 | R13 | R14 | R15 | R1 | 1,2,3,10 |
| | L | BA0 | BA1 | BA2 | R16 | R10 | R11 | R2 | |
| Activate-2 | H | R17 | R18 | R6 | R7 | R8 | R9 | R1 | 1,10,13 |
| | L | R0 | R1 | R2 | R3 | R4 | R5 | R2 | |

Notes

1. All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
5. Mask Write-1 command supports only BL 16. For Mark Write-1 comamnd, CA5 must be driven LOW on first rising clock cycle (R1).
6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.
13. In case of the densities which not to use R17 and R18 as row address, R17 and R18 must both be driven High for every ACT-2 command to maintain backward compatibility.
14. CA3 R2 edge is 'V' when RFM is not required, but becomes 'RFM' when read-only MR24 OP[0]=1B.
15. Issuing the RFMpb or RFMab command allows the LPDDR4 to use the command period for additional Refresh Management.

## 2.48. Refresh Management Command

### 2.48.1. Refresh Management Command Definition

Periods of high LPDDR4 SDRAM activity may require additional REFRESH commands to protect the integrity of the SDRAM data. LPDDR4 devices that require additional activity based refreshes include support for an Activation-based refresh management (RFM) command. The LPDRAM will indicate the requirement for additional Refresh Management (RFM) by setting read only MR24 opcode bit 0. OP[0]=0 indicates no additional refresh management is needed beyond the requirement in the Refresh section of the specification. OP[0]=1 indicates additional LPDRAM refresh management is required.

A suggested implementation of Refresh Management by the controller monitors ACT commands issued per bank to the LPDRAM. This activity can be monitored as a Rolling Accumulated ACT (RAA) count. Each ACT command will increment the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a DRAM vendor-specified Initial Management Threshold (RAAIMT), which is set by the DRAM vendor in the read only MR24 opcode bits 5:1 (Table 71), additional LPDRAM refresh management may be required. Executing the Refresh Management (RFM) command allows additional time for the LPDRAM to manage refresh internally. The RFM operation can be initiated to all banks on the LPDRAM with the RFMab command, or to a single bank with the RFMpb command.

The RFM command bits are the same as the REF command, except for CA3. If the Refresh Management Required bit is "0", (MR24 OP[0]=0), the state of CA3 will be ignored. If the Refresh Management Required bit is "1", (MR24 OP[0]=1), CA3="L" executes the REF command and CA3="H" executes either a RFMab command if CA5="H" or a RFMpb command if CA5="L".

**Table 91 - Refresh Management Parameters**

| Refresh Requirements | Symbol | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | 24Gb | 32Gb | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Refresh Management Cycle time (All Bank) | tRFMab | TBD | TBD | TBD | TBD | 210 | 280 | 280 | TBD | TBD | ns |
| Refresh Management Cycle time (per Bank) | tRFMpb | TBD | TBD | TBD | TBD | 170 | 190 | 190 | TBD | TBD | ns |

When an RFM command is issued to the LPDRAM, the RAA counter in any bank receiving the command can be decremented. The decrease in RAA count for an RFM command is determined by the RAAIMT multiplier value RAADEC, set by MR36 OP[1:0], as shown in Table 4. Issuing a RFMab command allows the RAA count in all banks to be decremented by the RAAIMT multiplied by the RAADEC value. Issuing an RFMpb command with BA[2:0] allows the RAA count only for the bank specified by BA[2:0] to be decremented by RAAIMT * RAADEC.

The RAA counter can only be decremented to a minimum RAA value of 0. No negative RAA value, or "pullin" of RFM commands, is allowed.

RFM commands are allowed to accumulate or "postpone", but the RAA counter shall never exceed the vendor specified RAA Maximum Management Threshold (RAAMMT), which is determined by multiplying the RAAIMT value by the RAAMULT value set by the DRAM vendor in read only MR24 OP[7:6]. If the RAA counter for a bank reaches RAAMMT, no additional ACT commands are allowed to that LPDRAM bank until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

RFM command scheduling shall meet the same minimum separation requirements as those for the REF command.

A RFM command does not replace the requirement for the controller to issue periodic REF commands to the LPDRAM. The RFM commands are supplemental time for the LPDRAM to manage refresh internally. Issuing a REF command allows the RAA counter to be decremented by RAAIMT for the bank or banks being refreshed. Hence, any periodic REF command issued to the LPDRAM allows the RAA counter of the banks being refreshed to be decremented by the RAAIMT value This would nominally occur once every effective Refresh interval (tREFIe), which is the average Refresh command interval currently being supplied to the SDRAM. This tREFIe must be equal to or less than the MR4 OP[4:0] RM x 3.906us. Issuing a REFab command allows the RAA count in all banks to be decremented. Issuing a REFpb command with a bank address allows the RAA count only with that bank address to be decremented. No decrement to the RAA count values is allowed for entering/exiting Self Refresh. The per bank count values before Self Refresh is entered will be the same upon Self Refresh exit.

Issuing an RFM command also allows decrementing of the RAA counter.

Devices which require Refresh Management may not require RFM at every refresh rate multiplier. The Refresh Management Threshold value RFMTH defines an effective refresh interval (tREFIe) above which Refresh Management is required. RFMTH is determined by the equation:
RFMTH = RAAIMT * tRC absolute min

Maximum interval between two REFab without RFM requirement is defined with following formula "tREFIe ? RFMTH". When RFMTH is longer than tRFEIe. Interval between two REFab defined in Table 116 and Table 117 “REFRESH Command Timing Constraints”, no RFM command is required even using max pullin and postpone.

Operation at any refresh rate slower (i.e. longer tREFIe) than that indicated by RFMTH requires RFM to ensure integrity of data stored in the LPDRAM. Operation at the tREFIe indicated by RFMTH, or operation at any higher refresh rate (i.e. shorter tREFIe) is exempt from RFM requirements regardless of any RAA count value.

Refresh Management Examples

Following are some operation examples to aid in understanding of the Refresh Management function. Values shown are hypothetical and may not represent values from any actual LPDDR4 SDRAM design now or in the future.

**Table 92 - RFM Operation Examples (One Bank)**

| Device-Specific RFM Requirements | | | | Current Device State | | Operating Requirements |
|---|---|---|---|---|---|---|
| RAAIMT | RAAMMT | RAADEC | RFMTH | tREFIe | RAA | |
| 160 | 4x | 2x | 9600ns (160*60ns) | 7.8us | 120 | No additional commands required, RAA<RAAIMT and tREFIe≤RFMTH |
| 160 | 4x | 2x | 9600ns | 7.8us | 500 | No additional commands required, tREFIe≤RFMTH |
| 160 | 4x | 2x | 9600ns | 15.6us | 120 | No additional commands required, RAA<RAAIMT |
| 160 | 4x | 2x | 9600ns | 15.6us | 500 | No additional commands required immediately since RAA<RAAMMT, but RAA is approaching RAAMMT so one or more RFM commands to this bank are recommended to prevent interruption of operation |
| 160 | 4x | 2x | 9600ns | 15.6us | 640 | RFM or REF command to this bank required before any activate command to this bank is legal, since RAA=RAAMMT. Issuing one RFMpb or RFMab command will reduce RAA to 320 since RAADEC=2x. Issuing one REFpb or REFab command will reduce RAA to 480. |
| 120 | 4x | 1.5x | 7200ns | 7.8us | 480 | RFM or REF command to this bank required before any activate command to this bank is legal, since RAA=RAAMMT. Issuing one RFMpb or RFMab command will reduce RAA to 300 since RAADEC=1.5x. Issuing one REFpb or REFab command will reduce RAA to 360. |

## 2.49. TRR Mode - Target Row Refresh

A LPDDR4 SDRAM's row has a limited number of times a given row can be accessed within a refresh period (tREFW * 2) prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive actives is the Target Row (TRn), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TRn, either the LPDRR4 SDRAM receive all (R * 2) Refresh Commands before another row activate is issued, or the LPDRR4 SDRAM should be placed into Targeted Row Refresh (TRR) mode. The TRR Mode will re-fresh the rows adjacent to the TRn that encountered tMAC limit.

If LPDDR4 SDRAM supports Unlimited MAC value: MR24 [OP2:0=000] and MR24 [OP3=1], Target Row Refresh operation is not required. Even though LPDDR4 SDRAM allows to set MR24 [OP7=1]: TRR mode enable, in this case LPDDR4 SDRAM's behavior is vendor specific. For example, a certain LPDDR4 SDRAM may ignore MRW command for entering/exiting TRR mode or a certain SDRAM may support commands related TRR mode. See vendor device datasheets for details about TRR mode definition at supporting Unlimited MAC value case.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the ac-tivates from the two target rows on a victim row in a bank should not exceed MAC value as well.

MR24 fields required to support the new TRR settings. Setting MR24 [OP7=1] enables TRR Mode and setting MR24 [OP7=0] disables TRR Mode. MR24 [OP6:OP4] defines which bank (BAn) the target row is located in (See MR24 table for details).

The TRR mode must be disabled during initialization as well as any other LPDRR4 SDRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR24 [OP7=0] to interrupt and reissue the TRR mode is allowed.

When enabled; TRR Mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus tMRD. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR24 [OP7=0]; if the TRR is exited via another MRS command, the value written to MR24 [OP6:OP4] are don’t cares.

### 2.49.1. TRR Mode Operation

1. The timing diagram in Figure "TRR Mode Timing Example" depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three cor-responding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. A Precharge All (PREA) commands issued while LPDRR4 SDRAM is in TRR mode will also perform precharge to BAn and counts towards a PREn command.

2. Prior to issuing the MRW command to enter TRR mode, the SDRAM should be in the idle state. A MRW command must be issued with MR24 [OP7=1] and MR24 [OP6:OP4] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.

3. No activity is to occur in the DRAM until tMRD has been satisfied. Once tMRD has been satis-fied, the only commands to BAn allowed are ACT and PRE until the TRR mode has been com-pleted.

4. The first ACT to the BAn with the TRn address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until [(1.5 * tRAS) + tRP] is satisfied.

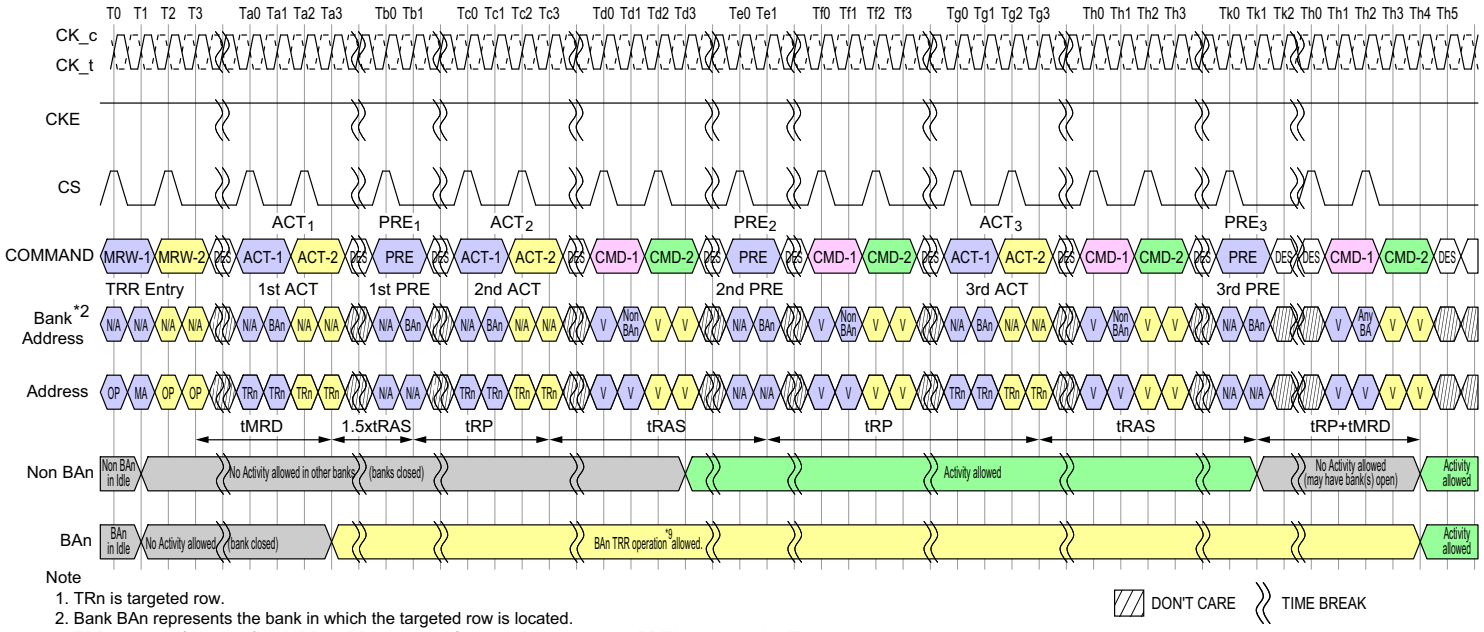
5. After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued (1.5 * tRAS) later; and then followed tRP later by the second ACT to the BAn with the TRn address. Once the 2nd activate to the BAn is issued, nonBAn banks are allowed to have activity.

6. After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the TRn address.

7. After the third ACT to the BAn with the TRn address is issued, a PRE to BAn would be issued tRAS later; and once the third PRE has been issued, nonBAn bank groups are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMRD is satisfied.

8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any-time the TRR mode is interrupted and not completed, the interrupted TRR Mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, an MR24 change is required with setting MR24 [OP7=0], MR24 [OP6:OP4] are don't care, followed by three PRE to BAn, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.

9. Refresh command to the LPDRR4 SDRAM or entering Self-Refresh mode is not allowed while the DRAM is in TRR mode.




Note
1. TRn is targeted row.
2. Bank BAn represents the bank in which the targeted row is located.
3. TRR mode self-clears after tMRD + tRP measured from 3rd BAn precharge PRE3 at clock edge Th4.
4. TRR mode or any other activity can be re-engaged after tRP + tMRD from 3rd BAn precharge PRE3.
   PRE_ALL also counts if issued instead of PREn. TRR mode is cleared by DRAM after PRE3 to the BAn bank.
5. Activate commands to BAn during TRR mode do not provide refreshing support, i.e. the Refresh counter is unaffected.
6. The DRAM must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) neccessary to meet refresh requirements.
7. A new TRR mode must wait tMRD+tRP time after the third precharge.
8. BAn may not be used with any other command.
9. ACT and PRE are the only allowed commands to BAn during TRR Mode.
10. Refresh commands are not allowed during TRR mode.
11. All DRAM timings are to be met by DRAM during TRR mode such as tFAW. Issuing of ACT1, ACT2 and ACT3 counts towards tFAW budget.

**Figure 155 - TRR Mode Timing Example**

## 2.50. Post Package Repair - PPR

LPDDR4 supports Fail Row address repair as an optional feature and it is readable through MR25 OP[7:0].
PPR provides simple and easy repair method in the system and Fail Row address can be repaired by the electrical programming of Electrical-fuse scheme.

With PPR, LPDDR4 can correct 1Row per Bank.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended the PPR mode entry and repair.

### 2.50.1. Fail Row Address Repair

The following is procedure of PPR.

1. Before entering 'PPR' mode, All banks must be Precharged
2. Enable PPR using MR4 bit "OP4=1" and wait tMRD
3. Issue ACT command with Fail Row address
4. Wait tPGM to allow DRAM repair target Row Address internally then issue PRE
5. Wait tPGM_Exit after PRE which allow DRAM to recognize repaired Row address RAn
6. Exit PPR with setting MR4 bit "OP4=0"
7. Issue RESET command after tPGMPST
8. Repeat steps in '3.3.2 Reset Initialization with Stable Power' section
9. In More than one fail address repair case, Repeat Step 2 to 8

Once PPR mode is exited, to confirm if target row is repaired correctly, host can verify by writing data into the target row and reading it back after PPR exit with MR4 [OP4=0] and tPGMPST.

The following Timing diagram show PPR related MR bits and its operation.

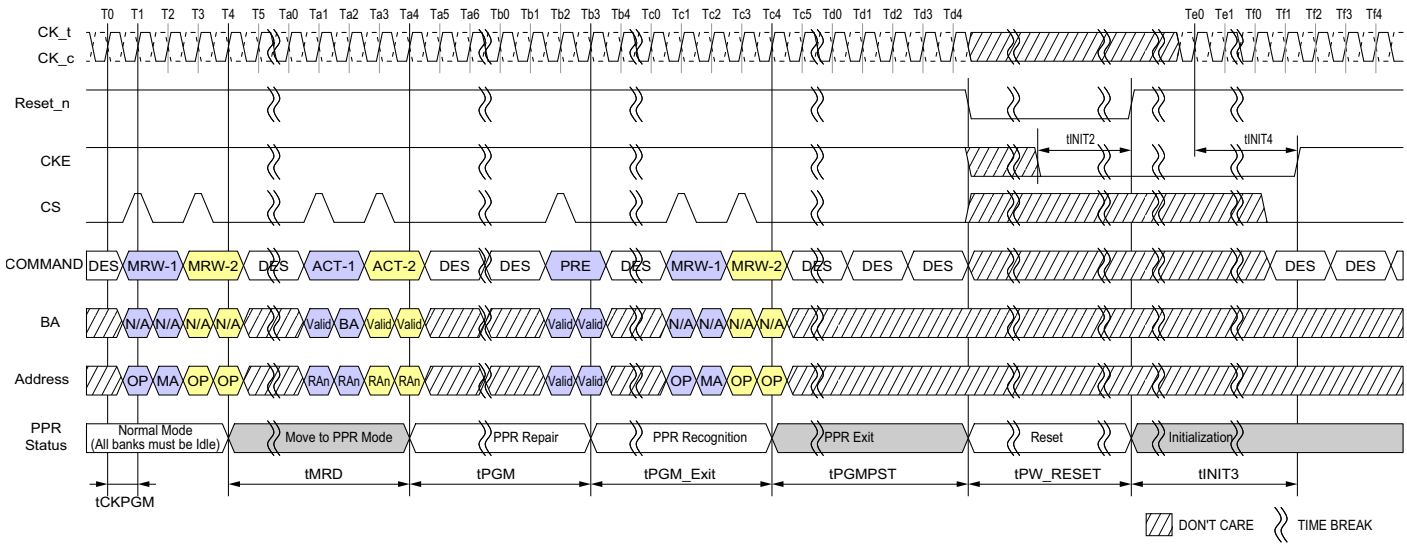



**Figure 156 - PPR Timing**

Notes

1. During tPGM, any other commands (including refresh) are not allowed on each die.
2. With one PPR command, only one row can be repaired at one time per die.
3. RESET command is required at the end of every PPR procedure.
4. During PPR, memory contents is not refreshed and may be lost.
5. Assert Reset_n below 0.2 X $V_{DD2}$. Reset_n needs to be maintained LOW for minimum tPW_RESET. CKE must be pulled LOW at least 10ns before deassserting Reset_n.
6. After RESET command, follow steps 4 to 10 in 'Voltage Ramp and Device Initialization' section.
7. Only DES command is allowed during tMRD.

**Table 93 - PPR Timing Parameters**

| Parameter | Symbol | min | max | Unit | Note |
|---|---|---|---|---|---|
| PPR Programming Time | tPGM | 1000 | - | ms | |
| PPR Exit Time | tPGM_Exit | 15 | - | ns | |
| New Address Setting time | tPGMPST | 50 | - | us | |
| PPR Programming Clock | tCKPGM | 1.25 | - | ns | |

# 3. Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 94 - Absolute Maximum DC Ratings**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| VDD1 supply voltage relative to VSS | VDD1 | -0.4 | 2.1 | V | 1 |
| VDD2 supply voltage relative to VSS | VDD2 | -0.4 | 1.4 | V | 1 |
| VDDQ supply voltage relative to VSSQ | VDDQ | -0.4 | 1.4 | V | 1 |
| Voltage on Any Pin except VDD1 relative to VSS | VIN, VOUT | -0.4 | 1.4 | V | |
| Storage Temperature | TSTG | -55 | 125 | °C | 2 |

Notes
1. See the section 1.3. "Power-up and Initialization" and 1.3.3. "Power-off Sequence" for information about relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, please refer to JESD51-2 standard.

# 4. AC and DC Operating Conditions

## 4.1. Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Core Power 1 | VDD1 | 1.70 | 1.80 | 1.95 | V | 1,2 |
| Core Power 2 / Input Buffer Power | VDD2 | 1.06 | 1.10 | 1.17 | V | 1,2,3 |
| I/O Buffer Power | VDDQ | 0.57 | 0.6 | 0.65 | V | 2,3,4,5 |

Notes
1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20 MHz exceeding a pk-pk tolerance of 45 mV at the DRAM ball is not included in the TdIVW.
4. VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.
5. Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

## 4.2. Input Leakage Current

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Leakage current | $I_L$ | -4 | 4 | uA | 1,2 |

Notes
1. For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

## 4.3. Input/Output Leakage Current

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input/Output Leakage current | $I_{OZ}$ | -5 | 5 | uA | 1,2 |

Notes
1. For DQ, DQS_t, DQS_c and DMI. Any I/O 0V ≤ VOUT ≤ VDDQ.
2. I/Os status are disabled: High Impedance and ODT Off.

## 4.4. Operating Temperature

| Parameter | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Temperature | Standard | $T_{OPER}$ | -25 | 85 | °C | 1 |
| | Extended | | 85 | 105 | | 1 |

Notes
1. Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Some applications require operation of LPDDR4 in the maximum temperature conditons in the Elevated Temperature Range between 85°C and 105°C case temperature. For LPDDR4 devices, derating may be neccessary to operate in this range.
   See MR4 on the section 1.4. "Mode Register Definition"
3. Either the device case temperature rating or the temperature sensor (See the section of "Temperature Sensor") may be used to set an appro priate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

# 5. AC and DC Input Measurement Levels

## 5.1. 1.1V High speed LVCMOS (HS_LLVCMOS)

### 5.1.1. Standard specifications

All voltages are referenced to ground except where noted.

### 5.1.2. DC electrical characteristics

#### 5.1.2.1. Input Level for CKE

This definition applies to CKE_A/B.

**Table 95 - LPDDR4 Input level for CKE**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high level (AC) | VIH(AC) | 0.75*VDD2 | VDD2+0.2 | V | 1 |
| Input low level (AC) | VIL(AC) | -0.2 | 0.25*VDD2 | V | 1 |
| Input high level (DC) | VIH(DC) | 0.65*VDD2 | VDD2+0.2 | V | |
| Input low level (DC) | VIL(DC) | -0.2 | 0.35*VDD2 | V | |

Notes
1. Refer to LPDDR4 AC Over/Undershoot section.

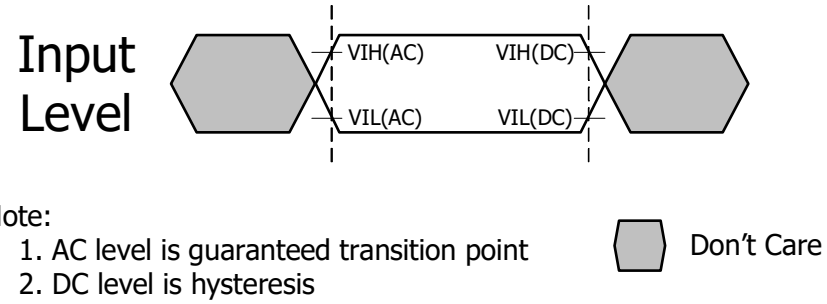



**Figure 157 - Input AC timing definition for CKE**

### 5.1.2.2. LPDDR4 Input Level for Reset_n and ODT_CA

This definition applies to Reset_n and ODT_CA.

**Table 96 - LPDDR4 Input AC timing definition for Reset_n and ODT_CA**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high level | VIH | 0.8*VDD2 | VDD2+0.2 | V | 1 |
| Input low level | VIL | -0.2 | 0.20*VDD2 | V | 1 |

Notes
1. Refer to LPDDR4 AC Over/Undershoot section.

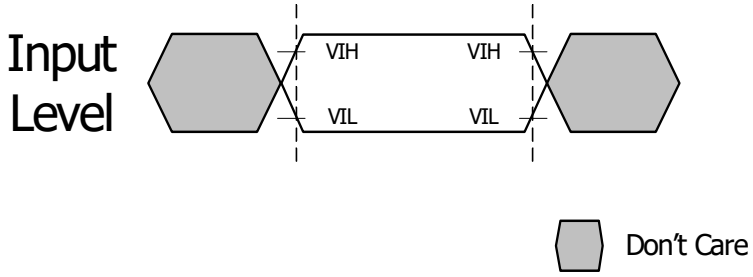



**Figure 158 - Input AC timing definition**

### 5.1.3. AC Over/Undershoot

#### 5.1.3.1. LPDDR4 AC Over/Undershoot

**Table 97 - LPDDR4 AC Over/Undershoot**

| Parameter | Specification | Units |
|---|---|---|
| Maximum peak amplitude allowed for overshoot area | 0.35 | V |
| Maximum peak amplitude allowed for undershoot area | 0.35 | V |
| Maximum overshoot area above VDD/VDDQ | 0.8 | V-ns |
| Maximum undershoot area below VSS/VSSQ | 0.8 | V-ns |

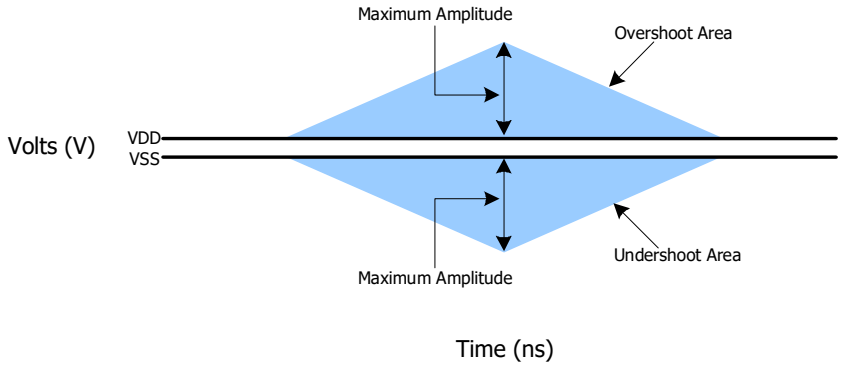



**Figure 159 - AC Overshoot and Undershoot Definition for Address and Control Pins**

## 5.2. Differential Input Voltage

### 5.2.1. Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

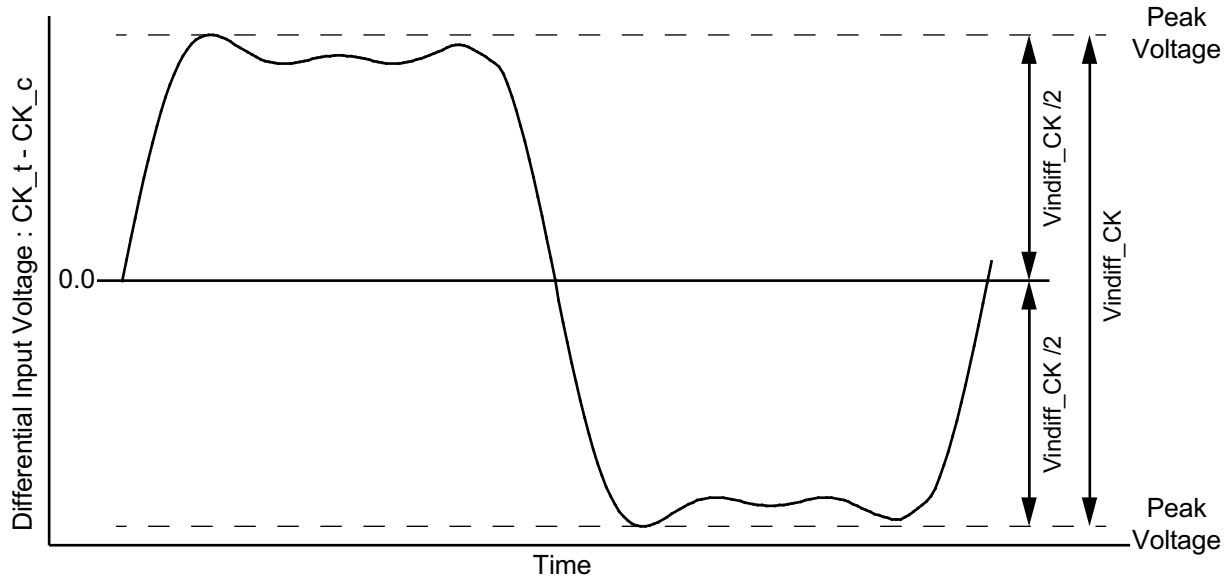



**Figure 160 - CK Differential Input Voltage**

**Table 98 - CK differential input voltage**

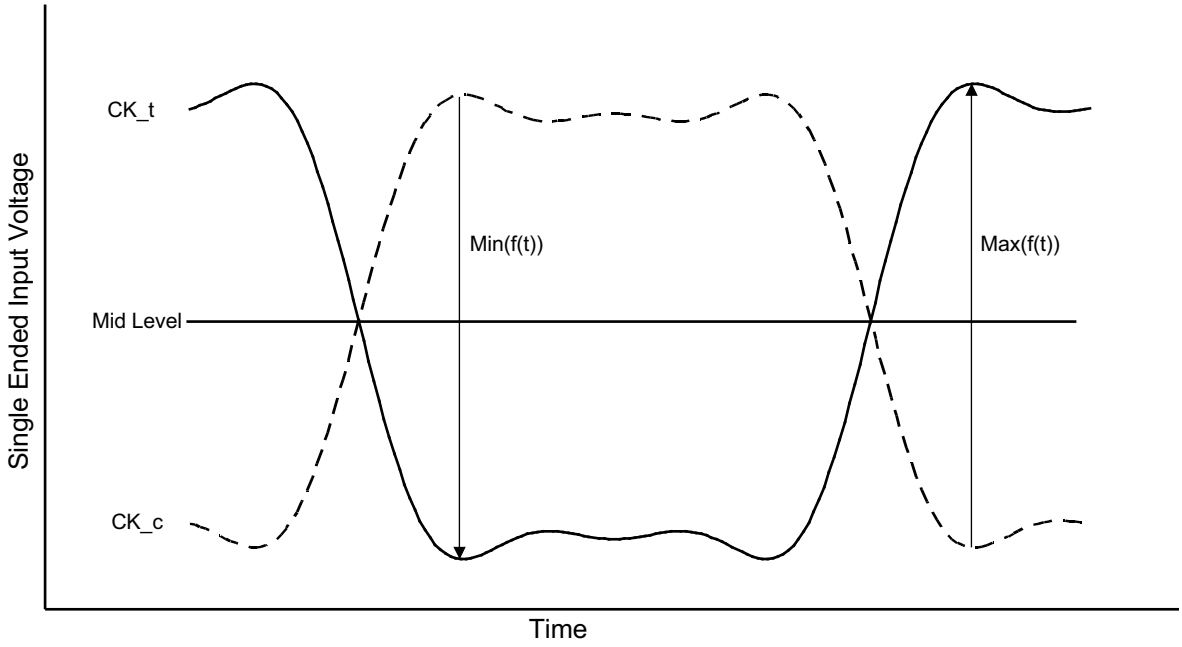
| Parameter | Symbol | Data Rate | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| CK differential input voltage | Vindiff_CK | 420 | - | 380 | - | 360 | - | mV | 1,2 |

Notes
1. These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column,1600/1867.
2. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VCK_t - VCK_c

### 5.2.2. Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in a following equation.

**VIH.DIFF.Peak Voltage = Max(f(t))**
**VIL.DIFF.Peak Voltage = Min(f(t))**
**f(t) = VCK_t - VCK_c**

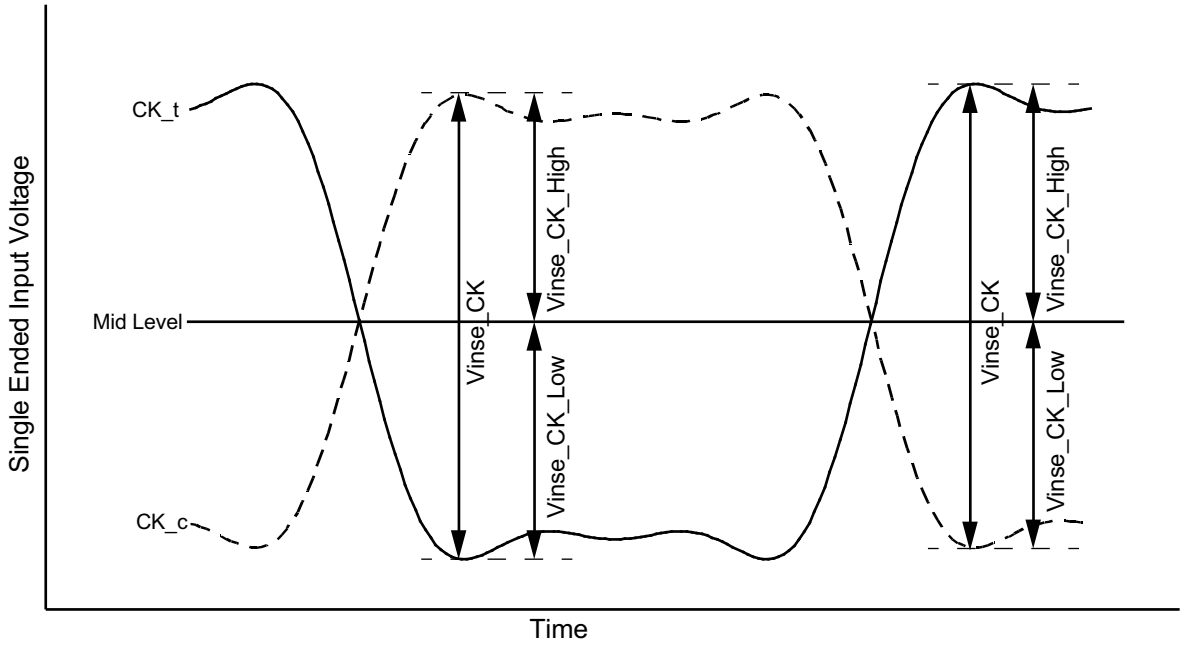



NOTES : 1. $V_{REF}CA$ is LPDDR4 SDRAM internal setting value by $V_{REF}$ Training.

**Figure 161 - Definition of differential Clock Peak Voltage**

### 5.2.3. Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.




NOTES : 1. $V_{REF}CA$ is LPDDR4 SDRAM internal setting value by $V_{REF}$ Training.

**Figure 162 - Clock Single-Ended Input Voltage**

**Table 99 - Clock Single-Ended input voltage**

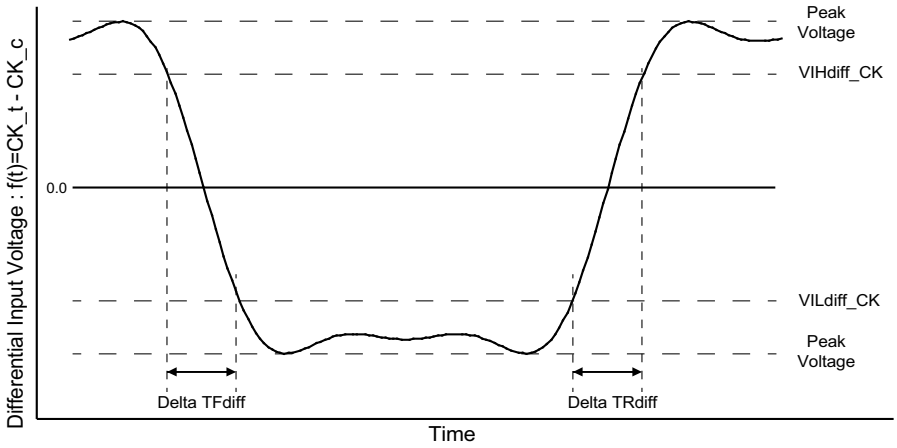
| Parameter | Symbol | Data Rate | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Clock Single-Ended input voltage | Vinse_CK | 210 | - | 190 | - | 180 | - | mV | 1 |
| Clock Single-Ended input voltage High from $V_{REF}DQ$ | Vinse_CK_High | 105 | - | 95 | - | 90 | - | mV | 1 |
| Clock Single-Ended input voltage Low from $V_{REF}DQ$ | Vinse_CK_Low | 105 | - | 95 | - | 90 | - | mV | 1 |

Notes

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

### 5.2.4. Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure below and the following Tables.




NOTES : 1. Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2. Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

**Figure 163 - Differential Input Slew Rate Definition for CK_t, CK_c**

**Table 100 - Differential Input Slew Rate Definition for CK_t, CK_c**

| Description | From | To | Defined by |
|---|---|---|---|
| Differential input slew rate for rising edge(CK_t - CK_c) | VILdiff_CK | VIHdiff_CK | \|VILdiff_CK - VIHdiff_CK\|/DeltaTRdiff |
| Differential input slew rate for falling edge(CK_t - CK_c) | VIHdiff_CK | VILdiff_CK | \|VILdiff_CK - VIHdiff_CK\|/DeltaTFdiff |

**Table 101 - Differential Input Level for CK_t, CK_c**

| Parameter | Symbol | Data Rate | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input High | VIHdiff_CK | 175 | - | 155 | - | 145 | - | mV | 1 |
| Differential Input Low | VILdiff_CK | - | -175 | - | -155 | - | -145 | mV | 1 |

Notes
1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

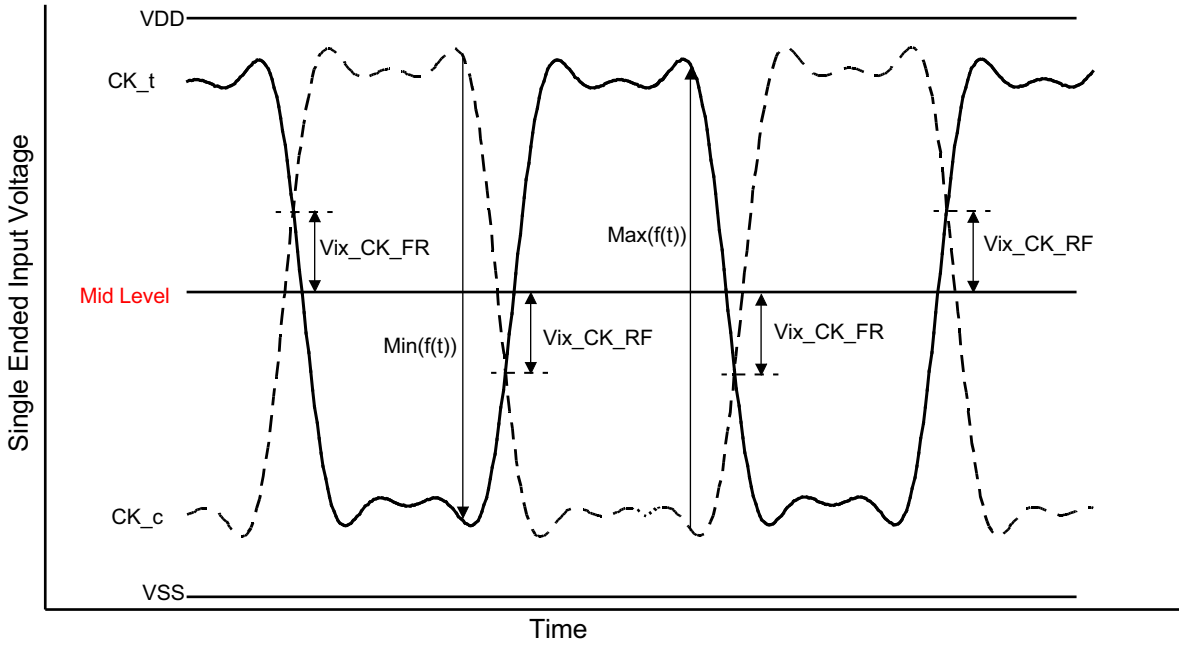
**Table 102 - Differential Input Slew Rate for CK_t, CK_c**

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867 | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input Slew Rate for Clock | SRIdiff_CK | 2 | 14 | 2 | 14 | 2 | 14 | V/ns | |

### 5.2.5. Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.

**Figure 164 - Vix Definition (Clock)**




NOTES : 1. The base level of Vix_CK_FR/RF is $V_{REF}$CA that is LPDDR4 SDRAM internal setting value by $V_{REF}$ Training.

**Table 103 - Cross point voltage for differential input signals (Clock)**

| Parameter | Symbol | Data Rate | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Clock Differential input cross point voltage ratio | Vix_CK_ratio | - | 25 | - | 25 | - | 25 | % | 1,2,3, 4,5 |

Notes
1.The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
3. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
4. Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
   Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
5. In LPDDR4X un-terminated case, CK mid-level is calculated as : High level?VDDQ, Low level=VSS, Mid-level = VDDQ/2.
   In LPDDR4 un-terminated case, Mid-level must be equal or lower than 369mV (33.6% of VDD2).

### 5.2.6. Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

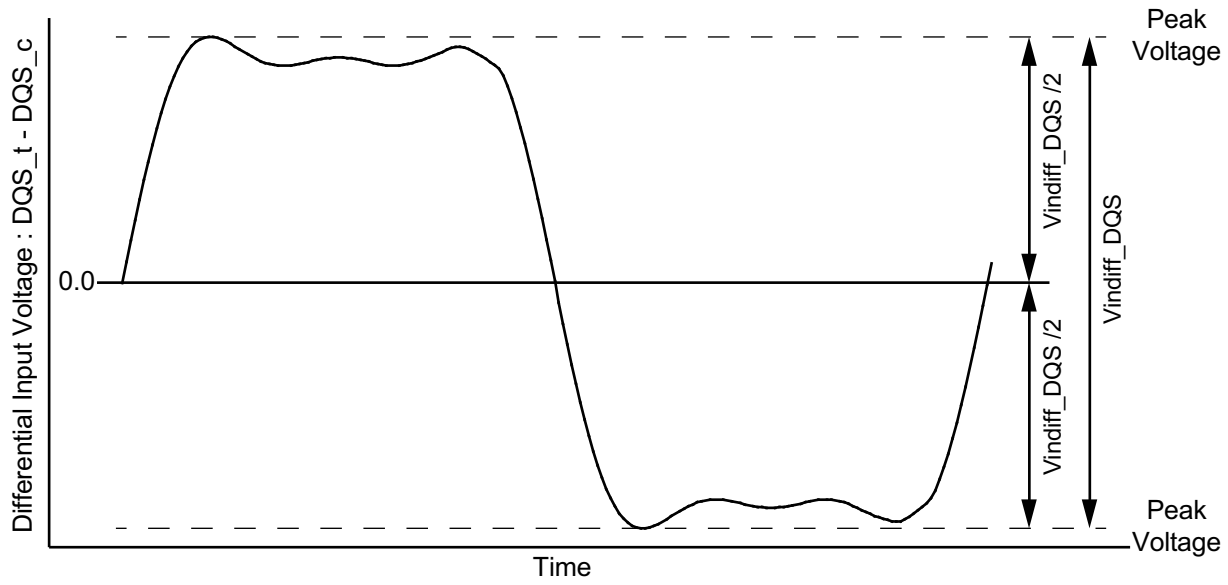



**Figure 165 - DQS Differential Input Voltage**

**Table 104 - DQS differential input voltage**

| Parameter | Symbol | Data Rate | | | | | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS differential input | Vindiff_DQS | 360 | - | 360 | - | 340 | - | mV | 1 |

Notes

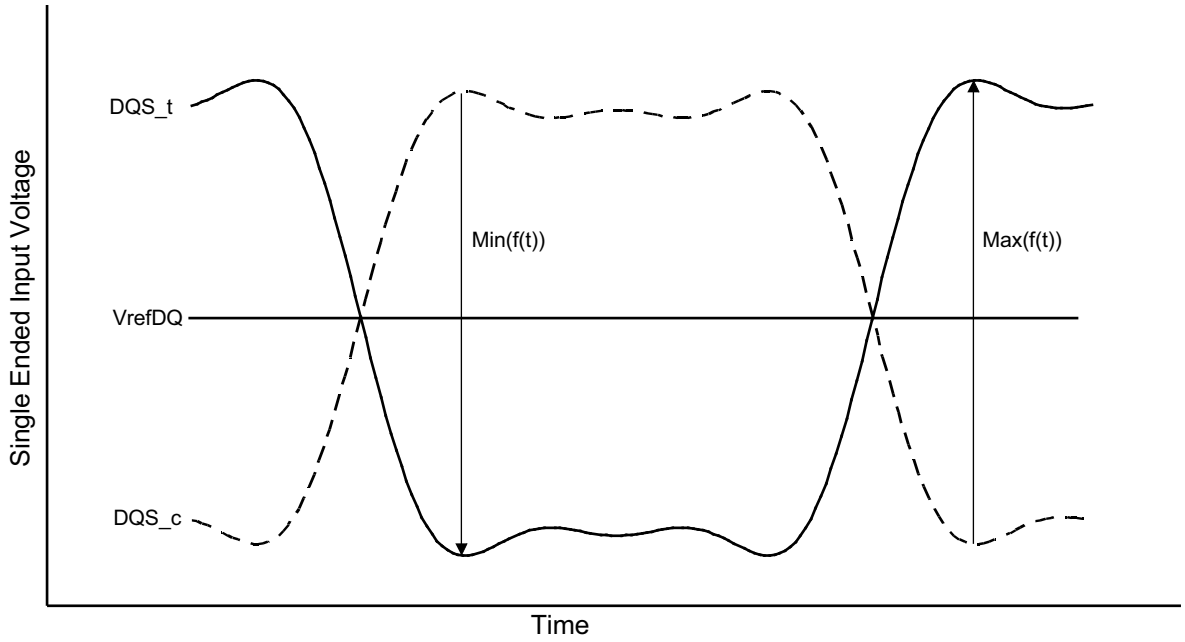
1. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VDQS_t - VDQS_c

a. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1867.

### 5.2.7. Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

**VIH.DIFF.Peak Voltage = Max(f(t))**
**VIL.DIFF.Peak Voltage = Min(f(t))**
**f(t) = VDQS_t - VDQS_c**

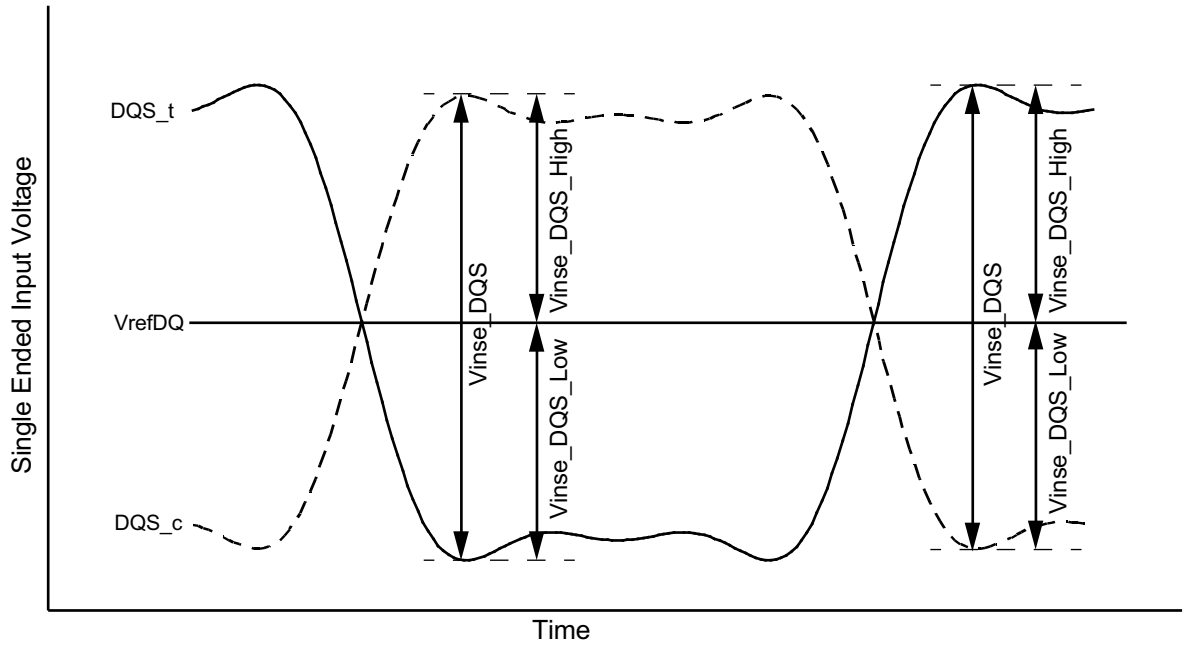



NOTES : 1. VrefDQ is LPDDR4 SDRAM internal setting value by Vref Training.

**Figure 166 - Definition of differential DQS Peak Voltage**

### 5.2.8. Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both Vinse_DQS, Vinse_DQS_High/Low specification at input receiver.




NOTES : 1. VrefDQ is LPDDR4 SDRAM internal setting value by Vref Training.

**Figure 167 - DQS Single-Ended Input Voltage**

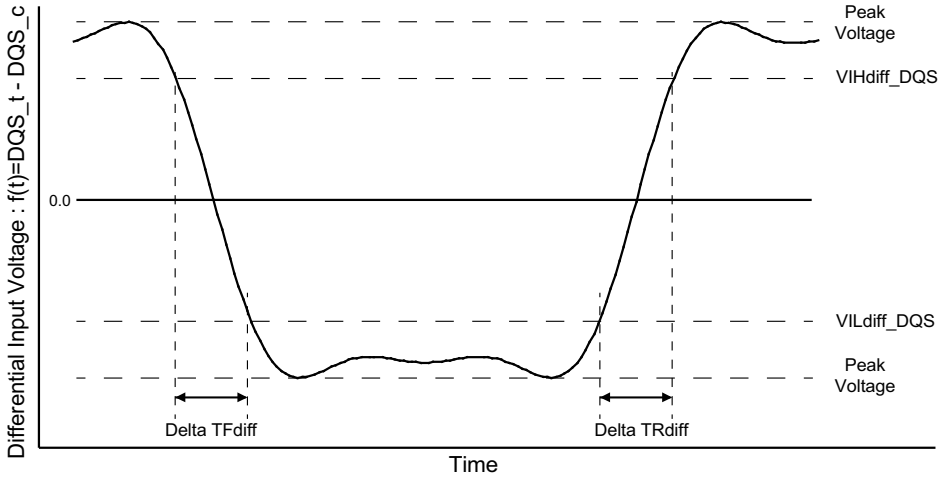
**Table 105 - DQS Single-Ended input voltage**

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS Single-Ended input voltage | Vinse_DQS | 180 | - | 180 | - | 170 | - | mV | 1 |
| DQS Single-Ended input voltage High from $V_{REF}$DQ | Vinse_DQS_High | 90 | - | 90 | - | 85 | - | mV | 1 |
| DQS Single-Ended input voltage Low from $V_{REF}$DQ | Vinse_DQS_Low | 90 | - | 90 | - | 85 | - | mV | 1 |

Notes
1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

### 5.2.9. Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure below and Table below.




NOTES : 1. Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

**Figure 168 - Differential Input Slew Rate Definition for DQS_t, DQS_c**

**Table 106 - Differential Input Slew Rate Definition for DQS_t, DQS_c**

| Description | From | To | Defined by |
|---|---|---|---|
| Differential input slew rate for rising edge(DQS_t - DQS_c) | VILdiff_DQS | VIHdiff_DQS | \|VILdiff_DQS - VIHdiff_DQS\|/DeltaTRdiff |
| Differential input slew rate for falling edge(DQS_t - DQS_c) | VIHdiff_DQS | VILdiff_DQS | \|VILdiff_DQS - VIHdiff_DQS\|/DeltaTFdiff |

**Table 107 - Differential Input Level for DQS_t, DQS_c**

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input High | VIHdiff_DQS | 140 | - | 140 | - | 120 | - | mV | 1 |
| Differential Input Low | VILdiff_DQS | - | -140 | - | -140 | - | -120 | mV | 1 |

Notes
1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

**Table 108 - Differential Input Slew Rate for DQS_t, DQS_c**

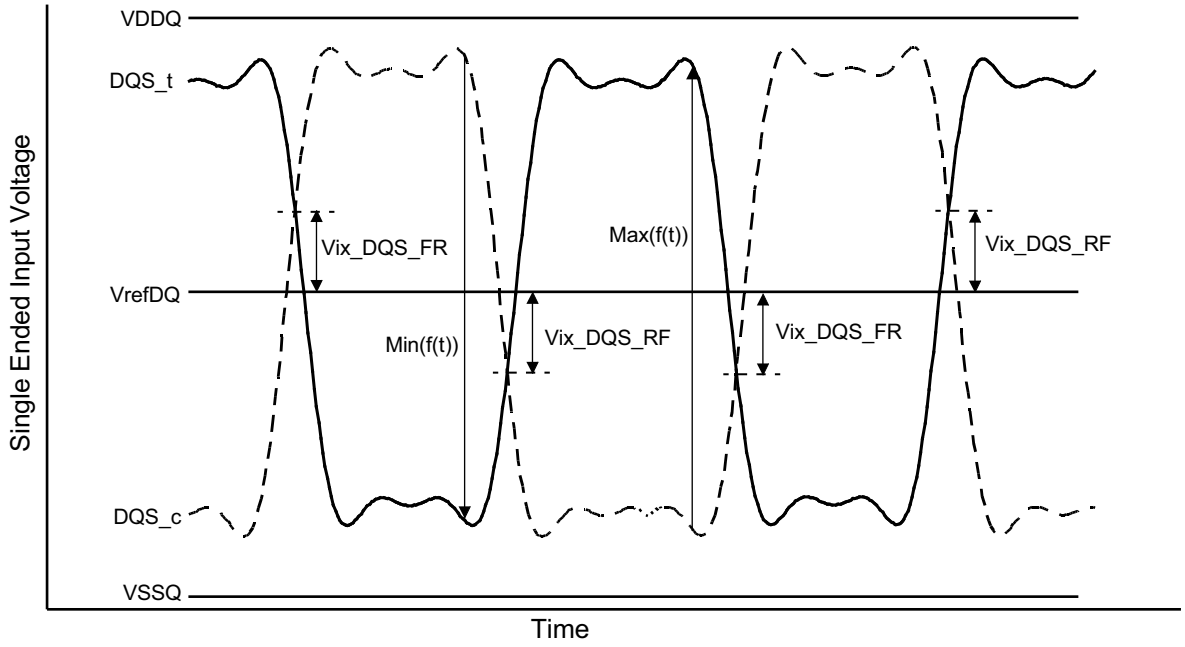
| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input Slew Rate | SRIdiff | 2 | 14 | 2 | 14 | 2 | 14 | V/ns | 1 |

Notes

1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.

### 5.2.10. Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is $V_{REF}DQ$.




NOTES : 1. The base level of Vix_DQS_FR/RF is VrefDQ that is LPDDR4 SDRAM internal setting value by Vref Training.

**Figure 169 - Vix Definition (DQS)**

**Table 109 - Cross point voltage for differential input signals (DQS)**

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | 1600/1867[a] | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS Differential input cross point voltage ratio | Vix_DQS_ratio | - | 20 | - | 20 | - | 20 | % | 1,2,3 |

Notes
1. The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1867.
1. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
2. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))

## 5.3. Input Level for ODT(ca) input

**Table 110 - LPDDR4 Input level for ODT(ca)**

| Symbol | | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| ODT Input high level | VIHODT | 0.75*VDD2 | VDD2+0.2 | V | |
| ODT Input low level | VILODT | -0.2 | 0.25*VDD2 | V | |

## 5.4. Single Ended Output Slew Rate

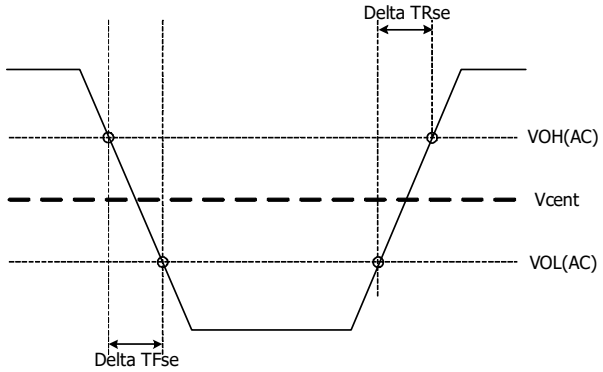



**Figure 170 - Single Ended Output Slew Rate Definition**

**Table 111 - Output Slew Rate (Single-ended)**

| Parameter | Symbol | Value | | Units |
|---|---|---|---|---|
| | | Min (Note 1) | Max (Note 2) | |
| Single-ended Output Slew Rate (VOH = VDDQ*0.5) | SRQse | 3.0 | 9.0 | V/ns |
| Output slew-rate matching ratio (Rise to Fall) | | 0.8 | 1.2 | - |
| SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals | | | | |

Notes
1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

## 5.5. Differential Output Slew Rate

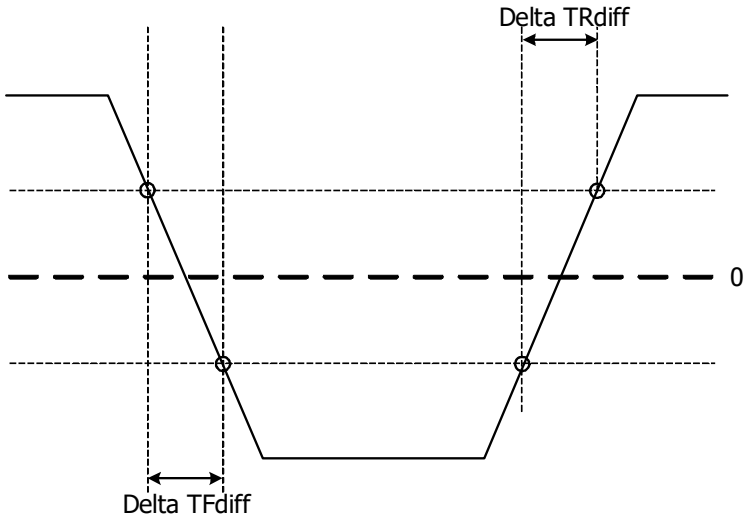



**Figure 171 - Differential Output Slew Rate Definition**

**Table 112 - Differential Output Slew Rate**

| Parameter | Symbol | Value | | Units |
|---|---|---|---|---|
| | | Min (Note 1) | Max (Note 2) | |
| Differential Output Slew Rate (VOH = VDDQ*0.5) | SRQdiff | 6 | 18 | V/ns |
| SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals | | | | |

Notes
1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC)= -0.8*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
3. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

## 5.6. Overshoot and Undershoot Specification for LVSTL

The levels are provided in Table below and Figure below.

**Table 113 - AC Overshoot / Undershoot Specification**

| Parameter | Value | Units |
|---|---|---|
| Maximum peak amplitude allowed for overshoot area | 0.3 | V |
| Maximum peak amplitude allowed for undershoot area | 0.3 | V |
| Maximum overshoot area above VDD/VDDQ | 0.1 | V-ns |
| Maximum undershoot area below VSS/VSSQ | 0.1 | V-ns |

Notes
1. VDD stands for VDD2 for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.
2. VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

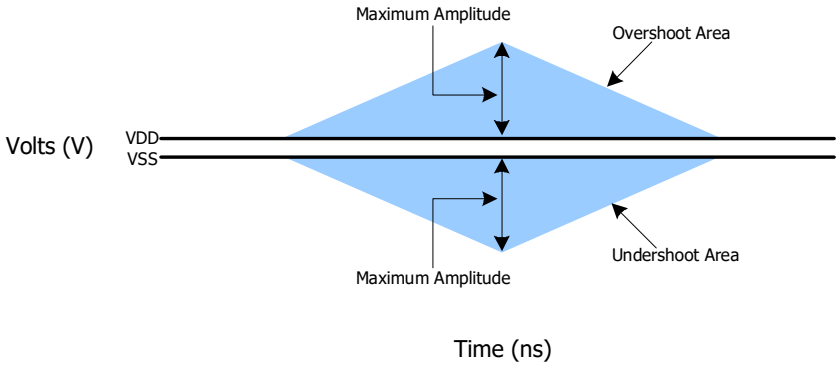
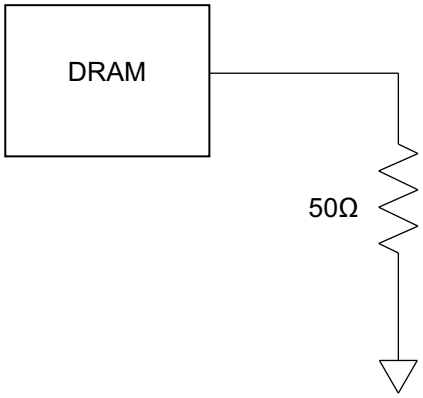



**Figure 172 - AC Overshoot and Undershoot Definition**

## 5.7. LVSTL Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.




Note
1. All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

**Figure 173 - Driver Output Reference Load for Timing and Slew Rate**

## 5.8. LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in figure below.

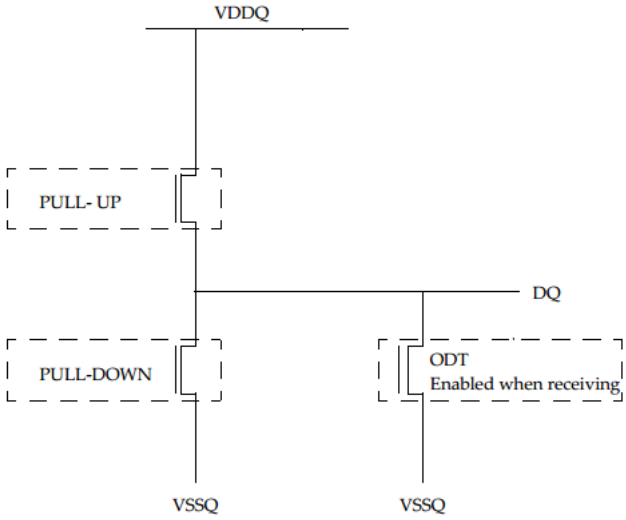



**Figure 174 - LVSTL I/O Cell**

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrated as below procedure.

1. First calibrate the pull-down device against a 240 Ω resister to $V_{DDQ}$ via the ZQ pin.

- Set Strength Control to minimum setting.
- Increase drive strength until comparator detects data bit is less than $V_{DDQ}/2$.
- NMOS pull-down device is calibrated to 240 Ω.

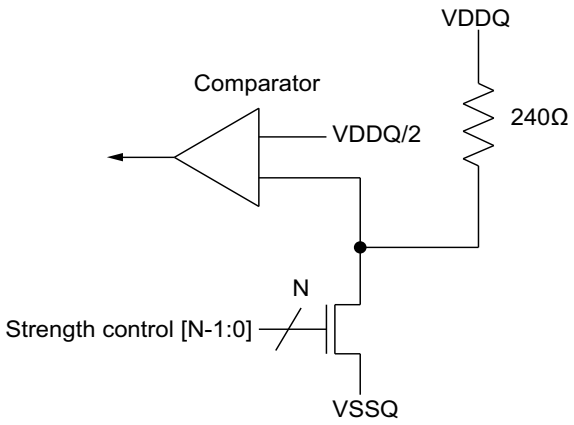



**Figure 175 - Pull-down calibration**

2. Then calibrate the pull-up device against the calibrated pull-down device.
   - Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
   - Set Strength Control to minimum setting.
   - Increase drive strength until comparator detects data bit is greater than VOH target.
   - NMOS pull-up device is now calibrated to VOH target.

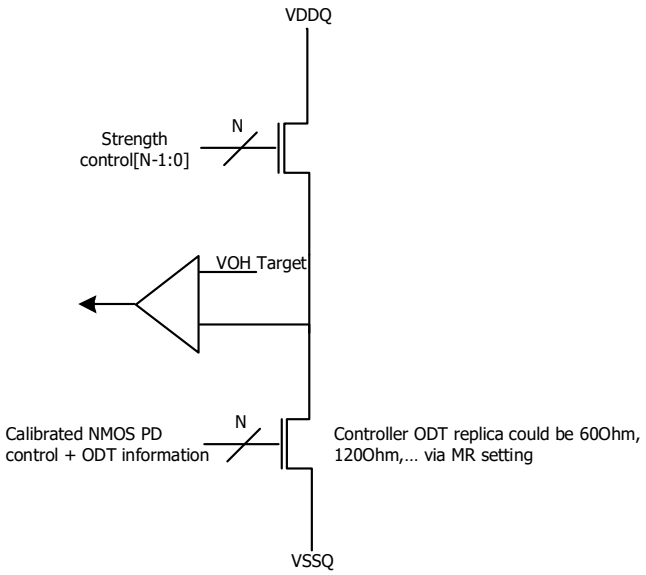



**Figure 176 - Pull-up calibration**

# 6. Input/Output Capacitance

**Table 114 - Input/Output Capacitance**

| Parameter | Symbol | Min/Max | 4266-533 | Unit | Note |
|---|---|---|---|---|---|
| Input capacitance, CK_t and CK_c | CCK | Min | 0.5 | pF | 1,2 |
| | | Max | 0.9 | | |
| Input capacitance delta, CK_t and CK_c | CDCK | Min | 0.0 | pF | 1,2,3 |
| | | Max | 0.09 | | |
| Input capacitance, all other input-only pins | CI | Min | 0.5 | pF | 1,2,4 |
| | | Max | 0.9 | | |
| Input capacitance delta, all other input-only pins | CDI | Min | -0.1 | pF | 1,2,5 |
| | | Max | 0.1 | | |
| Input/output capacitance, DQ, DMI, DQS_t, DQS_c | CIO | Min | 0.7 | pF | 1,2,6 |
| | | Max | 1.3 | | |
| Input/output capacitance delta, DQS_t and DQS_c | CDDQS | Min | 0.0 | pF | 1,2,7 |
| | | Max | 0.1 | | |
| Input/output capacitance delta, DQ and DM | CDIO | Min | -0.1 | pF | 1,2,8 |
| | | Max | 0.1 | | |
| Input/Output Capacitance ZQ | CZQ | Min | 0.0 | pF | 1,2 |
| | | Max | 5.0 | | |

Notes

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK_t . CCK_c.
4. CI applieds to CS_n, CKE, CA0~CA5.
5. CDI = CI . 0.5 * (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO . 0.5 * (CDQS_t + CDQS_c) in byte-lane.

# 7. IDD Specification Parameters and Test Conditions

## 7.1. IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: VIN ≤ VIL(DC) MAX

HIGH: VIN ≥ VIH(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See following tables for switching definition of signals.

**Table 115 - Definition of switching for CA input signals**

| Switching for CA | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| CK_t edge | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 |
| CKE | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| CS | LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

Notes

1. CS must always be driven LOW.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

**Table 116 - CA pattern for IDD4R for BL=16**

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|---|---|---|---|---|---|---|---|---|---|
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | H | H | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

Notes
1. BA[2:0] = 010, C[9:4] = 000000 or 111111, Burst Order C[3:2] = 00 or 11 (Same as LPDDR3 IDD4R Spec)
2. Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

**Table 117 - CA pattern for IDD4W for BL=16**

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|---|---|---|---|---|---|---|---|---|---|
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+5 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+6 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+7 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | L | L | H | H | H | H |
| N+12 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+13 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+14 | HIGH | LOW | Deselect | L | L | L | L | L | L |
| N+15 | HIGH | LOW | Deselect | L | L | L | L | L | L |

Notes
1. BA[2:0] = 010, C[9:4] = 000000 or 111111 (Same as LPDDR3 IDD4W Spec.)
2. Difference from LPDDR3 Spec:
1-No burst ordering
2-CA pins are kept low with DES CMD to reduce ODT current.

**Table 118 - Data Pattern for IDD4W (DBI off) for BL=16**

| | DBI OFF case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Notes

1. Simplified pattern compared with last showing.
2. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table 119 - Data Pattern for IDD4R (DBI off) for BL=16**

| | DBI OFF case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Notes

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table 120 - Data Pattern for IDD4W (DBI on) for BL=16**

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

Notes

1. Green colored cells are DBI enabled burst.

**Table 121 - Data Pattern for IDD4R (DBI on) for BL=16**

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

Notes

1. Green colored cells are DBI enabled burst.

**Table 122 - CA pattern for IDD4R for BL=32**

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|---|---|---|---|---|---|---|---|---|---|
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+9 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+10 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+11 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+16 | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+17 | HIGH | LOW | | L | H | L | L | H | L |
| N+18 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+19 | HIGH | LOW | | H | H | L | H | H | H |
| N+20 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+21 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+22 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+23 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+24 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+25 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+26 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+27 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+28 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+29 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+30 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+31 | HIGH | LOW | DES | L | L | L | L | L | L |
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |

Notes
1. BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst Order C[4:2] = 000 or 111

**Table 123 - CA pattern for IDD4W for BL=32**

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|---|---|---|---|---|---|---|---|---|---|
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+9 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+10 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+11 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+16 | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+17 | HIGH | LOW | | L | H | L | L | H | L |
| N+18 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+19 | HIGH | LOW | | L | L | L | H | H | H |
| N+20 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+21 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+22 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+23 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+24 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+25 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+26 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+27 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+28 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+29 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+30 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+31 | HIGH | LOW | DES | L | L | L | L | L | L |
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |

Notes
1. BA[2:0] = 010, C[9:5] = 00000 or 11111

**Table 124 - Data Pattern for IDD4W (DBI off) for BL=32**

| | DBI OFF case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| | DBI OFF case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL40 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL48 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL53 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL54 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL55 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL61 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL63 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | | |

Notes

1. Simplified pattern compared with last showing. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table 125 - Data Pattern for IDD4R (DBI off) for BL=32**

| | DBI OFF case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL32 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| DBI OFF case | | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL40 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL48 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL53 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL55 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL61 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL62 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL63 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 32 | 32 | 32 | 32 | 32 | 32 | 32 | 32 | | |

Notes

1. Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

**Table 126 - Data Pattern for IDD4W (DBI on) for BL=32**

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL32 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL40 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL48 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL53 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL55 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL61 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL63 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 32 | 32 | 16 | |

Notes

1. Green colored cells are DBI enabled burst.

**Table 127 - Data Pattern for IDD4R (DBI on) for BL=32**

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL32 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL33 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL35 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL36 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL37 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL38 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL39 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |

| | DBI ON case | | | | | | | | | No. of 1's |
|---|---|---|---|---|---|---|---|---|---|---|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL40 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL41 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL42 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL43 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL44 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL45 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL46 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL47 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL48 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL49 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL50 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL51 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL52 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL53 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL54 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL55 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL56 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL57 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL59 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL60 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL61 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL62 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL63 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 32 | 32 | 16 | |

Notes

1. Green colored cells are DBI enabled burst.

## 7.2. IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range. The values described below is the specification for 2ch based measurement. See the section 9. "IDD Measurement"

**Table 128 - LPDDR4 IDD Specification Parameters and Operating Conditions**

| Parameter/Condition | Symbol | Power Supply | Units | Notes |
|---|---|---|---|---|
| Operating one bank active-precharge current:<br>tCK = tCKmin; tRC = tRCmin;<br>CKE is HIGH;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD0_1$ | VDD1 | mA | |
| | $IDD0_2$ | VDD2 | mA | |
| | $IDD0_Q$ | VDDQ | mA | 3 |
| Idle power-down standby current:<br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD2P_1$ | VDD1 | mA | |
| | $IDD2P_2$ | VDD2 | mA | |
| | $IDD2P_Q$ | VDDQ | mA | 3 |
| Idle power-down standby current with clock stop:<br>CK_t =LOW, CK_c =HIGH;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD2PS_1$ | VDD1 | mA | |
| | $IDD2PS_2$ | VDD2 | mA | |
| | $IDD2PS_Q$ | VDDQ | mA | 3 |
| Idle non power-down standby current:<br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD2N_1$ | VDD1 | mA | |
| | $IDD2N_2$ | VDD2 | mA | |
| | $IDD2N_Q$ | VDDQ | mA | 3 |
| Idle non power-down standby current with clock stopped:<br>CK_t=LOW; CK_c=HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD2NS_1$ | VDD1 | mA | |
| | $IDD2NS_2$ | VDD2 | mA | |
| | $IDD2NS_Q$ | VDDQ | mA | 3 |
| Active power-down standby current:<br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD3P_1$ | VDD1 | mA | |
| | $IDD3P_2$ | VDD2 | mA | |
| | $IDD3P_Q$ | VDDQ | mA | 3 |

| Parameter/Condition | Symbol | Power Supply | Units | Notes |
|---|---|---|---|---|
| Active power-down standby current with clock stop:<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD3PS_1$ | VDD1 | mA | |
| | $IDD3PS_2$ | VDD2 | mA | |
| | $IDD3PS_Q$ | VDDQ | mA | 4 |
| Active non-power-down standby current:<br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD3N_1$ | VDD1 | mA | |
| | $IDD3N_2$ | VDD2 | mA | |
| | $IDD3N_Q$ | VDDQ | mA | 4 |
| Active non-power-down standby current with clock stopped:<br>CK_t=LOW, CK_c=HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD3NS_1$ | VDD1 | mA | |
| | $IDD3NS_2$ | VDD2 | mA | |
| | $IDD3NS_Q$ | VDDQ | mA | 4 |
| Operating burst READ current:<br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; RL = RL(MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $IDD4R_1$ | VDD1 | mA | |
| | $IDD4R_2$ | VDD2 | mA | |
| | $IDD4R_Q$ | VDDQ | mA | 5 |
| Operating burst WRITE current:<br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $IDD4W_1$ | VDD1 | mA | |
| | $IDD4W_2$ | VDD2 | mA | |
| | $IDD4W_Q$ | VDDQ | mA | 4 |
| All-bank REFRESH Burst current:<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5_1$ | VDD1 | mA | |
| | $IDD5_2$ | VDD2 | mA | |
| | $IDD5_Q$ | VDDQ | mA | 4 |
| All-bank REFRESH Average current:<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5AB_1$ | VDD1 | mA | |
| | $IDD5AB_2$ | VDD2 | mA | |
| | $IDD5AB_Q$ | VDDQ | mA | 4 |

| Parameter/Condition | Symbol | Power Supply | Units | Notes |
|---|---|---|---|---|
| Per-bank REFRESH Average current:<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5PB_1$ | VDD1 | mA | |
| | $IDD5PB_2$ | VDD2 | mA | |
| | $IDD5PB_Q$ | VDDQ | mA | 4 |
| Self refresh current (85°C):<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | mA | 4,6,7,8,<br>10 |
| Self refresh current (45°C):<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | mA | 4,6,7,8,<br>10 |
| Self refresh current (25°C):<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | mA | 4,6,7,8,<br>10 |
| Self refresh current (105°C):<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6ET_1$ | VDD1 | mA | 7,8,11 |
| | $IDD6ET_2$ | VDD2 | mA | 7,8,11 |
| | $IDD6ET_Q$ | VDDQ | mA | 4,7,8,11 |

Notes

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
10. IDD6 up to 85°C is guaranteed, and it is typical value of the distribution of the arithmetic mean.
11. IDD6ET is a typical value, is sampled only, and is not tested.

# 8. Electrical Characteristics and AC Timing

## 8.1. Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in mal-function of the LPDDR4 device.

### 8.1.1. Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left( \sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

### 8.1.2. Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
tCK(abs) is not subject to production test.

### 8.1.3. Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left( \sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left( \sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

### 8.1.4. Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

### 8.1.5. Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act is the actual clock jitter for a given system.
tJIT(per),allowed is the specified allowed clock period jitter.
tJIT(per) is not subject to production test.

### 8.1.6. Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCK(i +1) - tCK(i)}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

## 8.2. Clock Timing

**Table 129 - Clock timings**

| Parameter | Symbol | min max | 1600 | 2400 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Average Clock Period | tCK (avg) | min | 1.25 | 0.833 | 0.625 | 0.536 | 0.468 | ns | |
| | | max | 100 | 100 | 100 | 100 | 100 | | |
| Average high pulse width | tCH (avg) | min | 0.46 | 0.46 | 0.46 | 0.46 | 0.46 | tCK (avg) | |
| | | max | 0.54 | 0.54 | 0.54 | 0.54 | 0.54 | | |
| Average low pulse width | tCL (avg) | min | 0.46 | 0.46 | 0.46 | 0.46 | 0.46 | tCK (avg) | |
| | | max | 0.54 | 0.54 | 0.54 | 0.54 | 0.54 | | |
| Absolute Clock Period | tCK (abs) | min | tCK(avg)min + tJIT(per)min | | | | | ns | |
| | | max | - | | | | | | |
| Absolute clock HIGH pulse width | tCH (abs) | min | 0.43 | 0.43 | 0.43 | 0.43 | 0.43 | tCK (avg) | |
| | | max | 0.57 | 0.57 | 0.57 | 0.57 | 0.57 | | |
| Absolute clock LOW pulse width | tCL (abs) | min | 0.43 | 0.43 | 0.43 | 0.43 | 0.43 | tCK (avg) | |
| | | max | 0.57 | 0.57 | 0.57 | 0.57 | 0.57 | | |
| Clock Period Jitter | tJIT (per) | min | -70 | -50 | -40 | -40 | -30 | ps | |
| | | max | 70 | 50 | 40 | 40 | 30 | | |
| Maximum Clock Jitter between two consecutive clock cycles | tJIT (cc) | min | - | | | | | ps | |
| | | max | 140 | 100 | 80 | 80 | 80 | | |

## 8.3. Temperature Derating for AC Timing

**Table 130 - Temperature Derating for AC timing**

| Parameter | Symbol | min max | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DQS output access time from CK_t/CK_c (derated) | tDQSCK | max | 3600 | | | | | | | | ps | |
| RAS-to-CAS delay (derated) | tRCD | min | tRCD + 1.875 | | | | | | | | ns | |
| ACTIVATE-to- ACTIVATE command period (derated) | tRC | min | tRC + 3.75 | | | | | | | | ns | |
| Row active time (derated) | tRAS | min | tRAS + 1.875 | | | | | | | | ns | |
| Row precharge time (derated) | tRP | min | tRP + 1.875 | | | | | | | | ns | |
| Active bank A to active bank B (derated) | tRRD | min | tRRD + 1.875 | | | | | | | | ns | |

Notes

1. Timing derating applies for operation at 85$^{o}$C to 105$^{o}$C

## 8.4. CA Rx voltage and timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

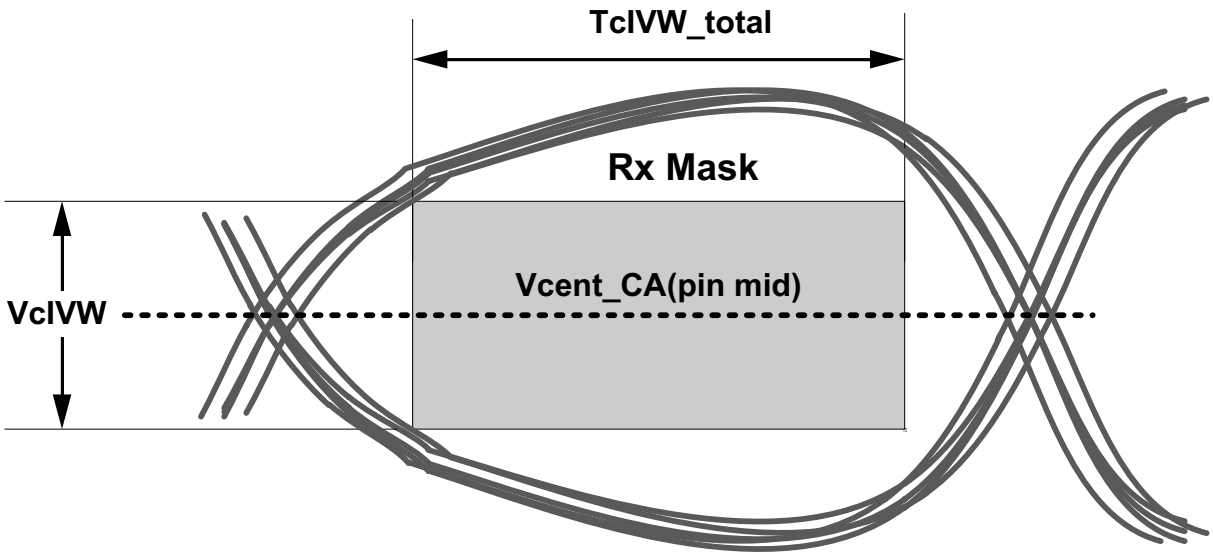



**Figure 177 - CA Receiver(Rx) mask**

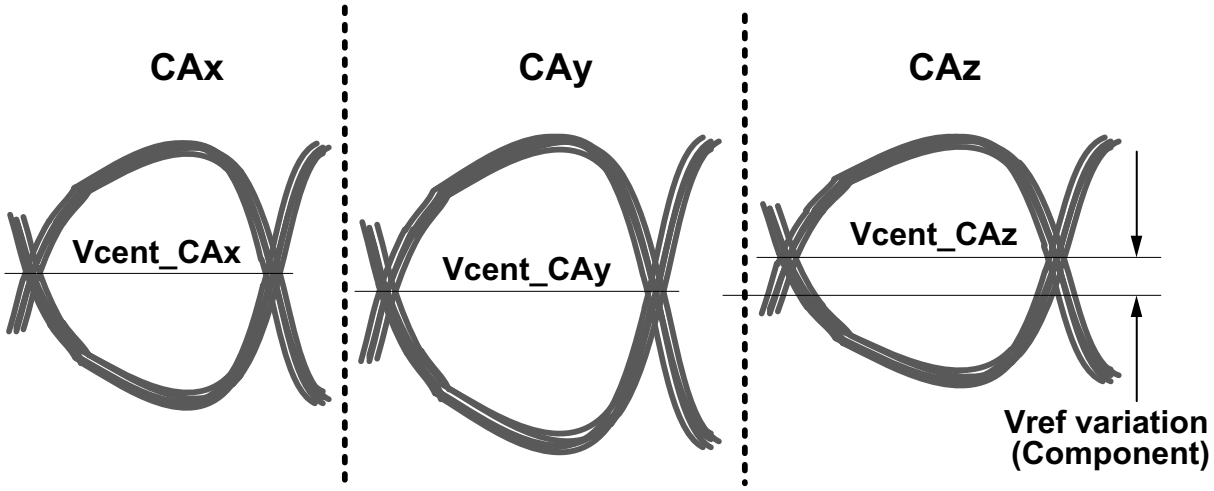



**Figure 178 - Across pin Vref CA voltage variation**

Vcent_CA(pin avg) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA pin Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in the above figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

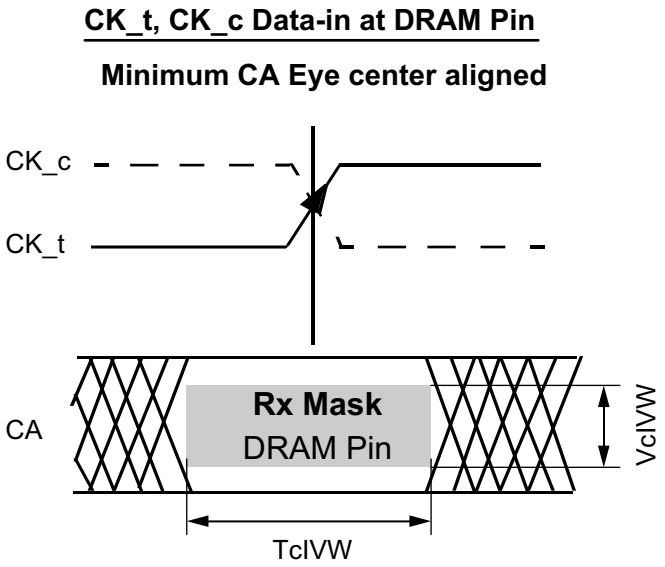
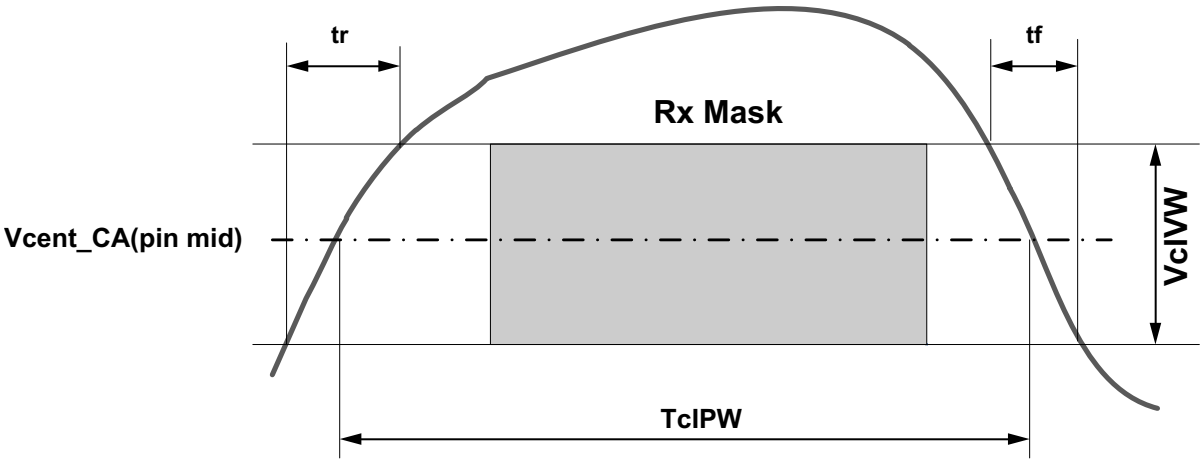



**Figure 179 - CA Timing at the DRAM pins**

All of the timing terms in figure 150 are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).




Note
1. SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

**Figure 180 - CA TcIPW and SRIN_cIVW definition (for each input pulse)**

Notes
1. SRIN_cIVW=VcIVW/(tr or tf), signal must be monotonic within tr and tf range.

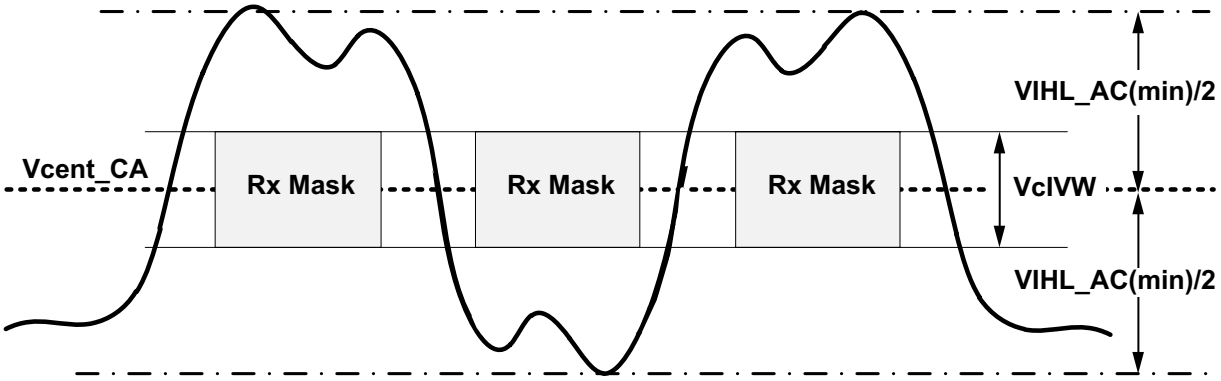



**Figure 181 - CA VIHIL_AC definition (for each input pulse)**

**Table 131 - Command Address Input Parameters**

| Parameter | Symbol | min max | DQ-1333[A)] | DQ-1600/ 1867 | DQ-3200 | DQ-3733 | DQ-4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| Rx Mask voltage - p-p | VcIVW | max | 175 | 175 | 155 | 155 | 145 | mV | 1,2,3 |
| Rx timing window | TcIVW | max | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | UI | 1,2,3 |
| CA AC input pulse amplitude pk-pk | VIHL_AC | min | 210 | 210 | 190 | 190 | 180 | mV | 4,7 |
| CA input pulse width | TcIPW | min | 0.55 | 0.55 | 0.6 | 0.6 | 0.6 | UI | 5 |
| Input Slew Rate over VcIVW | SRIN_cIVW | min | 1 | 1 | 1 | 1 | 1 | V/ns | 6 |
| | | max | 7 | 7 | 7 | 7 | 7 | | |
| A. The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies. | | | | | | | | | |

Notes
1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VcIVW total(max) must be centered around Vcent_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

## 8.5. DRAM Data Timing

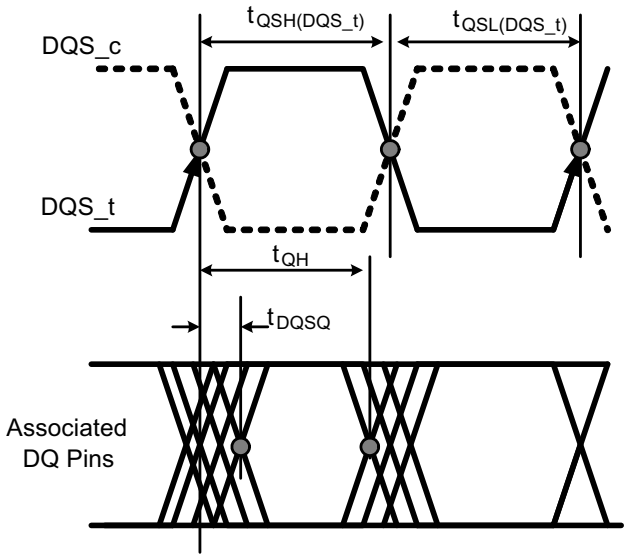



**Figure 182 - Read data timing definitions tQH and tDQSQ across on DQ signals per DQS group**

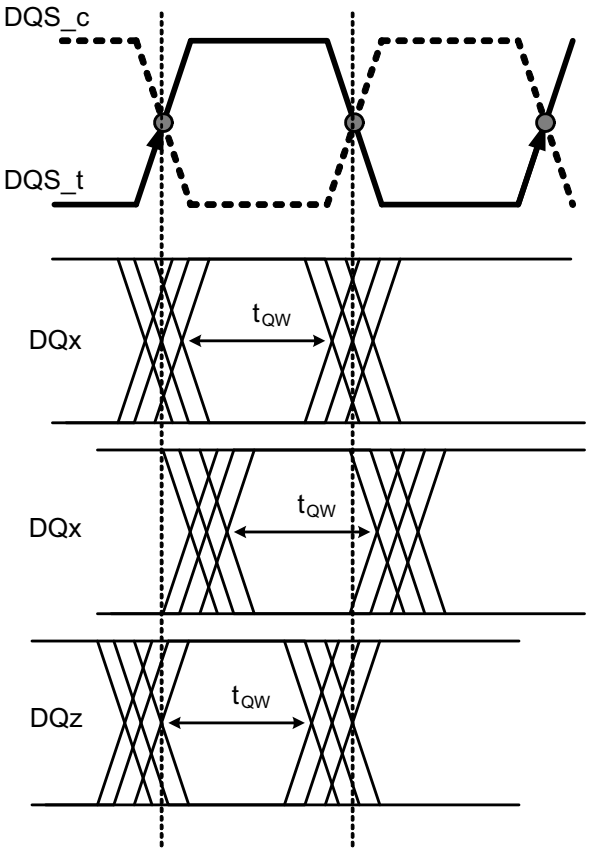



**Figure 183 - Read data timing tQW valid window defined per DQ signal**

**Table 132 - Read Output timings**

| Parameter | Symbol | min max | 1600/ 1867 | 2133/ 2400 | 3200 | 3733 | 4266 | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| **Data Timing** | | | | | | | | | |
| DQS_t,DQS_c to DQ Skew total, per group, per access (DBIDisabled) | tDQSQ | max | 0.18 | | | | | UI | |
| DQ output hold time total from DQS_t, DQS_c (DBI-Disabled) | tQH | min | min(tQSH, tQSL) | | | | | UI | |
| DQ output window time total, per pin (DBI-Disabled) | tQW_total | min | 0.75 | 0.73 | 0.7 | 0.7 | 0.7 | UI | 3 |
| DQ output window time deterministic, per pin (DBIDisabled) | tQW_dj | min | tbd | tbd | tbd | tbd | tbd | UI | 2,3 |
| DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled) | tDQSQ_DBI | max | 0.18 | | | | | UI | |
| DQ output hold time total from DQS_t, DQS_c (DBI-Enabled) | tQH_DBI | min | min(tQSH_DBI, tQSL_DBI) | | | | | UI | |
| DQ output window time total, per pin (DBI-enabled) | tQW_total_DBI | min | 0.75 | 0.73 | 0.7 | 0.7 | 0.7 | UI | 3 |
| **Data Strobe Timing** | | | | | | | | | |
| DQS, DQS# differential output low time (DBI-Disabled) | tQSL | min | tCL(abs)-0.05 | | | | | tCK (avg) | 4,5 |
| DQS, DQS# differential output high time (DBI-Disabled) | tQSH | min | tCH(abs)-0.05 | | | | | tCK (avg) | 4,6 |
| DQS, DQS# differential output low time (DBI-Enabled) | tQSL_DBI | min | tCL(abs)-0.045 | | | | | tCK (avg) | 5,7 |
| DQS, DQS# differential output high time (DBI-Enabled) | tQSH_DBI | min | tCH(abs)-0.045 | | | | | tCK (avg) | 6,7 |

Notes

1. Unit UI = tCK(avg)min/2
2. The deterministic component of the total timing. Measurement method tbd.
3. This parameter will be characterized and guaranteed by design.
4. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
5. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge
7. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
8. The Tx voltage and absolute timing requirements at 1600Mbps apply for all DQ operating frequencies for speed bins which is less than 1600Mbps.

## 8.6. DQ Rx Voltage and Timing Definition

The DQ input receiver mask for voltage and timing is shown in figure below, is applied per pin. The "total" mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than TBD. The mask is a receiver property and it is not the valid data-eye.

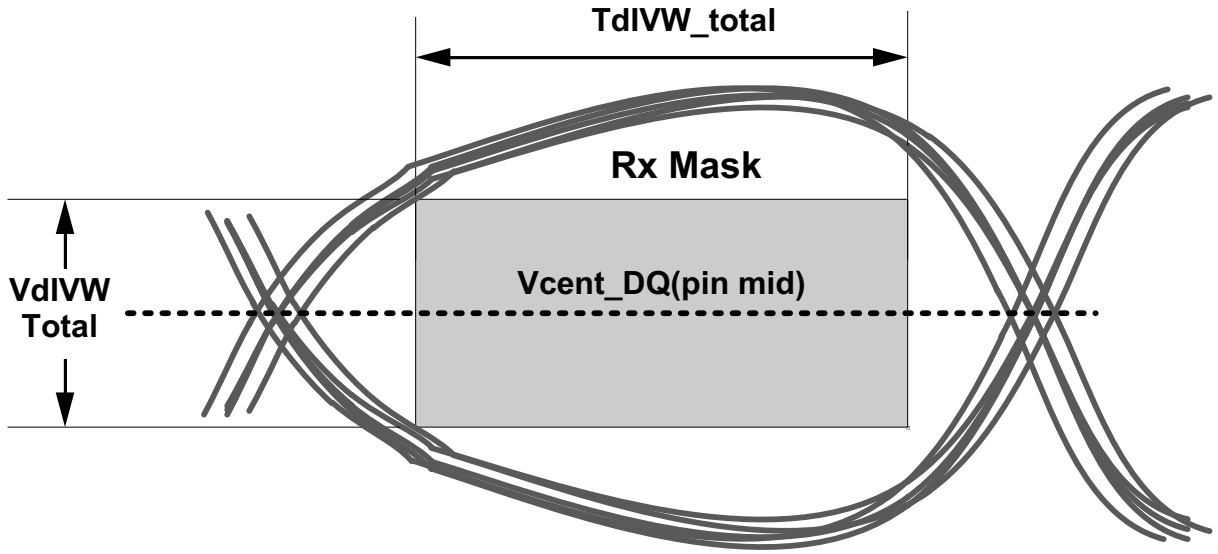



**Figure 184 - DQ Receiver(Rx) mask**

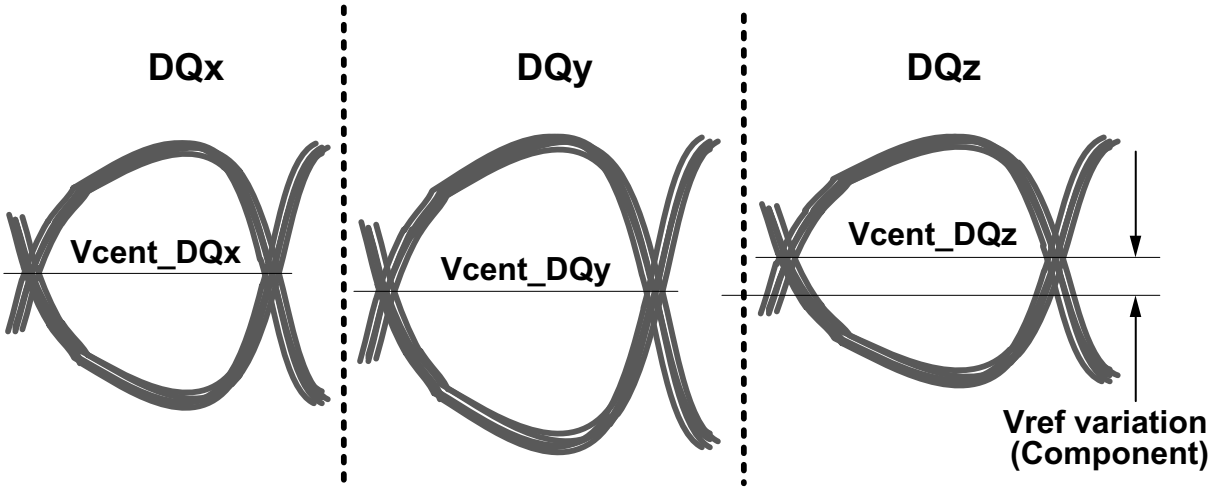
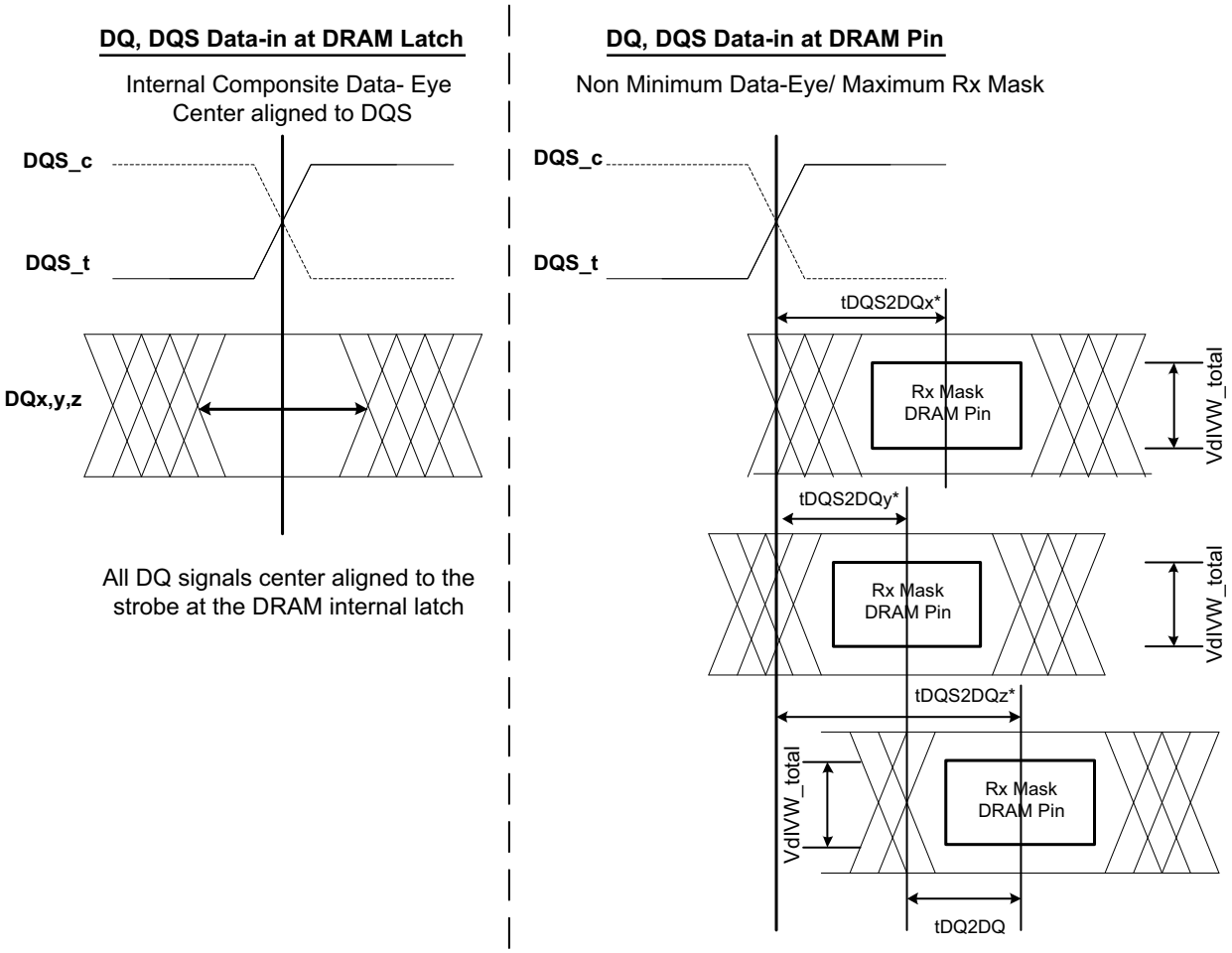



**Figure 185 - Across pin Vref DQ voltage variation**

Vcent_DQ(pin_mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Above Figure. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

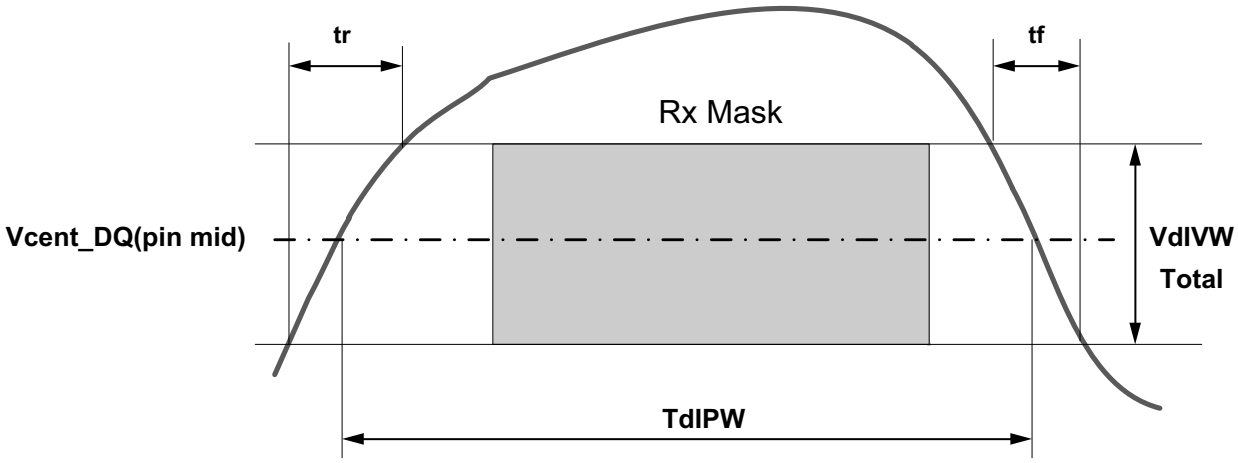



**NOTE:**

1. tDQS2DQ is measured at the center(midpoint) of the TdiVW window.
2. DQz represents the max tDQS2DQ in this example
3. DQy represents the min tDQS2DQ in this example

**Figure 186 - DQ to DQS (tDQS2DQ and tDQDQ) Timings at the DRAM pins referenced from the internal latch**

**Figure 187 - DQ TdIPW and SRIN_dIVW definition (for each input pulse)**




Note
1. SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

**Figure 188 - DQ VIHL_AC definition (for each input pulse)**

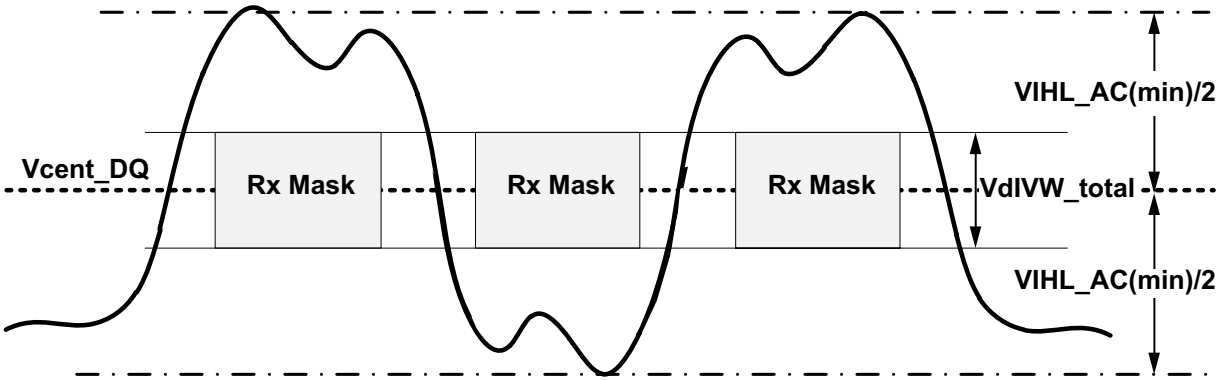


**Table 133 - DRAM DQs in Receive Mode**

| Parameter | Symbol | min max | 1600/ 1867 | 2133/ 2400 | 3200 | 3733 | 4266 | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Rx Mask voltage - p-p total | VdiVW_Total | max | 140 | 140 | 140 | 140 | 120 | mV | 1,2,3, 4,5 |
| Rx timing window total (At VdIVW voltage levels) | TdIVW_total | max | 0.22 | 0.22 | 0.25 | 0.25 | 0.25 | UI | 1,2,3, 5,18 |
| Rx timing window 1 bit toggle (At VdIVW voltage levels) | TdIVW_1bit | max | TBD | TBD | TBD | TBD | TBD | UI | 1,2,3, 5,13,1 8 |
| DQ AC input pulse amplitude pk-pk | VIHL_AC | min | 180 | 180 | 180 | 180 | 170 | mV | 1,6,14 |
| Input pulse width (At Vcent_DQ) | TdIPW DQ | min | 0.45 | 0.45 | 0.45 | 0.45 | 0.45 | UI | 1,7,18 |
| DQ to DQS offset | tDQS2DQ | min | 200 | 200 | 200 | 200 | 200 | ps | 1,8 |
| | | max | 800 | 800 | 800 | 800 | 800 | | |
| DQ to DQ offset | tDQ2DQ | max | 30 | 30 | 30 | 30 | 30 | ps | 1,9 |
| DQ to DQS offset temperature variation | tDQS2DQ_temp | max | 0.6 | 0.6 | 0.6 | 0.6 | 0.6 | ps/°C | 1,10 |
| DQ to DQS offset voltage variation | tDQS2DQ_volt | max | 33 | 33 | 33 | 33 | 33 | ps/50mV | 1,11 |
| Input Slew Rate over VdIVW_total | SRIN_dIVW | min | 1 | 1 | 1 | 1 | 1 | V/ns | 1,12 |
| | | max | 7 | 7 | 7 | 7 | 7 | | |
| DQ to DQS offset rank to rank variation | tDQS2DQ_rank2rank | max | 200 | 200 | 200 | 200 | 200 | ps | 1,15,1 6,17 |

Notes

1. The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW_total(ps) = 137.5ps at or below 1600 operating frequencies.
2. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
3. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
4. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
5. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
6. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
7. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
8. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
9. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
10. TDQS2DQ max delay variation as a function of temperature.
11. TDQS2DQ max delay variation as a function of the DC voltage variation for $V_{DDQ}$ and $V_{DD2}$. It includes the $V_{DDQ}$ and $V_{DD2}$ AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement $V_{DDQ}$ = $V_{DD2}$ is assumed.
12. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
13. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
14. VIHL_AC does not have to be met when no transitions are occurring.
15. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
16. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
17. tDQS2DQ_rabk2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.
18. Unit UI = tCK(avg)min/2

# 9. IDD Measurement

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range. The values described below is the specification for 2ch based measurement.

**Table - LPDDR4 IDD Specification Parameters and Operating Conditions**

| Parameter/Condition | Symbol | Power Supply | 4266 (x16) | Units | Notes |
|---|---|---|---|---|---|
| **Operating one bank active-precharge current:**<br>tCK = tCKmin; tRC = tRCmin;<br>CKE is HIGH;<br>CS is LOW between valid commands;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD0_1$ | VDD1 | 7.00 | mA | |
| | $IDD0_2$ | VDD2 | 80.00 | mA | |
| | $IDD0_Q$ | VDDQ | 2.50 | mA | 3 |
| **Idle power-down standby current:**<br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD2P_1$ | VDD1 | 1.80 | mA | |
| | $IDD2P_2$ | VDD2 | 6.90 | mA | |
| | $IDD2P_Q$ | VDDQ | 0.80 | mA | 3 |
| **Idle power-down standby current with clock stop:**<br>CK_t =LOW, CK_c =HIGH;<br>CKE is LOW;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD2PS_1$ | VDD1 | 1.80 | mA | |
| | $IDD2PS_2$ | VDD2 | 6.90 | mA | |
| | $IDD2PS_Q$ | VDDQ | 0.80 | mA | 3 |
| **Idle non power-down standby current:**<br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD2N_1$ | VDD1 | 1.80 | mA | |
| | $IDD2N_2$ | VDD2 | 37.30 | mA | |
| | $IDD2N_Q$ | VDDQ | 2.50 | mA | 3 |
| **Idle non power-down standby current with clock stopped:**<br>CK_t=LOW; CK_c=HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>All banks are idle;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD2NS_1$ | VDD1 | 1.80 | mA | |
| | $IDD2NS_2$ | VDD2 | 31. | mA | |
| | $IDD2NS_Q$ | VDDQ | 2.50 | mA | 3 |
| **Active power-down standby current:**<br>tCK = tCKmin;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD3P_1$ | VDD1 | 3.00 | mA | |
| | $IDD3P_2$ | VDD2 | 9.89 | mA | |
| | $IDD3P_Q$ | VDDQ | 0.80 | mA | 3 |

| Parameter/Condition | Symbol | Power Supply | 4266 (x16) | Units | Notes |
|---|---|---|---|---|---|
| **Active power-down standby current with clock stop:**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD3PS_1$ | VDD1 | 3.00 | mA | |
| | $IDD3PS_2$ | VDD2 | 9.88 | mA | |
| | $IDD3PS_Q$ | VDDQ | 0.80 | mA | 4 |
| **Active non-power-down standby current:**<br>tCK = tCKmin;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are switching;<br>Data bus inputs are stable<br>ODT disabled | $IDD3N_1$ | VDD1 | 3.00 | mA | |
| | $IDD3N_2$ | VDD2 | 50.00 | mA | |
| | $IDD3N_Q$ | VDDQ | 2.50 | mA | 4 |
| **Active non-power-down standby current with clock stopped:**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is HIGH;<br>CS is LOW;<br>One bank is active;<br>CA bus inputs are stable;<br>Data bus inputs are stable<br>ODT disabled | $IDD3NS_1$ | VDD1 | 3.00 | mA | |
| | $IDD3NS_2$ | VDD2 | 45.00 | mA | |
| | $IDD3NS_Q$ | VDDQ | 2.50 | mA | 4 |
| **Operating burst READ current:**<br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; RL = RL(MIN);<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $IDD4R_1$ | VDD1 | 19.61 | mA | |
| | $IDD4R_2$ | VDD2 | 481.65 | mA | |
| | $IDD4R_Q$ | VDDQ | 183.54 | mA | 5 |
| **Operating burst WRITE current:**<br>tCK = tCKmin;<br>CS is LOW between valid commands;<br>One bank is active;<br>BL = 16 or 32; WL = WLmin;<br>CA bus inputs are switching;<br>50% data change each burst transfer<br>ODT disabled | $IDD4W_1$ | VDD1 | 19.59 | mA | |
| | $IDD4W_2$ | VDD2 | 423.02 | mA | |
| | $IDD4W_Q$ | VDDQ | 2.50 | mA | 4 |
| **All-bank REFRESH Burst current:**<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tRFCabmin;<br>Burst refresh;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5_1$ | VDD1 | 26.40 | mA | |
| | $IDD5_2$ | VDD2 | 191.81 | mA | |
| | $IDD5_Q$ | VDDQ | 2.50 | mA | 4 |
| **All-bank REFRESH Average current:**<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5AB_1$ | VDD1 | 4.00 | mA | |
| | $IDD5AB_2$ | VDD2 | 49.00 | mA | |
| | $IDD5AB_Q$ | VDDQ | 2.50 | mA | 4 |

| Parameter/Condition | Symbol | Power Supply | 4266 (x16) | Units | Notes |
|---|---|---|---|---|---|
| **Per-bank REFRESH Average current:**<br>tCK = tCKmin;<br>CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are switching;<br>Data bus inputs are stable;<br>ODT disabled | $IDD5PB_1$ | VDD1 | 4.00 | mA | |
| | $IDD5PB_2$ | VDD2 | 49.00 | mA | |
| | $IDD5PB_Q$ | VDDQ | 2.50 | mA | 4 |
| **Self refresh current (85°C):**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | 6.00 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | 20.00 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | 0.80 | mA | 4,6,7,8, 10 |
| **Self refresh current (45°C):**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | 0.39 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | 1.50 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | 0.10 | mA | 4,6,7,8, 10 |
| **Self refresh current (25°C):**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6_1$ | VDD1 | 0.33 | mA | 6,7,8,10 |
| | $IDD6_2$ | VDD2 | 0.82 | mA | 6,7,8,10 |
| | $IDD6_Q$ | VDDQ | 0.10 | mA | 4,6,7,8, 10 |
| **Self refresh current (105°C):**<br>CK_t=LOW, CK_c=HIGH;<br>CKE is LOW;<br>CA bus inputs are stable;<br>Data bus inputs are stable;<br>Maximum 1x Self-Refresh Rate;<br>ODT disabled | $IDD6ET_1$ | VDD1 | 6.05 | mA | 7,8,11 |
| | $IDD6ET_2$ | VDD2 | 45.11 | mA | 7,8,11 |
| | $IDD6ET_Q$ | VDDQ | 0.10 | mA | 4,7,8,11 |

Notes

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 ohm.
6. The 1x Self-Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. Supplier datasheets may contain additional Self Refresh IDD values for temperature subranges within the Standard or elevated Temperature Ranges.
9. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
10. IDD6 up to 85°C is guaranteed, and it is typical value of the distribution of the arithmetic mean.
11. IDD6ET is a typical value, is sampled only, and is not tested.