2znm 8Gb HBM2 (Gen 2)

H5VR64ESA8H-N0C
H5VR32ESA4H-N0C
H5VR64ESA8H-N2C
H5VR32ESA4H-N2C

Revision History

Revision	History	Date	Remark
0.1	- Initial Version	Aug. 2017	
0.11	- Updated P/N	Sep. 2017	
1.0	- Updated AC timings - Updated CATTRIP in Figure 3. Power-up and Initialization - Updated IDD Specification	Feb. 2018	
1.1	- Updated IDD Specification	Mar. 2018	
1.11	- Device ID Wrapper Data Register	Apr. 2018	
1.2	- Updated Mode Register 4 (MR4) - Updated DQ Parity	Jul. 2018	
1.3	- Updated CATTEMP Value	Aug. 2018	
1.4	- Updated Operating Temperature	Nov. 2018	
1.5	- Updated AC timings	Jan. 2019	
1.51	- Updated POD description	Jan. 2019	
1.6	- Updated Table Absolute Maximum DC Rating	Feb. 2019	
1.7	- Updated Table Operating Temperature - Updated Table Temperature Compensated Refresh Trip Points	Apr. 2019	
1.71	- Corrected Typo	May. 2019	
1.8	- Corrected Typo	Sep. 2020	

1. Functional Description

The HBM DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM DRAM uses a wide-interface architecture to achieve high-speed, low power operation. The HBM DRAM uses differential clock CK_t/CK_c. Commands are registered at the rising edge of CK_t, CK_c. Each channel interface maintains a 128b data bus operating at DDR data rates.

2. Device Features and Ordering Information

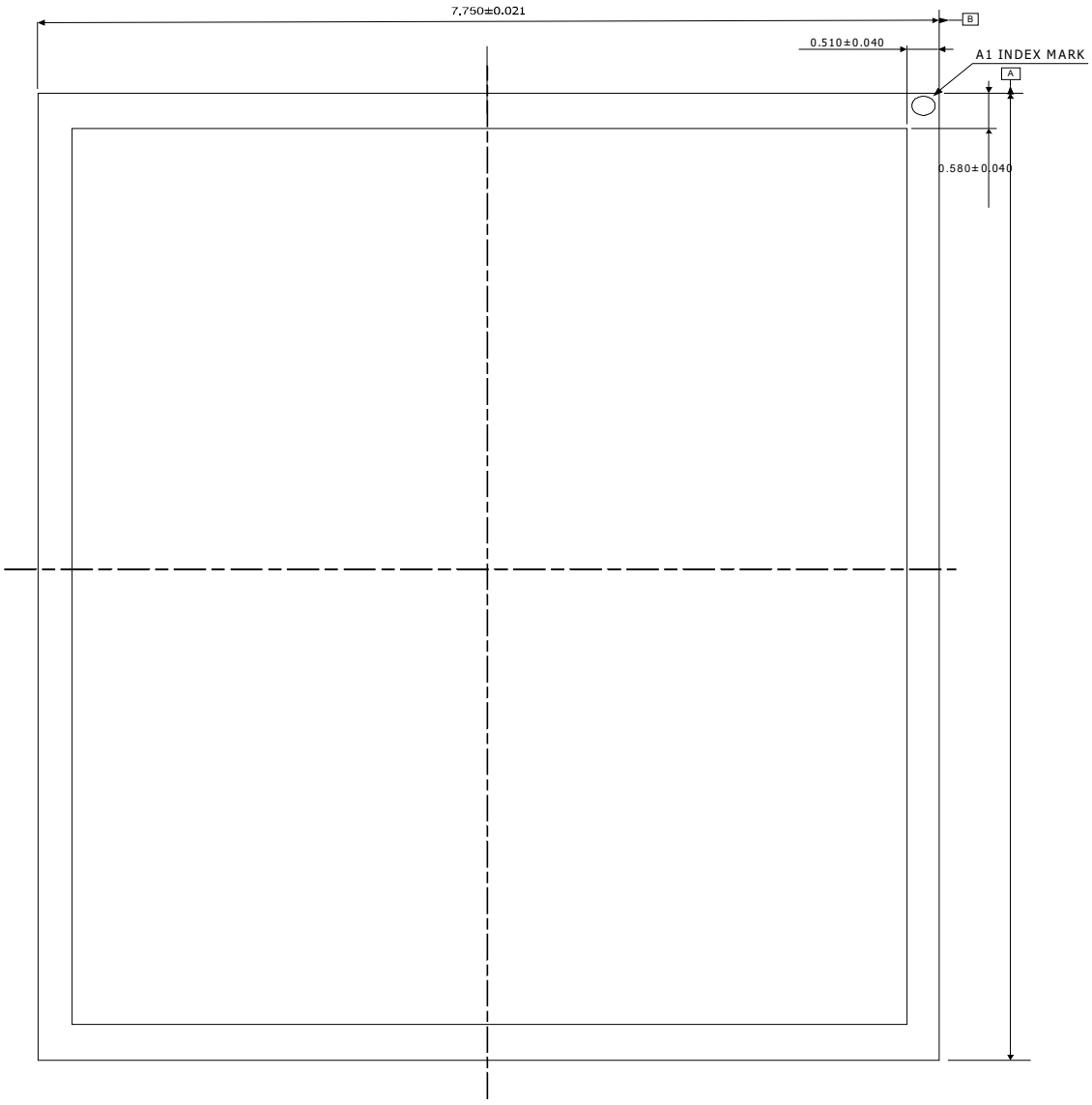
2.1. FEATURES

- 2n prefetch architecture with 256 bits per memory read and write access
- BL = 4
- 128 DQ width + Optional ECC pin support/channel
- Pseudo Channel Mode Operation;
  (64 DQ width for Pseudo Channel Mode)
- Differential clock inputs (CK_t/CK_c)
- DDR commands entered on each positive CK_t, CK_c edge. Row Activate commands require two cycles. All other commands are one cycle command.
- Semi-independent Row & Column Command Interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes.
- Data referenced to strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. 1 strobe pair per DWORD
- Up to 8 channels/stack (16 pseudo channel)
- 32 banks per channel; (16 banks per pseudo channel)
- Bank Grouping supported
- 1KB page size per Pseudo channel;
- DBIac support configurable via MRS
- Data mask for masking WRITE data per byte
- Self Refresh Modes
- IO voltage 1.2 V
- DRAM core voltage 1.2 V, independent of IO voltage
- 4Gb Channel density of 2Gb/4Gb/8Gb depend on number of stack
- Unterminated data/address/cmd/clk interfaces
- Temperature sensor with 3-bit encoded range output

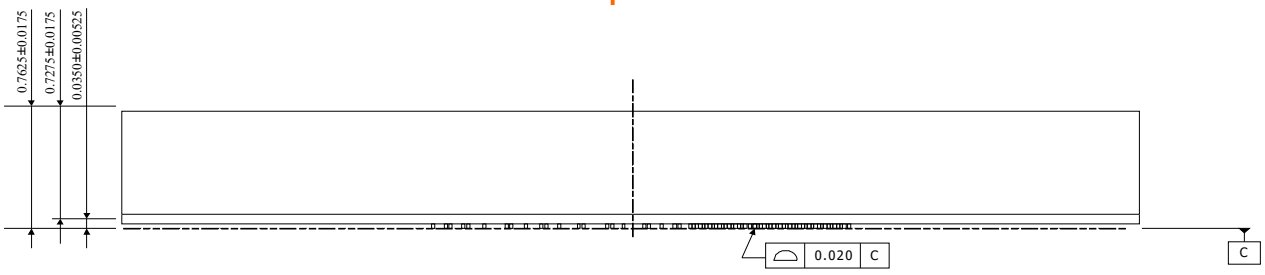
2.2. Ordering Information

Part Number	Power Supply	Clock Frequency	Data Rate	Density	# of DQs
H5VR64ESA8H-N0C	VDD/VDDQ=1.2	1,000MHz	2.0Gbps	8GB	x1024
H5VR32ESA4H-N0C	VDD/VDDQ=1.2	1,000MHz	2.0Gbps	4GB	x1024
H5VR64ESA8H-N2C	VDD/VDDQ=1.2	1,200MHz	2.4Gbps	8GB	x1024
H5VR32ESA4H-N2C	VDD/VDDQ=1.2	1,200MHz	2.4Gbps	4GB	x1024

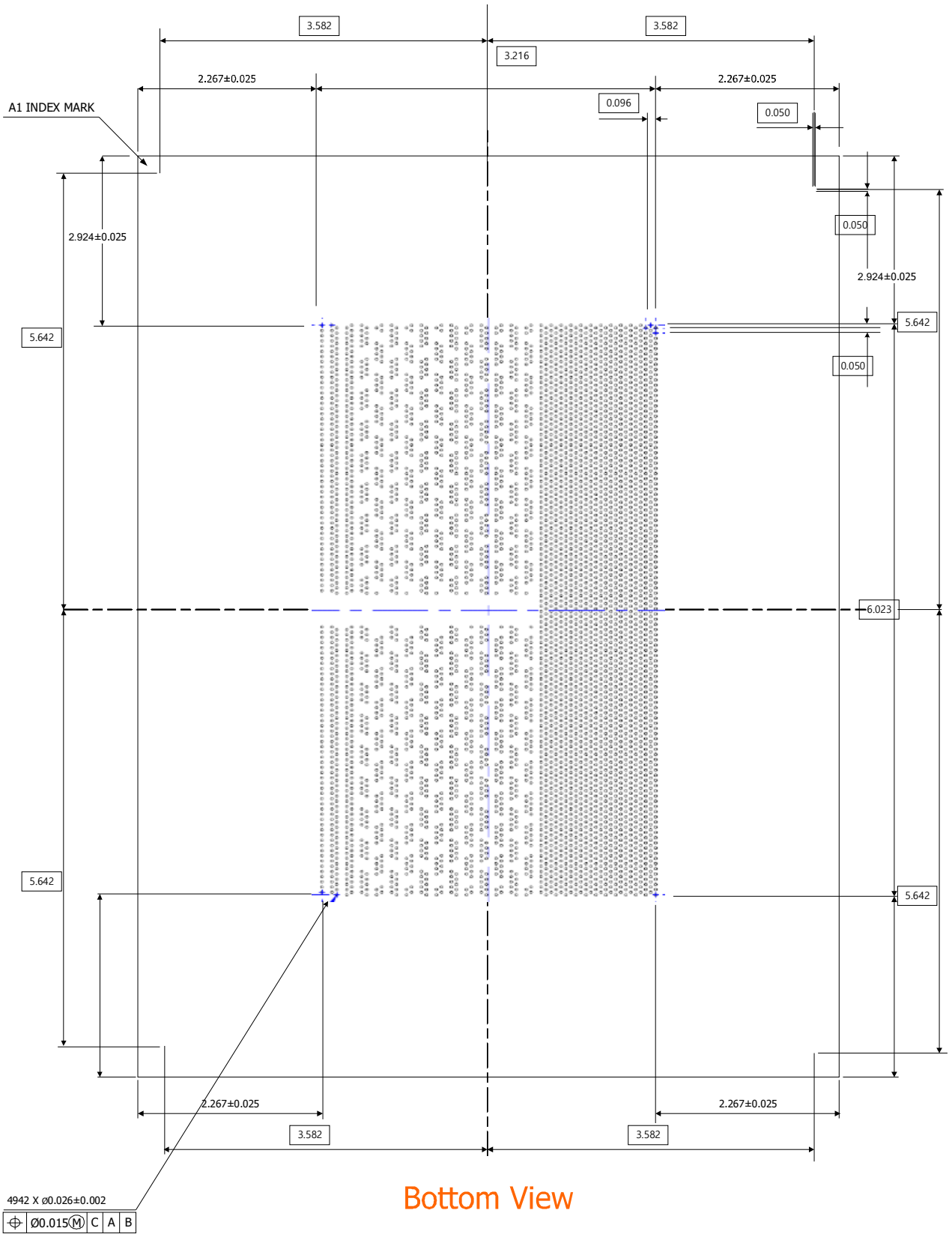
2.3. Mechanical specification



Top View



Front View


3.582
3.582
3.216
2.267±0.025
2.267±0.025
A1 INDEX MARK
0.096
0.050
0.050
2.924±0.025
2.924±0.025
5.642
5.642
0.050
6.023
5.642
5.642
2.267±0.025
2.267±0.025
3.582
3.582
4942 X ø0.026±0.002
Ø0.015Ⓜ C A B

Bottom View

3. HBM DRAM Organization

The HBM DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces called “channels”. It is anticipated that each DRAM stack will support up to 8 channels. Figure 1 shows an example stack containing 4 DRAM dies, each die supporting 2 channels. Each die contributes additional capacity and additional channels to the stack (up to a maximum of 8 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel may not access data attached to a different channel. Channels are independently clocked, and need not be synchronous.

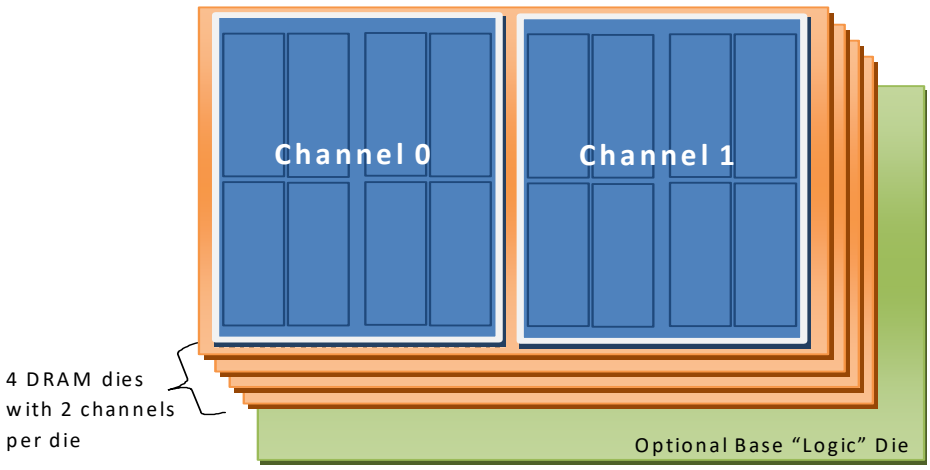


Figure 1. General Overview of a DRAM Die Stack with Channels

The DRAM vendor may choose to require an optional interface die that sits at the bottom of the stack and provides signal redistribution and other functions. The vendor may choose to implement many of the logic functions typically found on DRAM die on this logic die. This standard does not explicitly require nor prohibit such a solution.

The division of channels among the DRAM dies within a stack is left to the vendor. The example above, with the memory for two channels implemented on each die, is not a required organization. Organizations are permitted where the memory for a single channel is distributed among multiple dies; however, all accesses within a single channel must have the same latency for all accesses. Similarly, vendors may develop products where each memory die can flexibly support 1, 2, or 4 channels – enabling 8-channel configurations with stacks of 2 to 8 dies while keeping all data for a given channel on one die.

Since each channel is independent, much of this standard will describe a single channel. Where signal names are involved, families of signals belonging to a given channel will have the suffix a, b, …, h for channels a through h. If no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

3.1. Channel Definition

Each channel consists of an independent command and data interface. RESET_n, IEEE1500 test port and power supply signals are common to all channels. A channel provides access to a discrete pool of memory; no channel may access the memory storage for a different channel.

Each channel interface provides an independent interface to a number of banks of DRAM of a defined page size. See Table 4 .

3.2. Summary of Per-Channel Signals

Table 1 outlines the signals required for each channel, and Table 2 adds global signals that are required once per HBM device. See also Table 79 for 15 additional global signals associated with the IEEE1500 test access port.

Table 1 - Single Channel Signal Count

Function	# of uBumps	Notes
Data	128	DQ[127:0]
Column Command/Address	8	8 bits C[7:0]
Row Command/Address	6	6 bits R[5:0]
DBI	16	1 DBI per 8 DQs
DM	16	1 DM per 8 DQs
PAR	4	1 PAR per 32 DQs
DERR	4	1 DERR per 32 DQs
Strobes	16	1 RDQS_t/RDQS_c, WDQS_t/WDQS_c per 32 DQs
Clock	2	CK_t/CK_c
CKE	1	CKE
AERR	1	AERR
Redundant data	8	RD[7:0]
Redundant Row	1	RR
Redundant Column	1	RC
Total	212	

Table 2 - Global Signal Count

Function	# of uBumps	Notes
Reset	1	RESET_n
TEMP[2:0]	3	TEMP[2:0]
CATTRIP	1	Catastrophic Temperature Sensor
Total	5	

3.2.1. Legacy Mode and Pseudo Channel Mode

HBM DRAM defines two mode of operation depending on channel density. The mode support is fixed by design and is indicated on bits [17:16] of the DEVICE_ID wrapper register.

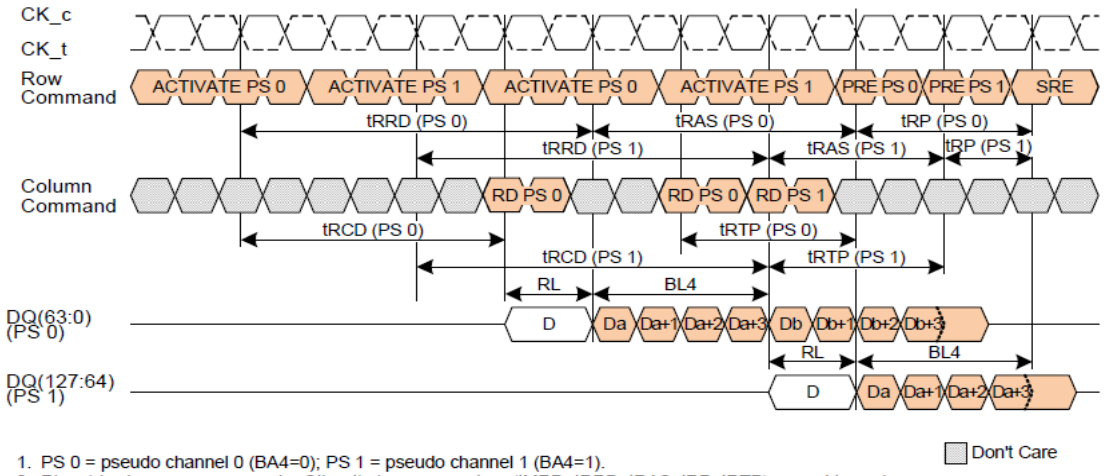
Legacy mode provides 256 bit prefetch per memory Read and Write access. Address bit BA4 is a “Don’t Care” in this mode.

Pseudo channel mode divides a channel into two individual sub-channels of 64 bit I/O each, providing 128 bit prefetch per memory read and write access for each pseudo channel. Pseudo channel mode requires that the burst length (BL) is set to 4, and each read or write access is internally executed as two seamless array accesses. The prefetch as seen by the memory controller therefore is 2x 128 bit = 256 bit per pseudo channel.

Both Pseudo channels operate semi independent: they share the channel’s row and column command bus as well as CK and CKE inputs, but decode and execute commands individually as illustrated in Figure 2. Address BA4 is used to direct commands to either to Pseudo Channel 0 (PS0, BA4 = 0) or Pseudo Channel 1 (PS1, BA4 = 1). Power-down and Self-Refresh are common to both Pseudo channels due to the shared CKE pin. Array access timings as listed in the table below are applicable for each individual pseudo channel. For example, an ACTIVATE to PS0 can be followed by an ACTIVATE to PS1 as shown in Figure 2. However a subsequent ACTIVATE to PS0 can only be done after t_{RRD} (PS0). For commands that are common to both Pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both Pseudo channels when issuing that command. Pseudo channel mode requires that burst length is set to 4. Both Pseudo channels also share the channel’s mode registers. All I/O signals of DWORD0 and DWORD1 are associated with Pseudo channel 0, and all I/O signals of DWORD2 and DWORD3 with Pseudo channel 1.

Table 3 - Array Access Timings Counted Individually Per Pseudo Channel

Array Timing Group	Timing Parameters
Row Access Timings	t_{RC}, t_{RAS}, t_{RCDRD}, t_{RCDWR}, t_{RRDL}, t_{RRDS}, t_{FAW}, t_{RTPL}, t_{RTPS}, t_{RP}, t_{WR},
Column Access Timings	t_{CCDL}, t_{CCDS}, t_{CCDR}, t_{WTRL}, t_{WTRS}, t_{RTW},
Refresh Timings	t_{RFC}, t_{RFCSB}, t_{RREFD}, t_{REFI}, t_{REFISB}, t_{RTW},



1. PS 0 = pseudo channel 0 (BA4=0); PS 1 = pseudo channel 1 (BA4=1).
2. RL = 1 is shown as an example. Other timings parameters (tMRD, tRRD, tRAS, tRP, tRTP) are not to scale.
3. Timing parameters like tRCD, tRRD, tRAS, tRP, tRTP apply independently for pseudo channels 0 and 1.
4. Self refresh entry (SRE) requires that tRP is satisfied in both pseudo channels.

Figure 2. Pseudo Channel Mode Operation

3.2.2. Dual Command Interfaces

To enable higher performance, HBM DRAMs exploit the increase in available signals in order to provide semi-independent row and column command interfaces for each channel. These interfaces increase command bandwidth and performance by allowing read and write commands to be issued simultaneously with other commands like activates and precharges. See Commands .

3.2.3. Addressing

Table 4 - HBM Cahnnel Addressing

	Channel Density Legacy Mode [6]			Channel Density Pseudo Channel (PC) Mode [5,6]				Notes
	1 Gb	2 Gb	4 Gb	2 Gb	4 Gb	8 Gb	8 Gb	
Prefetch Size (bits)	256	256	256	256 per PC	256 per PC	256 per PC	256 per PC	1,4
Row Address	RA12:RA0	RA13:RA0	RA13:RA0	RA13:RA0	RA13:RA0	RA13:RA0	RA13:RA0	
Column Address	CA5:CA0	CA5:CA0	CA5:CA0	CA5:CA1	CA5:CA1	CA5:CA1	CA5:CA1	2,3
Bank Address	BA2:BA0	BA2:BA0	BA3:BA0	BA2:BA0	BA3:BA0	BA3:BA0	SID, BA3:BA0	8
Page Size	2 KB	2 KB	2 KB	1 KB per PC	1 KB per PC	1 KB per PC	1 KB per PC	1,4
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	
Refresh Period	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	

NOTE 1 Prefetch size and page size reflect the effective addressing along with row and column commands.

NOTE 2 The burst order of a BL2 burst is fixed for Reads and Writes, and the HBM device does not assign a column address bit to distinguish between the first and second UI of a BL2 burst. A memory controller may internally assign such a column address bit but that column address bit is not transmitted to the HBM device. BL2 bursts are supported in legacy mode only.

NOTE 3 The burst order of a BL4 burst in pseudo channel mode is fixed for Reads and Writes, and the HBM device does not assign column address bits to distinguish between the four UI of a BL4 burst. A memory controller may internally assign such column address bits but those that column address bits are not transmitted to the HBM device. A BL4 burst is internally executed as two consecutive BL2 bursts.

NOTE 4 Page Size = 2^COLBITS * (Prefetch Size / 8); where COLBITS is the number of column address bits. Prefetch size and page size are for the configuration without ECC bits.

NOTE 5 In pseudo channel mode, an additional address bit BA4 is provided for row and column commands to direct commands either to pseudo channel 0 (BA4=0) or pseudo channel 1 (BA4=1). See Table 30 and Table 31.

NOTE 6 The HBM device indicates the support of Legacy Mode and/or pseudo channel Mode in bits [17:16] of the DEVICE_ID Wrapper Data Register.

NOTE 7 The “8 Gb 8-High” addressing is a specific configuration that is optimized for an HBM stack using 8 DRAM dies. The stack height of all other configuration is vendor specific.

NOTE 8 The stack ID (SID) acts as a bank address bit in command execution. Specific AC timing parameters or variations on selected timing parameters may be linked to SID. Table 30 and Table 31 and the vendor datasheets should be consulted for details.

3.2.4. Bank Groups

The activity within a bank group must be restricted to ensure proper operation of the device for HBM DRAMs operating at frequencies above a certain threshold f_{CKBG}. The banks within a device are divided into four or eight bank groups. The bank group feature is configurable via MRS. The assignment of banks to bank groups is shown in Table 5.

Different timing parameters are specified depending on whether back-to-back accesses are within the same bank group or across bank groups at shown in bank group or across bank groups at shown in Table 6.

Table 5 - Bank Group Assignments

Bank	8 Banks (BA2:BA0)	16 Banks (BA3:BA0)	32 Banks (SID, BA3:BA0)
0	Group A	Group A	Group A
1			
2	Group B		
3			
4	Group C	Group B	Group B
5			
6	Group D		
7			
8	N/A	Group C	Group C
9			
10			
11			
12		Group D	Group D
13			
14			
15			
16		N/A	Group E
17			
18			
19			
20			Group F
21			
22			
23			
24			Group G
25			
26			
27			
28			Group H
29			
30			
31			

Table 6 - Command Sequence Affected by Bank Groups

Command Sequence	Corresponding AC timing parameters			Notes
	Bank Groups Disable	Bank Groups Enabled		
		Accesses to different bank groups	Accesses within the same bank group	
ACTIVATE to ACTIVATE	t_{RRDS}	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS}	t_{CCDS}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	t_{RTPS}	t_{RTPS}	t_{RTPL}	1

Note 1 : Parameters t_{RTPS} and t_{RTPL} apply only when READ and PRECHARGE go to the same bank; use t_{RTPS} when Bank Groups are disabled, and t_{RTPL} when Bank Groups are enabled.

4. Initialization

To power-up and initialize the HBM device into functional operation the sequence in section 4.1 must be followed. At any time after the power-up initialization, the HBM device may be reset using the sequence in section 4.2. A limited set of IEEE 1500 port instructions may be used within the initialization sequences, as described in section 4.3.

The interactions between HBM functional reset and the IEEE 1500 port reset are as follows (also see section 13):

- Functional reset requires that the IEEE 1500 port also be reset.
- The IEEE 1500 port can be reset at any time without impacting normal operation.
- The IEEE 1500 port may be brought out of reset and a limited set of instructions may be used after a minimum time after RESET_n has been deasserted. See section 4.3.
- If not needed, the IEEE 1500 port may be left in reset (WRST_n = LOW) during normal operation.

4.1. HBM Power-up and Initialization Sequence

HBM device must be powered up and initialized in a predefined manner. The following sequence and timing must be satisfied for HBM power up and initialization sequence. Also refer to Figure 3.

1. Apply power to the V_{DDC}, V_{DDQ} and V_{PP} supplies. The V_{DDC} supply must be applied before or at the same time as V_{DDQ}. The power supply ramp time between 300 mV and V_{DDC} must be less than or equal to tINIT0. During the power ramp, $V_{DDC} > V_{DDQ}$ and $(V_{DDC} - V_{DDQ}) < 0.3$ V. The V_{PP} supply must be applied before or at the same time as V_{DDC} and must be equal to or higher than V_{DDC} at all times. During power supply ramp time tINIT0, RESET_n, WRST_n and all other input signals may be in an undefined state (driven LOW or HIGH, or High-Z).
2. RESET_n must be driven LOW (below 0.2 * V_{DDQ}) before or at the same time when t_{INIT0} expires as shown in Figure 3 (time Ta). WRST_n must be driven LOW before or at the same time as RESET_n. All other input signals may be in an undefined state (driven LOW or HIGH, or High-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{INIT1} time with stable power. After tINIT6 time has elapsed, the HBM device drives RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and AERR and DERR signals LOW. It also drives CATTRIP LOW or HIGH according to the measured junction temperature. CKE must be driven LOW a minimum of t_{INIT2} time before RESET_n is driven HIGH.
3. After RESET_n is driven HIGH, CKE must remain LOW for a minimum time of t_{INIT3}. The HBM device resets into the precharged power-down state. During t_{INIT3}, the HBM device will read and apply internal fuse configuration data and perform I/O driver impedance calibration. At the same time the WRST_n signal may be optionally driven HIGH to enable a subset of the IEEE 1500 instructions (see "Initialization Sequence For Use Of Limited IEEE 1500 Instruction Including Lane Repairs" and "IEEE Standard 1500").
4. The CK clock shall be started, and stable clocks shall be maintained for minimum of t_{INIT4} time before driving CKE HIGH. Since CKE is a synchronous signal, the corresponding setup time to clock (t_{IS}) must be met. Also, RNOP and CNOP commands must be registered (with t_{IS} /t_{IH} satisfied). After CKE is registered

HIGH, a minimum t_{INIT5} time must be satisfied before issuing a first MRS command. At or before the time that CKE is driven HIGH, WDQS_t and WDQS_c must be driven to LOW and HIGH static levels, respectively.

5. Issue all MRS commands to configure the HBM device appropriately for the application setting.
6. The HBM device is now ready for normal operation.

Table 7 - Initialization Timing Parameters

Symbol	Description	Min	Max	Unit
t_{INIT0}	Power supply ramp time	0.01	200	ms
t_{INIT1}	RESET_n signal LOW time at power-up (after stable power)	200	-	us
t_{INIT2}	CKE LOW time before RESET_n deassertion	10	-	ns
t_{INIT3}	CKE and WRST_n LOW time after RESET_n deassertion	500	-	us
t_{INIT4}	Stable clock before CKE HIGH	10	-	nCK
t_{INIT5}	Idle time before first MRS command	200	-	ns
t_{INIT6}	RDQS_t, RDQS_c driven valid and AERR, DERR driven LOW after RESET_n assertion	-	100	ns
t_{PW_RESET}	RESET_n signal LOW time with stable power	1	-	us

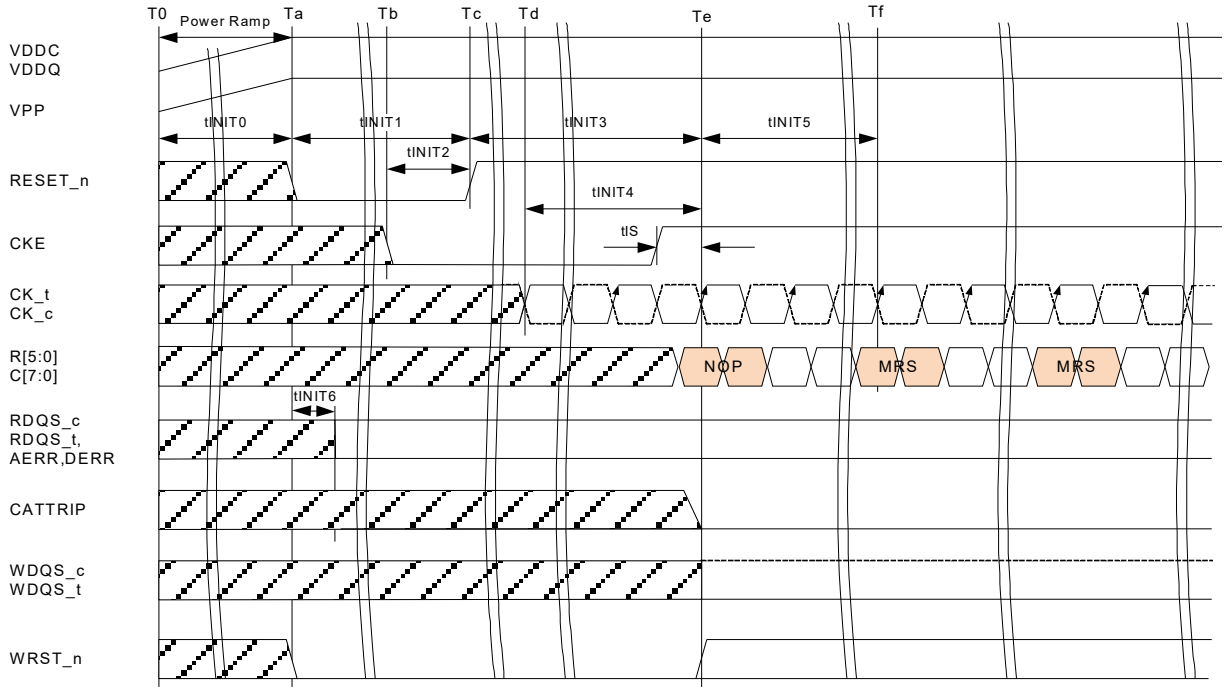


Figure 3. Power-up and Initialization

4.2. Initialization Sequence with Stable Power

The following sequence must be satisfied to perform a functional reset when power is kept stable at the HBM DRAM. See Figure 4.

1. tRESET_n must be driven LOW anytime when a functional reset is needed. WRST_n must be driven LOW before or at the same time as RESET_n. All other input signals may be in an undefined state (driven LOW or HIGH, or High-Z) at this point. RESET_n must be maintained LOW for a minimum of t_{PW_RESET}. CKE must be driven LOW a minimum of t_{INIT2} time before RESET_n is driven HIGH. Alternately, the IEEE 1500 port HBM_RESET instruction may be used to perform a re-initialization, with RESET_n continuing to be driven HIGH. Refer to "HBM RESET" section

2. Follow steps 3 to 6 as described in section "HBM Power-up and Initialization Sequence". Note that the CATTRIP output is sticky and not clearedby a functional reset.

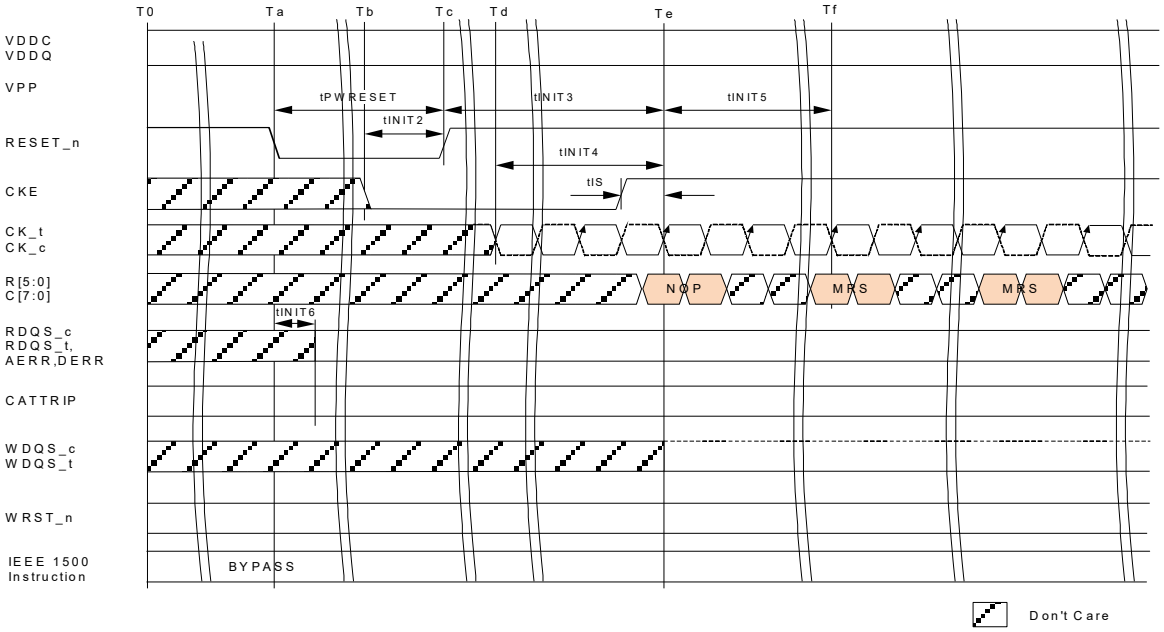


Figure 4. HBM RESET and Initialization Sequence with Stable Power

4.3. Initialization Sequence For Use Of Limited IEEE 1500 Instruction Including Lane Repairs

All IEEE 1500 port instructions are allowed after t_{INIT3} without completing the full initialization sequence.

Figure 5 illustrates usage of the EXTEST and SOFT_LANE_REPAIR instructions within the initialization sequence. This sequence may be applied as part of the power-up or stable-power initialization sequences to check for and correct failed connections on the row and column command buses, which must be correctly driven to RNOP and CNOP as part of the above initialization sequences. DWORD lane repairs are also allowed.

1. At time T_a, RESET_n and WRST_n must be driven LOW.

2. After a minimum time t_{INIT1} (if during an initial power-up sequence) or after t_{PW_RESET} (if during a stable power initialization sequence) RESET_n shall be driven HIGH. t_{INIT2} must also be met.

3. After t_{INIT3}, WRST_n is driven HI GH. IEEE 1500 port instructions may now be used. (Note that theWRST_n low pulse width $t_{WRSTL}$is met since t_{WRSTL} is less than the t_{INIT1} or t_{PW_RESET}). Refer to "IEEE1500 PORT INSTRUCTION INTERACTIONS" for timing requirements for operating the IEEE 1500 port, including t_{SWRST}. At this point, defective lane detection and soft lane repair may be executed. EXTEST operations may be applied to identify lanes needing repair. If soft lane repair is needed, SOFT_LANE_REPAIR operations can be applied after another RESET_n toggle, which is required after EXTEST instruction operation. A IEEE 1500 port BYPASS instruction should be applied to return all HBM signals to their normal functional mode after SOFT_LANE_REPAIR operations. Alternately, WRST_n may be driven LOW.

4. The initialization sequence may then continue per steps 4 to 6 of "HBM Power-up and Initialization Sequence", as needed.

During the t_{INIT3} period before WRST_n is driven HIGH, the HBM device executes various internal configuration operations, including applying hard lane repairs based on previously fused data. Executing soft lane repair instructions after t_{INIT3} overwrites any previously programmed hard lane repair data. It is suggested that the hard lane repair data is read from the HBM device and merged in any new lane repairs before applying the new soft lane repair operations. Any applicable IEEE 1500 port instructions timings must be met before continuing to time point T_h, such as t_{SLREP} if a SOFT_LANE_REPAIR instruction has been applied.

The EXTEST instructions are not required before applying the soft lane repair(s). Previously determined needed lane repairs may be applied as part of each initialization event.

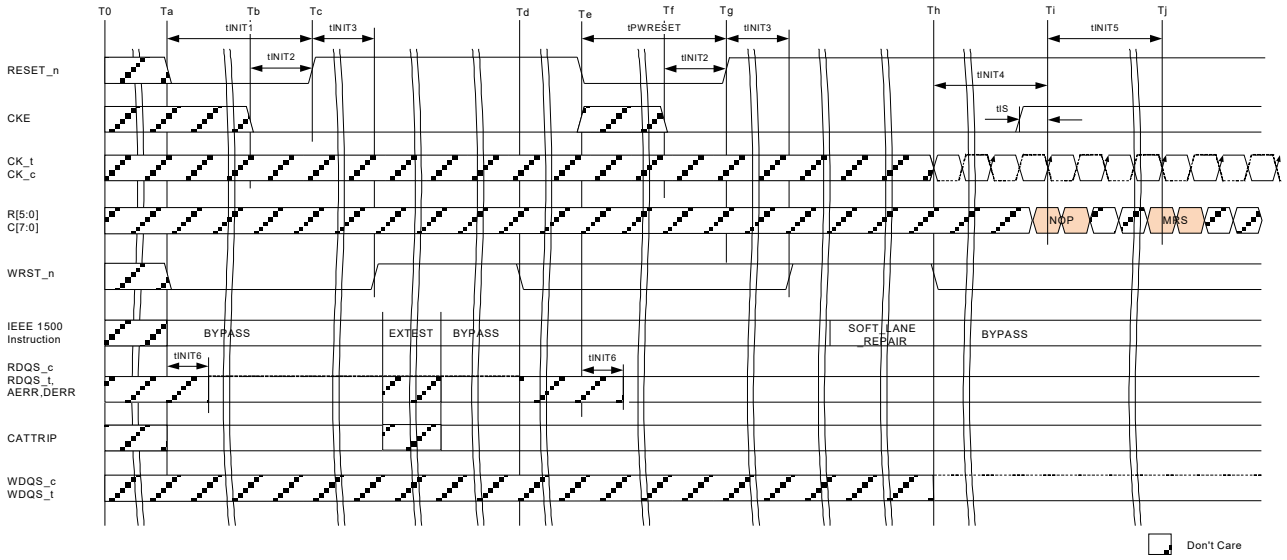


Figure 5. Initialization Sequence with Lane Repairs

5. Mode Registers

The mode registers define the specific mode of operation for the HBM device. MR0 to MR7 and MR15 are defined as shown in Figure 1. MR8 to MR14 are reserved. Reprogramming the mode registers does not alter the contents of the memory array.

All mode registers are programmed via the "Mode Register Set (MRS)" command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode registers must be loaded when all banks are idle and no bursts are in progress; the controller must wait the specified time tMOD before initiating any subsequent operations. Violating either of these requirements results in unspecified operation.

No default states are defined for mode registers except when otherwise noted. Users therefore must fully initialize all mode registers to the desired values upon power-up.

Reserved bits must be programmed to 0.

Table 8 - HBM Mode Register Overview

Mode Register	MRS Command C[7:4]	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR0 (Table 9)	0000	Test mode	ADD/ CMD Par- ity	DQ Write Parity	DQ Read Parity	Reserved	TCSR	DBIac Write	DBIac Read
MR1 (Table 10)	0001	Drive Strength			Write Recovery (WR)				
MR2 (Table 11)	0010	Read Latency (RL)					Write Latency (WL)		
MR3 (Table 12)	0011	BL	Bank Group	Active to Precharge (RAS)					
MR4 (Table 14)	0100	Reserved				Parity Latency (PL)		DM	ECC
MR5 (Table 15)	0101	TRR	TRR - PS Select	Reserved		TRR Mode BAn			
MR6 (Table 16)	0110	imPRE tRP Value							
MR7 (Table 17)	0111	CATTRIP	Reserved	MISR Control			Read Mux Control		Loop-back
MR8 (Table 19)	1000	Reserved							DA[28] Lockout
MR9	1001	Reserved							
MR10	1010	Reserved							
MR11	1011	Reserved							
MR12	1100	Reserved							
MR13	1101	Reserved							
MR14	1110	Reserved							
MR15 (Table 26)	1111	Reserved					Optional Internal Vref(Applies to DQ and Addr/CMD(bus)		

Table 9 - Mode Register 0 (MR0)

Field	Bits	Description
Test Mode	OP[7]	0 - Normal operation (Default) 1 - Test mode (vendor specific)
Address, Command Bus Parity for Row, Column Bus	OP[6]	0 - Disable (Default) 1 - Enable
DQ Bus Write Parity	OP[5]	0 - Disable (Default) 1 - Enable
DQ Bus Read Parity	OP[4]	0 - Disable (Default) 1 - Enable
Reserved	OP[3]	0
TCSR (Temperature Compensated Self Refresh)	OP[2]	0 - Disable 1 - Enable (Default)
Write DBIac	OP[1]	0 - Disable 1 - Enable (Default)
Read DBIac	OP[0]	0 - Disable 1 - Enable (Default)

Table 10 - Mode Register 1 (MR1)

Field	Bits	Description	Note
Nominal Drive Strength	OP[7:5]	000 - 6 mA driver (Default) 001 - 9 mA driver 010 - 12 mA driver 011 - 15 mA driver 100 - 18 mA driver All other encoding are reserved	1
Write Recovery WR (for Auto-Precharge Only)	OP[4:0]	00000 - Reserved 00001 - Reserved 00010 - Reserved 00011 - 3 nCK 00100 - 4 nCK 00101 - 5 nCK 00110 - 6 nCK ... 01011 - 11nCK ... 11111 - 31 nCK	2
NOTE1. 18mA driver encoding is not needed until higher speed operation such as 2 Gbps. NOTE2. HBM Stack is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.0505			

Table 11 - Mode Register 2 (MR2)

Field	Bits	Description	Note
Read Latency (RL)	OP[7:3]	00000 - 2 nCK (minimum) 00001 - 3 nCK 00010 - 4 nCK 00011 - 5 nCK 00100 - 6 nCK ... 01000 - 10 nCK 01001 - 11 nCK ... 11111 - 33 nCK	1
Write Latency (WL)	OP[2:0]	000 - 1 nCK (minimum) 001 - 2 nCK 010 - 3 nCK 011 - 4 nCK 100 - 5 nCK 101 - 6 nCK 110 - 7 nCK 111 - 8 nCK	1
NOTE 1. HBM stack is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous			

Table 12 - Mode Register 3 (MR3) Description

Field	Bits	Description	Note
Burst Length(BL)	OP[7]	0 - BL2 1 - BL4	
Bank Group	OP[6]	0 - Disable 1 - Enable (Default)	
Activate to Precharge RAS	OP[5:0]	000000 - Reserved 000001 - Reserved 000010 - Reserved 000011 - 3 nCK 000100 - 4 nCK 000101 - 5 nCK 000110 - 6 nCK ... 111111 - 63 nCK	1
NOTE 1. HBM stack is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous. NOTE 2. In Pseudo Channel mode, BL must be set to 4.			

Table 13 - MR3 - Burst Type and burst Order Definition - BL2

Burst Type	Burst Length	Read/Write	Burst Order
Sequential	2	Read	0, 1
		Write	0, 1

Table 14 - MR3 - Burst Type and burst Order Definition - BL4

Burst Type	Burst Length	Read/Write	Starting Column Address CA0	Burst Order	Notes
Sequential	4	Read	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2
		Write	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2

NOTE 1 Reads and Write are treated as two consecutive access with BL=2.

NOTE 2 Burst re-order via address bit CA0 is supported in legacy mode only. The burst order is fixed in pseudo channel mode and address bit CA0 is not defined.

Table 15 - Mode Register 4 (MR4)

Field	Bits	Description	Notes
Reserved	OP[7:4]	0x00	
Parity Latency (PL)	OP[3:2]	00 - 0 nCK	
Write Data Mask (DM)	OP[1]	0 - Enable 1 - Disable NOTE: DM and ECC cannot be enabled simultaneously. i.e., OP[1:0] = 01 is not allowed.	
ECC	OP[0]	0 - Disable 1 - Enable NOTE: DM and ECC cannot be enabled simultaneously. i.e., OP[1:0] = 01 is not allowed.	

Table 16 - Mode Register 5 (MR5)

Field	Bits	Description	Notes
TRR Mode	OP[7]	0 - Disable (default) 1 - Enable	
TRR Mode - Pseudo Channel Select	OP[6]	0 - Enable TRR mode for pseudo channel 0 1 - Enable TRR mode for pseudo channel 1	1,2
Reserved	OP[5:4]	00	
TRR Mode - Bank address	OP[3:0]	0000 - Bank 0 ... 1111 - Bank 15	

NOTE 1 Only applicable when MR5 OP[7] = 1.
NOTE 2 Only applicable when DEVICE_ID Wrapper Data Register bits [17:16] = 01.

Table 17 - Mode Register 6 (MR6)

Field	Bits	Description	Notes
imPRE t_{RP} Value	OP[7:3]	00000 - 2nCK (Minimum) 00001 - 3nCK 00010 - 4nCK 00011 - 5nCK ... 11111 - 33nCk	1,2

Table 17 - Mode Register 6 (MR6)

Field	Bits	Description	Notes
Reserved	OP[2:0]	000	
NOTE 1 HBM Stack is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous NOTE 2 imPRE is only available in pseudo channel mod. DEVICE_ID Wrapper Data Register bits [17:16] = 01.			

Table 18 - Mode Register 7 (MR7)

Field	Bits	Description	Notes
CATTRIP	OP[7]	0- Clear CATTRIP pin (default) 1 - Assert CATTRIP pin to "1"	1
Reserved	OP[6]	0	
DWORD MISR Control	OP[5:3]	Only applicable if Loopback is enabled in OP[0] 000 - Preset The DWORD MISR/LFSRs are set to 0xAAAAAh, and the DWORD LFSR_COMPARE_STICKY bits are set to all zeros. 001 - LFSR mode (read direction) 010 - Register mode (read and write directions) DWORD writes are captured directly into the MISR registers without compression. The MISR registers will contain the most recent write data. 011 - MISR mode (write direction) 100 - LFSR Compare mode (write direction)	
DWORD Read Mux Control	OP[2:1]	Only applicable if Loopback is enabled in OP[0] 00 - Reserved 01 - Return data from MISR registers (default) 10 - Return data from Rx path sampler 11 - Return LFSR_COMPARE_STICKY (optional)	
DWORD Loopback	OP[0]	0. Disable (default) 1 - Enable; enables link testing circuitry. All Writes and Reads will be to/from the MISR. (Does not require any additional Activation to Write/Reads - Column addresses are ignored in this mode.)	
NOTE 1 The CATTRIP pin can be asserted to "1" from any of the channels [a:h] MR7 [OP7] bit (logic OR). NOTE 2 See HBM Loopback Test Modes for DWORD MISR mode features and usage.			

Table 19 - Mode Register 8 (MR8)

Field	Bits	Description	Note
Reserved	OP[7:0]	0x00	

Table 19 - Mode Register 8 (MR8)

Field	Bits	Description	Note
DA[28] lockout	OP[0]	0 - Disable (default) 1 - Enable (See "DA[28] Lockout")	1
NOTE 1 : DA[28] lockout is defined for channels a and e only. Once enabled, the DA[28] lockout can only be cleared when power is removed. The bit is also not accessible via IEEE1500 instruction "MODE REGISTER DUMP SET"			

Table 20 - Mode Register 9 (MR9)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 21 - Mode Register 10 (MR10)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 22 - Mode Register 11 (MR11)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 23 - Mode Register 12 (MR12)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 24 - Mode Register 13 (MR13)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 25 - Mode Register 14 (MR14)

Field	Bits	Description
Reserved	OP[7:0]	0x00

Table 26 - Mode Register 15 (MR15)

Field	Bits	Description
Reserved	OP[7:3]	00000
Internal Vref	OP[2:0]	Optional HBM feature. HBM may simply ignore these bits if there is no internal Vref generator. If there is internal Vref, these bits are programmed appropriately. Applies to both DQ bus as well as Row/Column address/cmd bus. HBM has only one internal Vref generator across all 8 channels. These bits must programmed identically in all eight mode registers. 000 - 0.50 * V_{DDQ} 001 - 0.46 * V_{DDQ} 010 - 0.42 * V_{DDQ} 011 - 0.38 * V_{DDQ} 100 - 0.54 * V_{DDQ} 101 - 0.58 * V_{DDQ} 110 - 0.62 * V_{DDQ} 111 - 0.66 * V_{DDQ}

6. Operation

6.1. Clocking Overview

The HBM device captures data on row bus and column bus using differential CK_t/CK_c. The row and column bus operate at double data rate. The CKE input signal is captured only on the rising edge of CK_t signal.

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32 DQ bits (DWORD). The data bus operate at double data rate. The data is captured on both rising and falling edge of WDQS_t for Write operation and RDQS_t for Read operation.

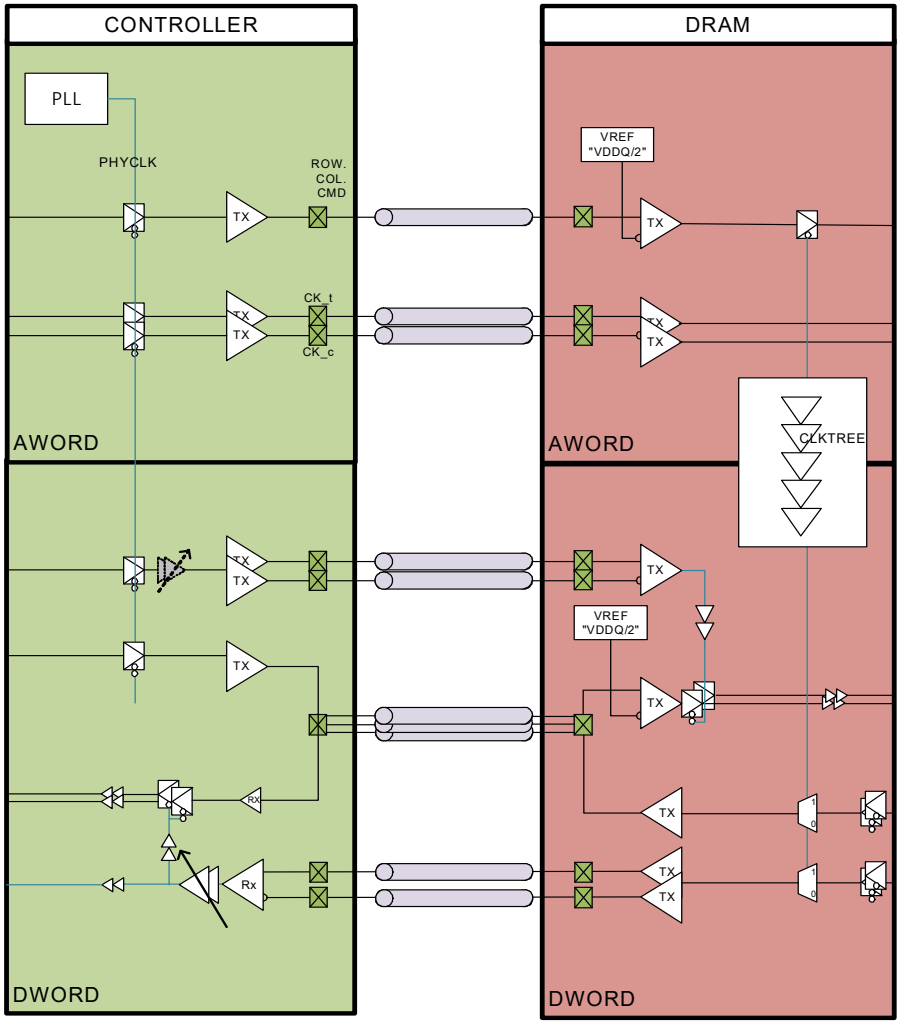


Figure 6. High level block diagram example of clocking scheme

6.2. HBM Write Data Mask (DM), Data Bus Inversion (DBIac) Function and ECC

The HBM device supports Write Data Mask (DM), Data Bus Inversion (DBIac) and optionally ECC with byte granularity. One Data Mask (DM) pin and one Data Bus Inversion (DBI) pin per byte are provided as shown in Table 27. DBI is a bi-directional DDR pin and driven or sampled along with the DQ pins for Read and Write operation. DM is a bi-directional DDR pin and driven or sampled along with DQ signals pins for Read or Write operation when used with ECC (see below); the pin is input only and used for Write operations when used with Write Data Mask.

Table 27 - DM DBI to DQ Correspondence and Even/Odd Byte Groups

DQ Signals	DBI Signal	DM Signal	Byte Type
DQ[7:0]	DBI0	DM0	Even Byte
DQ[15:8]	DBI1	DM1	Odd Byte
DQ[23:16]	DBI2	DM2	Even Byte
DQ[31:24]	DBI3	DM3	Odd Byte
DQ[39:32]	DBI4	DM4	Even Byte
DQ[47:40]	DBI5	DM5	Odd Byte
DQ[55:48]	DBI6	DM6	Even Byte
DQ[63:56]	DBI7	DM7	Odd Byte
DQ[71:64]	DBI8	DM8	Even Byte
DQ[79:72]	DBI9	DM9	Odd Byte
DQ[87:80]	DBI10	DM10	Even Byte
DQ[95:88]	DBI11	DM11	Odd Byte
DQ[103:96]	DBI12	DM12	Even Byte
DQ[111:104]	DBI13	DM13	Odd Byte
DQ[119:112]	DBI14	DM14	Even Byte
DQ[127:120]	DBI15	DM15	Odd Byte

6.2.1. Write Data Mask (DM)

Write data mask (DM) function can be enabled per MR4 OP[1] (see Table 15)
DQ inputs are masked in case DM is sampled HIGH and DQ input signals are don't care (either valid HIGH or LOW); DQ input signals are valid and write data is written to the DRAM array in case DM is sampled LOW.

Please note that when DQ parity is enabled for Writes, the data inputs are included in the parity calculation regardless whether a byte is masked by DM or not.

Table 28 - Write Data Mask (DM)

Function	DM	DQ
Write Enable	LOW	Valid
Write Inhibit	HIGH	Ignored

6.2.2. Error Correction Code (ECC)

HBM DRAM devices may optionally support ECC (one bit per data byte). The HBM DRAM itself does not compute any ECC. The HBM DRAM provides the additional DRAM cells to store ECC information. ECC bits are not included in parity calculation when Write or Read DQ Parity Function is enabled (see Table 37). The ECC function can be enabled or disabled per MR4 OP[0].

6.2.3. DM & ECC Function Combinations

Table 29 summarizes the DM pin function as configured by MR4 OP[1:0].

Table 29 - DM Pin Function

MR		Write Data MASK (DM)	Error Correction Code (ECC)	DM Pin Function
OP[1]	OP[0]			
0	0	Enabled	Disabled	Input only
0	1	Not allowed		Undefined
1	0	Disabled	Disabled	High-Z (input receivers and output drivers turned off
1	1	Disabled	Enabled	Bi-directional

6.2.4. DBIac Function

DBIac function can be enabled or disabled independently for Write and Read operation per HBM mode register MR0 OP[1] and OP[0] respectively (see Table 9).
When both Write and Read DBIac function is disabled in mode register, DBI signal is a don’t care for HBM device. HBM DBI input receivers and output drivers are turned off.

6.2.4.1. DBIac Disabled

HBM devices supports byte granular Data Bus Inversion during Write and Read operation. In this standard, the word DBI refers to internal state of the device unless explicitly noted as DBI signal or pin.

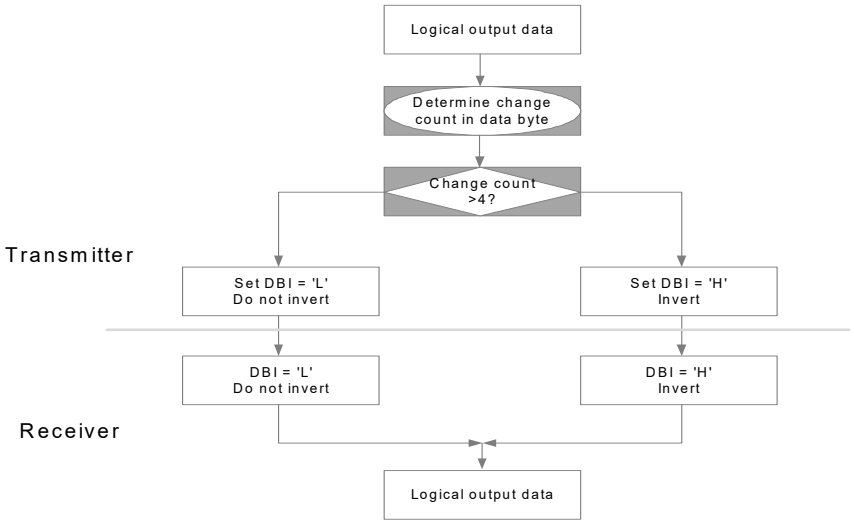


Figure 7. DBIac algorithmD

HBM device supports byte granular Data Bus Inversion during Write and Read operation. In this standard, the word DBI refers to internal state of the device unless explicitly noted as DBI signal or pin.

Write Operation - HBM device inverts Write data received on the DQ inputs in case DBI is sampled HIGH, or leaves the Write data non-inverted in case DBI is sampled LOW. Note that DM input is not affected by the DBIac function.

Read Operation - HBM device counts the number of DQ signals that are transitioning from previous state. Note that DM output is not affected by the DBIac function. See Read Operation under DBIac States section for bus pre-condition. The HBM device inverts Read data and sets DBI HIGH when the number of transitioning data bits within a byte is greater than 4, or when the number of transitioning data bits within a byte equals 4 and DBI was High; otherwise the HBM device does not invert the Read data and sets DBI LOW.

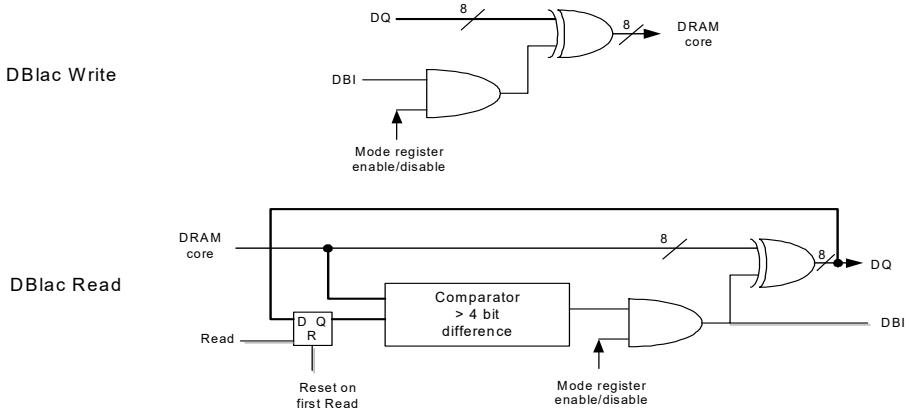


Figure 8. Example DBIac Logic for Write and Read

6.2.5. DBIac States

The HBM device resets DBIac value to LOW (All eight DQs and DBI signals within a byte group) whenever any of the following four events occur:

- RESET_n signal de-assertion
- The HBM device registers Mode Register Set command (MRS)
- The HBM device registers Read or Read w/AP command after Write command. Note that HBM device is only required to reset DBIac value 1/2 clock prior to Read operation begins and hence it may reset DBIac value anytime before that.
- Self Refresh exit

  For all other events or commands registered by the HBM, the DBIac value is not reset to LOW and the HBM device will use its previous value for DBIac calculation.

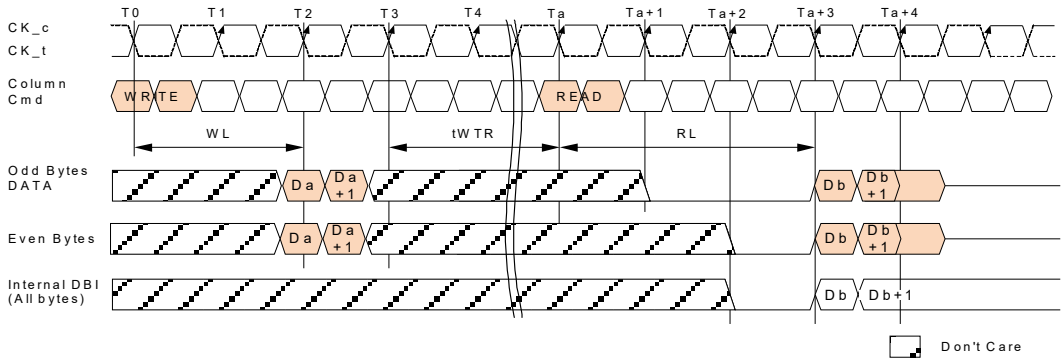


Figure 9. Write followed by Read Timing; BL=2

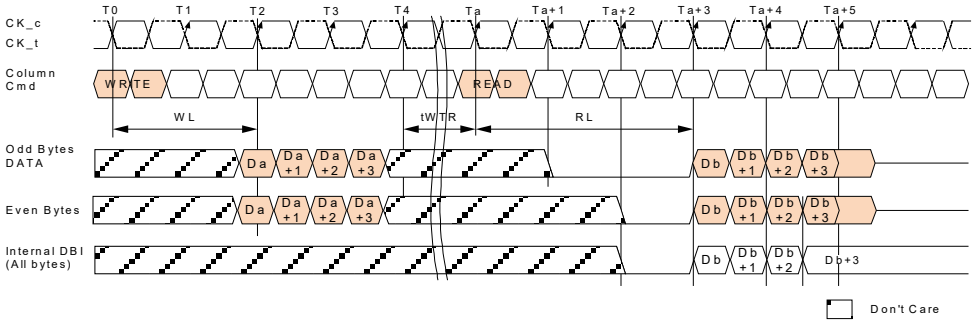


Figure 10. Write followed by Read Timing; BL=4

6.2.5.1. Read Operation

First Read Command:

When a first Read command is registered after a DBI reset, HBM device pre-conditions the bus to LOW over 2 tCK period prior to Read data. HBM drives odd byte signals to LOW 2 tCK prior to Read data and even byte signals to LOW 1 tCK prior to Read data.When DBIac function is disabled in MR, HBM device does not pre-condition the bus as described. The PAR signal is not included in the DBI calculation and therefore not preconditioned to LOW; its initial state is undefined (LOW or HIGH).

Consecutive Read Commands (Seamless and non-seamless):

Once the Read DQ burst is complete, the HBM device tri-states DBI, DM and all DQ output drivers. However, the HBM device must store the last beat of all DQ, DM and DBI states and use that to precondition the bus prior to Read data and for Read DBIac calculation for any subsequent Read operation barring a condition to DBI reset. For back to back Read operation with a gap, the HBM device preconditions all DQ, DM and DBI to last beat of previous burst over 2 tCK period prior to Read data. HBM drives Odd byte signals to previous state 2 tCK prior to Read data and Even byte signals to previous state 1 tCK prior to Read data.

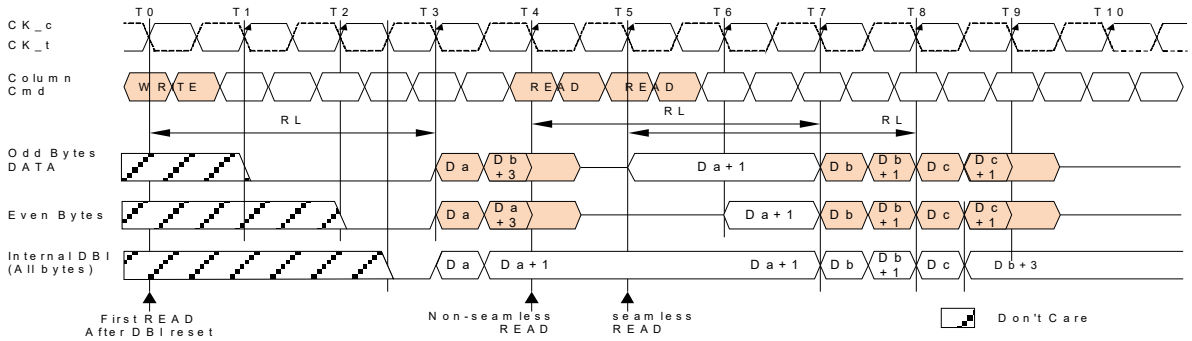


Figure 11. Read Timing : BL=2

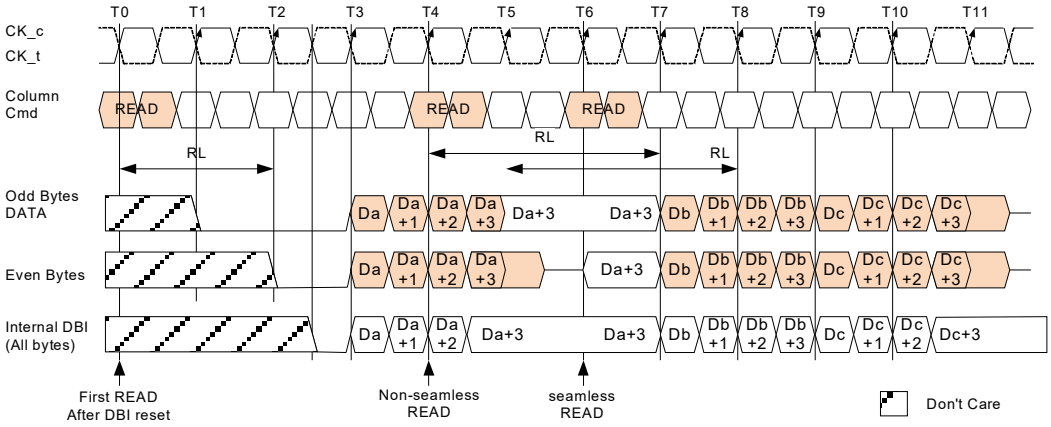


Figure 12. Read Timing : BL=4

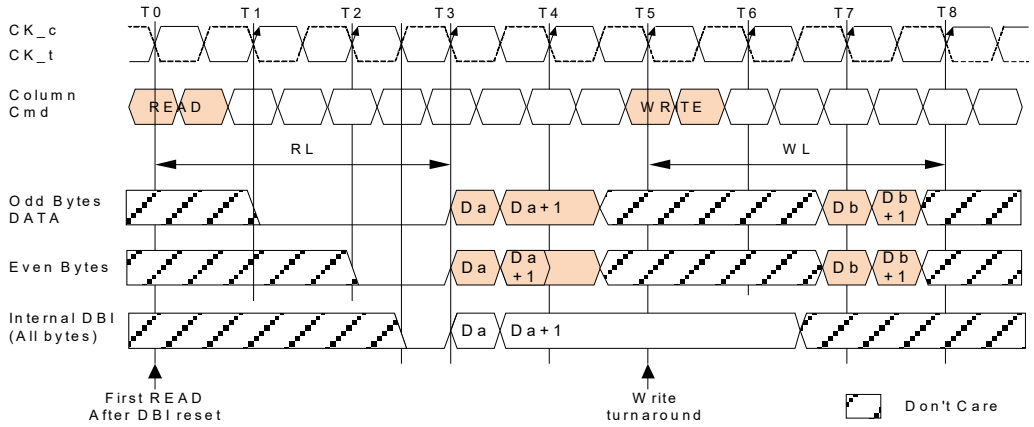


Figure 13. Read followed by Write Timing : BL=2

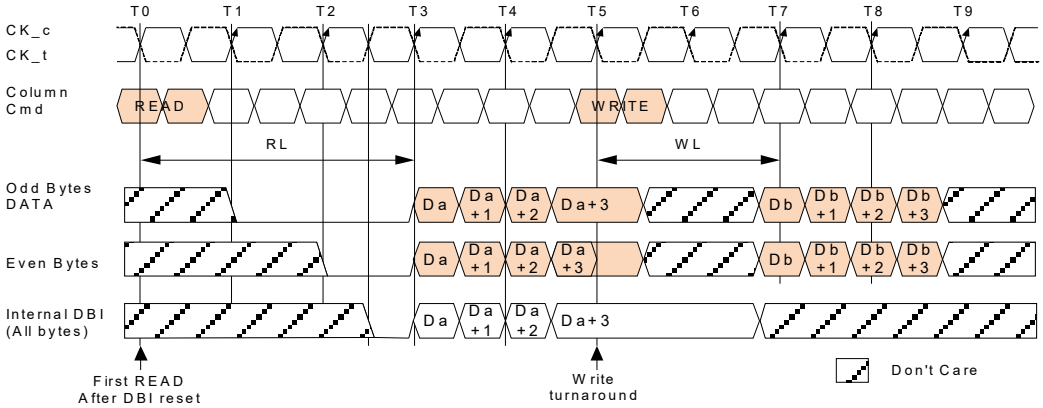


Figure 14. Read followed by Write Timing : BL=4

6.3. Commands

The HBM DRAM features DDR commands entered on each positive CK_t, CK_c edge. Row Activate commands require two cycles, other row and column commands require only one cycle.

6.3.1. Command Truth Table

Table 30 - Row Commands Truth Table

Function	Symbol	Clock Cycle	CKE		R[0]	R[1]	R[2]	R[3]	R[4]	R[5]	Notes
			(n-1)	n							
Row No Operation	RNOP	Rising	H	H	H	H	H	V	V	V	1,4,7
		Falling			V	V	PAR	V	V	V	
Activate	ACT	Rising	H	H	L	H	RA14/ SID	BA0	BA1	BA2	1,2,3,4,7, 8
		Falling			RA11	RA12	PAR	RA15/ BA4	RA13	BA3	
		Rising			RA5	RA6	RA7	RA8	RA9	RA10	
		Falling			RA0	RA1	PAR	RA2	RA3	RA4	
Precharge	PRE	Rising	H	H	H	H	L	BA0	BA1	BA2	1,3,4,7, 8, 9, 10
		Falling			V	V/SID	PAR	BA4	L	BA3	
Precharge All	PREA	Rising	H	H	H	H	L	V	V	V	1,3,4,7,8,9
		Falling			V	V	PAR	BA4	H	V	
Single Bank Refresh	REFSB	Rising	H	H	L	L	H	BA0	BA1	BA2	1,3,4,7,8,9 ,10
		Falling			V	V/SID	PAR	BA4	L	BA3	
Refresh	REF	Rising	H	H	L	L	H	V	V	V	1,4,7,8
		Falling			V	V	PAR	BA4	H	V	
Power Down Entry	PDE	Rising	H	L	H	H	H	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	
Self Refresh Entry	SRE	Rising	H	L	L	L	H	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	
Power Down & Self Refresh Exit	PDX/SRX	Rising	L	H	H	H	H	V	V	V	1,5,6,7
		Falling			V	V	V	V	V	V	

Table 30 - Row Commands Truth Table

Function	Symbol	Clock Cycle	CKE		R[0]	R[1]	R[2]	R[3]	R[4]	R[5]	Notes
			(n-1)	n							

NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but floating).

NOTE 2 The unused upper row address bits RA13, RA14 and RA15 to Valid signal level depending on the DRAM density; they are evaluated in the parity calculation if the parity function is enabled in the mode register.

NOTE 3 For 8 bank device, BA3 must be driven to Valid signal level; it is evaluated in the parity calculation if the parity function is enabled in the mode register.

NOTE 4 PAR signal must be driven to Valid signal level even if Parity function is disabled in DRAM mode register.

NOTE 5 No Parity checking at Power Down Exit or Self Refresh Exit command. The HBM device requires RNOP and CNOP commands on Row and Column bus respectively with valid parity if enabled during power down exit period (tXP) and self refresh exit period(tXS).

NOTE 6 CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising clock edge. Refer to CKE Truth Table for more detail with CKE transitions.

NOTE 7 All other command encoding not shown in the table for pins R[4,2:0] at the rising clock edge are reserved commands for future use.

NOTE 8 BA4 applies to only Pseudo channel mode. BA4 = 0 means Pseudo Channel 0; BA4 = 1 means Pseudo Channel 1. See "Legacy Mode and Pseudo Channel Mode" for detailed explanation of Pseudo channel mode operation and timing. The Pseudo channel not selected by BA4 performs a RNOP.

NOTE 9 The SID acts as bank address bit in conjunction with ACT, PRE and REFSB commands, and related timing diagrams shall be interpreted accordingly. PREA and REF commands do not use SID.

NOTE 10 Timing parameter tFAW may have two values depending on whether related commands refer to the same or a different SID. Vendor datasheets should be checked for details.

Table 31 - Column Commands Truth Table

Function	Symbol	Clock Cycle	CKE		C[0]	C[1]	C[2]	C[3]	C[4]	C[5]	C[6]	C[7]	Notes
			(n-1)	n									
Column No Operation	CNOP	Rising	H	H	H	H	H	V	V	V	V	V	1,4,5,6
		Falling			V	V	PAR	V	V	V	V	V	
Read	RD	Rising	H	H	H	L	H	L	BA0	BA1	BA2	BA3	1,2,3,4,5,6,7,8,9
		Falling			CA0/V/SID	CA1	PAR	CA2	CA3	CA4	CA5	CA6/BA4	
Read w/ AP	RDA	Rising	H	H	H	L	H	H	BA0	BA1	BA2	BA3	1,2,3,4,5,6,7,8,9
		Falling			CA0/V/SID	CA1	PAR	CA2	CA3	CA4	CA5	CA6/BA4	
Write	WR	Rising	H	H	H	L	L	L	BA0	BA1	BA2	BA3	1,2,3,4,5,6,7,8
		Falling			CA0/V/SID	CA1	PAR	CA2	CA3	CA4	CA5	CA6/BA4	
Write w/ AP	WRA	Rising	H	H	H	L	L	H	BA0	BA1	BA2	BA3	1,2,3,4,5,6,7,8
		Falling			CA0/V/SID	CA1	PAR	CA2	CA3	CA4	CA5	CA6/BA4	
Mode Register Set	MRS	Rising	H	H	L	L	L	OP7	BA0	BA1	BA2	BA3	1,2,4,5,6
		Falling			OP0	OP1	PAR	OP2	OP3	OP4	OP5	OP6	

Table 31 - Column Commands Truth Table

Function	Symbol	Clock Cycle	CKE		C[0]	C[1]	C[2]	C[3]	C[4]	C[5]	C[6]	C[7]	Notes
			(n-1)	n									

NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but not floating).

NOTE 2 The unused upper row address bits RA13, RA14 and RA15 to valid signal level depending on the DRAM density; they are evaluated in the parity calculation if the parity function is enabled in the mode register.

NOTE 3 For 8 bank device, BA3 must be driven to valid signal level; it is evaluated in the parity calculation if the parity function is enabled in the mode register.

NOTE 4 PAR signal must be driven to valid signal level even if Parity function is disabled in DRAM mode register.

NOTE 5 CKE transition from HIGH to LOW or LOW to HIGH must be accompanied with a Column No Operation (CNOP) command. Refer to CKE Truth Table for more detail with CKE transitions.

NOTE 6 All other command encoding not shown in the table for pins R[4,2:0] at the rising clock edge are reserved commands for future use.

NOTE 7 BA4 applies to only Pseudo channel mode. BA4 = 0 means Pseudo Channel 0; BA4 = 1 means Pseudo Channel 1. See Section "Legacy Mode and Pseudo Channel Mode" for detailed explanation of Pseudo channel mode operation and timing. The Pseudo channel not selected by BA4 performs a CNOP.

NOTE 8 The SID acts as bank address bit in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly.

NOTE 9 HBM configurations using the SID specify a timing parameter for consecutive READs to different SID. Vendor datasheets should be checked for details.

Table 32 - CKE Truth Table

Current State	CKE		Row Command	Action	Notes
	Previous Cycle (n-1)	Current Cycle (n)			
Power Down	L	L	X	Maintain Power Down	1,4,6,7
	L	H	RNOP	Power Down Exit	1,2,3,8
Self Refresh	L	L	X	Maintain Self Refresh	1,4,9
	L	H	RNOP	Self Refresh Exit	1,2,3,8
Bank(s) Active	H	L	RNOP	Active Power Down Entry	2,3,6,7
Precharging	H	L	RNOP	Power Down Entry	2,3,6,7
Refreshing	H	L	RNOP	Power Down Entry	2,3,6,7
All Banks Idle	H	L	RNOP	Precharge Power Down Entry	2,3,6,7
	H	L	REF	Self Refresh Entry	2,4,5,9

NOTE 1. X = Don't care (Command decoder disabled).

NOTE 2. CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising clock edge.

NOTE 3. With CKE transition from HIGH to LOW or LOW to HIGH, CNOP commands must be registered on Column bus.

NOTE 4. In Power Down state (either Active or Precharge) and Self Refresh State, Row and Column bus signals are X (Don't care; either H or L or floating).

NOTE 5. Self Refresh mode can only be entered from All Banks Idle state. Idle state is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is HIGH and all timing from previous operations are satisfied as well as all Self Refresh Exit and Power Down Exit timing parameters are satisfied.

NOTE 6. The Power Down state (either Active or Precharge) does not perform any refresh operation.

NOTE 7. In Power Down mode, clocks may be turned off after tTBD.

NOTE 8. Clocks must be valid and stable tTBD time prior to Power Down and tCKSRX prior to Self Refresh exit.

NOTE 9. In Self Refresh, clocks may be turned off after tTBD.

6.3.2. Row Command

6.3.2.1. Row No Operation Command(RNOP)

The ROW NO OPERATION (RNOP) command as shown in Figure 15 is used to instruct the HBM device to perform a NOP as row command; this prevents unwanted row commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated on all R[5:0] inputs when the parity calculation is enabled in the Mode Register.

RNOP is assumed on subsequent timing diagrams unless other row commands are explicitly shown.

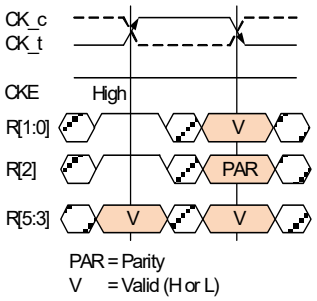


Figure 15. RNOP Command

6.3.2.2. Bank and Row Activation Command (ACT)

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the tRCD specification.

The ACTIVATE command is a 2-cycle command as shown in Figure 16. The actual bank and row activation is initiated with the second clock cycle; therefore all relevant timing parameters refer to this second clock cycle as shown in subsequent timing diagrams.

Parity is evaluated on all R[5:0] inputs separately on both clock cycles of the ACT command when the parity calculation is enabled in the Mode Register.

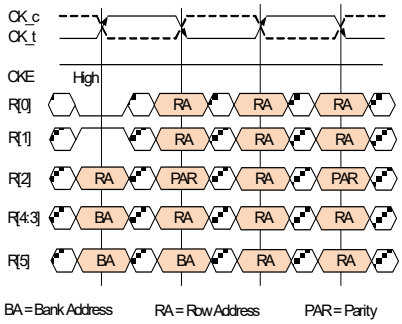


Figure 16. ACTIVATE Command

A subsequent ACTIVATE command to another row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by tRC, as shown in Figure 17. A minimum time tRAS must have elapsed between opening and closing a row.

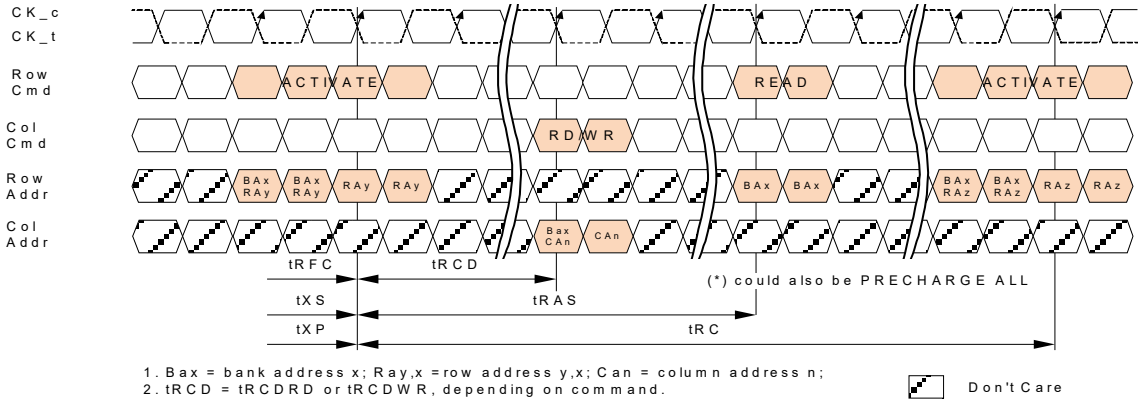


Figure 17. Bank and Row Activation Command Cycle

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by tRRD. The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

6.3.2.2.1. Bank Restrictions

There is a need to limit the number of bank activations in a rolling window to ensure that the instantaneous current supplying capability of the device is not exceeded. To reflect the short term capability of the HBM device's current supply, the parameter tFAW (four activate window) is defined: no more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW (ns) by tCK (ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 25 clocks, and an ACTIVATE command is issued at clock T0, no more than three further ACTIVATE commands may be issued at clocks T1 through T24 as illustrated in Figure 18.

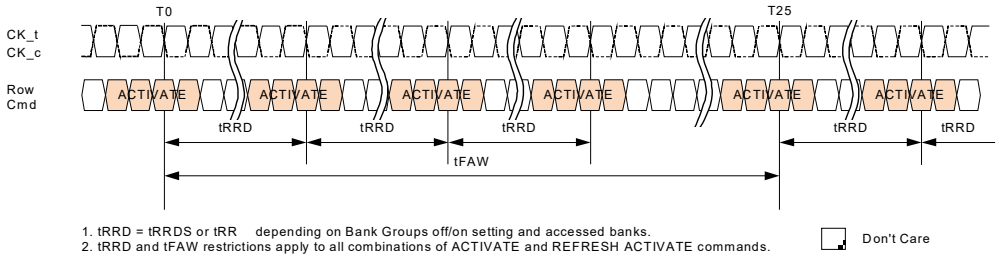
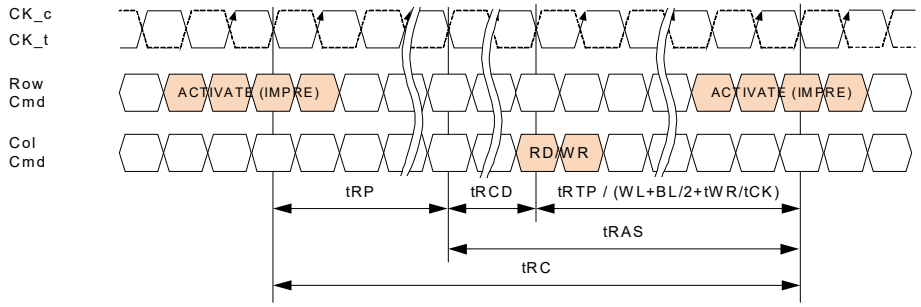


Figure 18. Multiple Bank Activations

6.3.2.3. Bank and Row ACTIVATE Command (ACT) - Implicit Precharge

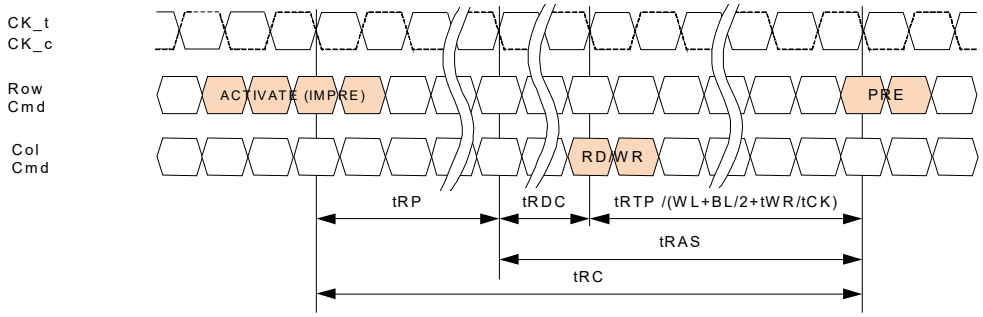
For devices operating in pseudo channel mode, a subsequent ACTIVATE command to another row in the same bank can be issued without closing the previous row. If a row is open and a new row within the bank is activated, the DRAM will internally issue a PRE command (imPRE) after the 2nd clock to precharge the row. After the imPRE command time has elapsed as set by MR6 (see Table 17), the requested ACTIVATE command is issued internally.



1. Two consecutive ACT commands with Implicit Precharge to the same bank are shown.
2. tRP is the number of clock cycles programmed in the Mode Register.
3. tRCD is tRCDRD for Reads and tRCDWR for Writes.

Figure 19. imPRE to imPRE Timing

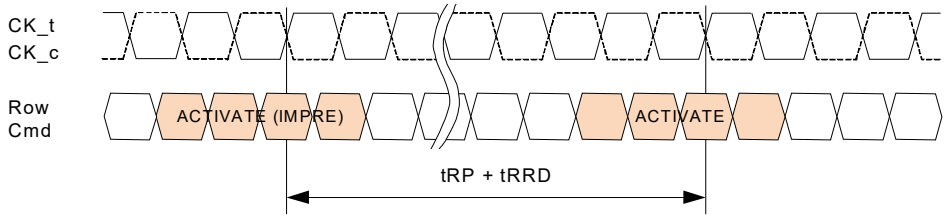
In the case of an imPRE to a row, a READ or WRITE to that row can be issued after $t_{RP} + t_{RCD}$. The minimum time interval between successive ACTIVATE commands to the same bank is defined by t_{RC} as shown in Figure 20. A minimum time t_{RAS} must have elapsed between actual opening and closing a row (closing can be done by either imPRE or external PRE command).



1. An ACT command with Implicit Precharge followed by an explicit PRE command to the same bank are shown.
2. PRE could also be PREALL.
3. tRP is the number of clock cycles programmed in the Mode Register.
4. tRCD is tRCDRD for Reads and tRCDWR for Writes.

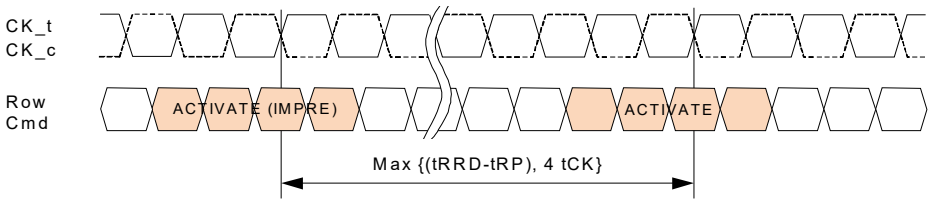
Figure 20. imPRE to EXPLICIT PRE

ACTIVATE to ACTIVATE times to different banks is limited by the tRRD spec. For back to back activates to banks with open rows or back to back activates to banks with no open rows, tRRD applies. For back to back ACTIVATE first to a bank with an open row and then an ACTIVATE to a bank that is idle (closed), the ACTIVATE to ACTIVATE time is tRRD + tRP to allow for the first bank to complete its internal precharge shown in Figure 21. For back to back ACTIVATE first to a bank that is idle (closed) and then an ACTIVATE to a bank that has an open row, the ACTIVATE to ACTIVATE time is MAX{(tRRD - tRP), 4 tCK} shown in Figure 22.



1. An ACT command with Implicit Precharge followed by and ACT command to a different bank are shown.
2. tRP is the number of clock cycles programmed in the Mode Register.

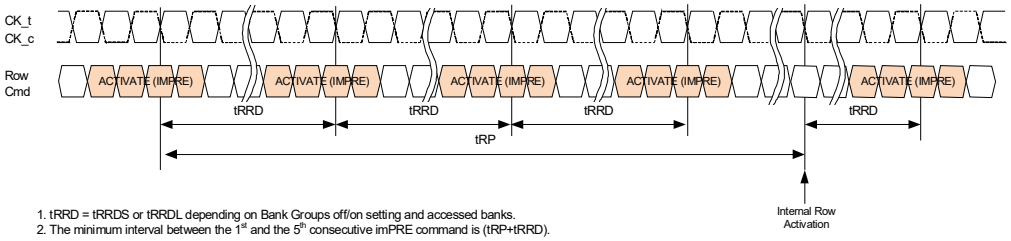
Figure 21. imPRE to ACTIVATE



1. An ACT command followed by an ACT command with Implicit Precharge to a different bank are shown.
2. tRP is the number of clock cycles programmed in the Mode Register.

Figure 22. ACTIVATE to imPRE

There is a limit to the number of concurrent imPRE commands. If an ACTIVATE command triggers an imPRE, a subsequent ACTIVATE command to a different bank with an already open row can be issued within the tRP time of the previous imPRE. Only four concurrent imPRE commands can occur, meaning that the minimum interval between a first and a fifth consecutive imPRE command is given by (tRP + tRRD) as shown in Figure 23.



1. tRRD = tRRDS or tRRDL depending on Bank Groups off/on setting and accessed banks.
2. The minimum interval between the 1st and the 5th consecutive imPRE command is (tRP+tRRD).

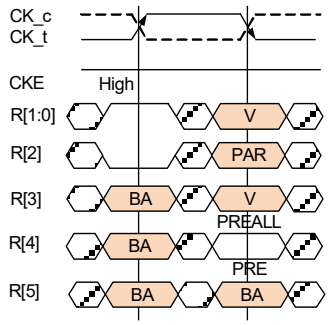
Figure 23. Concurrent Activations with Implicit Precharge

An explicit PRE command can be issued to yet a different bank with one or two on-going imPRE commands. PREALL cannot be issued with ongoing imPRE commands.

6.3.2.4. Precharge Command(PRE/PRE ALL)

The PRECHARGE command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will be in idle state and available for a subsequent row access a specified time t_{RP} after the PRECHARGE command is issued.

Parity is evaluated with the PRECHARGE command when the parity calculation is enabled in the Mode Register.



BA = Bank Address if R4 = Low, otherwise Don't Care
PAR = Parity
V = Valid (H or L)

Figure 24. PRECHARGE Command

Input R4 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, bank addresses BA[3:0] select the bank. Otherwise the bank addresses are treated as “Don’t Care”.

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

6.3.2.4.1. AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit PRECHARGE command. Auto Precharge is nonpersistent meaning that it is enabled or disabled along for each individual READ or WRITE command.

For read bursts an auto precharge of the bank and row that is addressed with the READ command begins t_{RTP} after the READ command was issued or after tRAS has been met, with t_{RAS} as programmed in clock cycles in the RAS field of Mode Register MR3 OP[5:0].

For write bursts an auto precharge of the bank and row that is addressed with the WRITE command begins WL + BL/2 + WR clock cycles after the WRITE command was issued or after t_{RAS} has been met, with WR as programmed in clock cycles in the WR field of MR1 OP[4:0] (Table 10) and t_{RAS} as programmed in clock cycles in the RAS field of MR3 OP[5:0] (Table 12).

Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for READ or WRITE commands. A precharge resulting from a READ or WRITE with Auto Precharge may occur in parallel with an explicit PRECHARGE or PREALL command.

Table 33 - Precharge and Auto Precharge Timings

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Note
READ	PRECHARGE (same bank)	t_{RTP}	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	PREALL	t_{RTP}	nCK	5
	WRITE or WRITE w/ AP (any bank)	t_{RTW}	ns	
	READ or READ w/ AP (any bank)	t_{CCD}	nCK	6
READ w/ AP	PREALL	t_{RTP}	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$t_{RTP} + RU_{(t_{RP}/t_{CK})}$	nCK	2,5
	WRITE or WRITE w/ AP (same bank)	Illegal	nCK	
	WRITE or WRITE w/ AP (different bank)	$RL + BL/2 + t_{RTW}$	nCK	
	READ or READ w/ AP (same bank)	Illegal	nCK	
	READ or READ w/ AP (different bank)	t_{CCDS} or t_{CCDL}	nCK	6
WRITE	PRECHARGE (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	PREALL	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	WRITE or WRITE w/ AP (any bank)	t_{CCD}	nCK	6
	READ w/ AP (same bank)	$WL + BL/2 + MAX[RU(t_{WR}/t_{CK}) t_{RTP}, t_{WTR}]$	nCK	2,5,7,8
	READ (same bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
WRITE w/ AP	PREALL	$WL + BL/2 + WR$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$WL + BL/2 + WR + RU_{(t_{RP}/t_{CK})}$	nCK	2,7
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	t_{CCD}	nCK	6
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
PRECHARGE	PRECHARGE (same bank)	1	nCK	
	PREALL	1	nCK	3
PREALL	PRECHARGE or PREALL	1	nCK	3

NOTE 1 A command issued during the minimum delay time is illegal.
NOTE 2 RU = round up to next integer.
NOTE 3 PREALL is treated as a NOP for a bank when that bank is already idle or in the process of being precharged.
NOTE 4 READ or WRITE and PRECHARGE commands may be issued simultaneously.
NOTE 5 t_{RTP} could either be t_{RTPS} or t_{RTPL}.
NOTE 6 t_{CCD} could either be t_{CCDS} or t_{CCDL}; for READs, t_{CCD} could also be t_{CCDR}.
NOTE 7 WL = write latency. BL = burst length.
NOTE 8 t_{WTR} could either be t_{WTRS} or t_{WTRL}

6.3.2.5. Refresh Command(REF)

The REFRESH command is used during normal operation of the HBM device. The command is received on the row command inputs R[5:0] as shown in Figure 25 and requires a CNOP command on the column command inputs C[7:0].

Parity is evaluated with the REFRESH command when the parity calculation is enabled in the Mode Register.

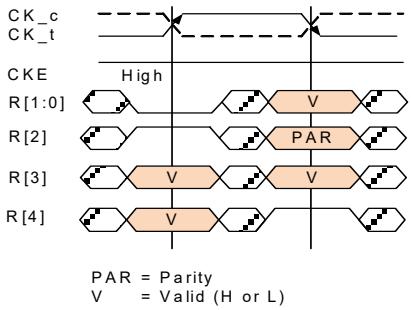
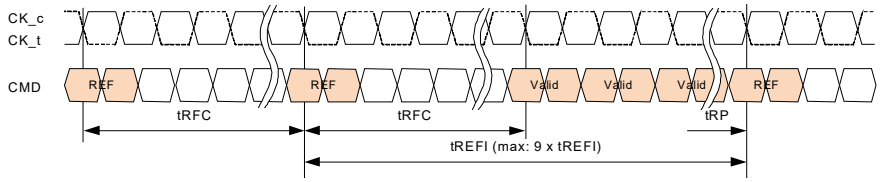


Figure 25. REFRESH Command

The REFRESH command is nonpersistent, so it must be issued each time a refresh is required. A minimum time tRFC is required between two REFRESH commands or a REFRESH command and any subsequent access command after the refresh operation. All banks must be precharged with tRP satisfied prior to the REFRESH command. The banks are in idle state after completion of the REFRESH command.

The refresh addressing is generated by an internal refresh controller. This makes the address bits “Don’t Care” during a REFRESH command.



1. Only RNOP and CNOP commands allowed after REFRESH command registered until tRFC expires.
2. The time interval between two REFRESH commands may be extended to a maximum of 9 x tREFI.

Figure 26. Refresh Cycle

In general, the HBM device requires REFRESH cycles at an average periodic interval of t_{REFI}. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 REFRESH commands can be postponed during operation of the HBM device, meaning that at no point in time more than a total of 8 REFRESH commands are allowed to be postponed. Incase that 8 REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to 9 × t_{REFI} (see Figure 27). A maximum of 8 additional REFRESH commands can be issued in advance (“pulled in”), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than 8 REFRESH commands in advance does not further reduce the number of regular REFRESH commands required later, so that the resulting maximum interval between two surrounding REFRESH commands is limited to 9 × t_{REFI} (see Figure 28). At any given time, a maximum of 16 REFRESH commands can be issued within 2 x t_{REFI}.

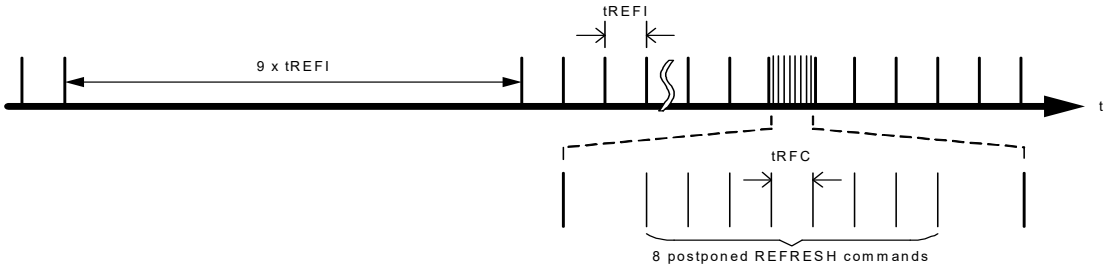


Figure 27. Postponing Refresh Commands (Example)

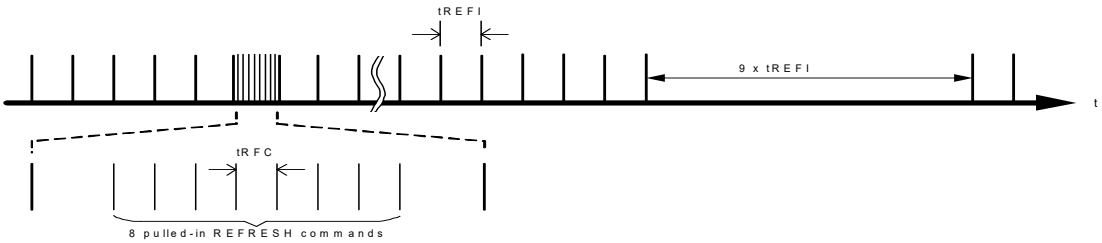


Figure 28. Pulling - In Refresh Commands (Example)

Self-Refresh Mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting Self-Refresh Mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after the Self-Refresh) will never exceed eight. During Self-Refresh Mode, the number of postponed or pulled-in REFRESH commands does not change.

6.3.2.6. Single Bank Refresh Command(REFSB)

The SINGLE BANK REFRESH command provides an alternative solution for the refresh of the HBM device. The command initiates a refresh cycle on a single bank while accesses to other banks including writes and reads are not affected. The command is received on the row command inputs R[5:0] as shown in Figure 29.

Parity is evaluated with the SINGLE BANK REFRESH command when the parity calculation is enabled in the Mode Register.

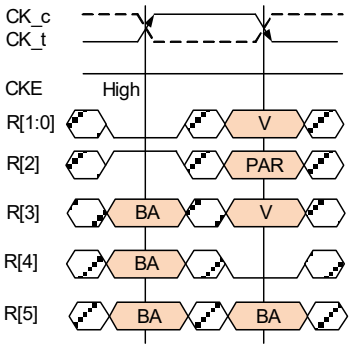


Figure 29. SINGLE BANK REFRESH Command

The SINGLE BANK REFRESH command is nonpersistent, so it must be issued each time a refresh is required.

A minimum time t_{RRD} is required between an ACTIVATE command and a SINGLE BANK REFRESH command to a different bank. A minimum time t_{RREFD} is required between any two SINGLE BANK REFRESH commands (see below for an exception requiring t_{RFCSB}), and between a SINGLE BANK REFRESH command and an ACTIVATE command to a different bank as shown in Figure 30. A minimum time t_{RFCSB} is required between a SINGLE BANK REFRESH command and an access command to the same bank that follows. The selected bank must be precharged with t_{RP} satisfied prior to the SINGLE BANK REFRESH command. The bank is in idle state after completion of the SINGLE BANK REFRESH command.

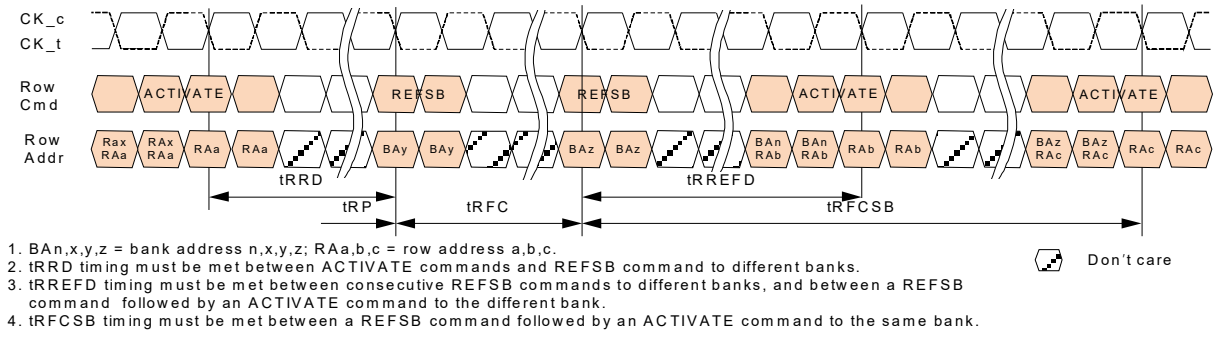


Figure 30. Single Bank Refresh Command Cycle

The row address for each bank is provided by internal refresh counters. This makes the row address bits “Don’t Care” during SINGLE BANK REFRESH commands.

A SINGLE BANK REFRESH command to one of the 8, 16 or 32 (for HBM configurations with SID) banks can be issued in any order. After all 8, 16 or 32 banks have been refreshed using the SINGLE BANK REFRESH command and after waiting for at least t_{RFCSB}, the controller can issue another set of SINGLE BANK REFRESH commands in the same or different order. However, it is illegal to send another SINGLE BANK REFRESH command to a bank unless all 8, 16 or 32 banks have been refreshed using the SINGLE BANK REFRESH command. The controller must track the bank being refreshed by the SINGLE BANK REFRESH command.

The bank count is synchronized between the controller and the HBM device by resetting the bank count to zero. Synchronization can occur upon exit from reset state or by issuing a REFRESH or SELF-REFRESH ENTRY command. Both commands may be issued at any time even if a preceeding sequence of SINGLE BANK REFRESH commands has not completed cycling through all 8 or 16 or 32 banks.

The example in Table 34 (with 16 banks shown as an example) shows two full sets of REFSB commands with the bank counter reset to 0 and the refresh counter incremented after 16 REFSB commands each. The 3rd set of REFSB commands is interrupted by the REFRESH command which resets the bank counter to 0 and performs refreshes to all banks indicated by the refresh counter.

Table 34 - Refresh Counter Increments

Cont	Sub-count	Command	Bank ADDR	Refresh BANK	Bank COUNTER	Refresh Counter
0	0	Reset, REFRESH or SRE command			To 0	
1	1	REFSB	0000	0	0 to 1	n
2	2	REFSB	0001	1	1 to 2	
3	3	REFSB	0010	2	2 to 3	
4	4	REFSB	0011	3	3 to 4	
...		...				
15	15	REFSB	1110	14	14 to 15	
16	16	REFSB	1111	15	15 to 0	
17	1	REFSB	0100	4	0 to 1	n + 1
18	2	REFSB	0111	7	1 to 2	
19	3	REFSB	1011	11	2 to 3	
20	4	REFSB	0110	6	3 to 4	
...		...				
31	15	REFSB	1100	12	14 to 15	
32	16	REFSB	0001	1	15 to 0	
33	1	REFSB	0010	2	0 to 1	n + 2
34	2	REFSB	1001	9	1 to 2	
35	3	REFSB	0000	0	2 to 3	
36	0	REFRESH	V	all	To 0	n + 2
37	1	REFSB	1010	10	0 to 1	n + 3
38	2	REFSB	0101	5	1 to 2	
...						

The average rate of SINGLE BANK REFRESH commands t_{REFISB} depends on the bank count N and can be calculated by the following formula:

$t_{REFISB} = t_{REFI}/N$

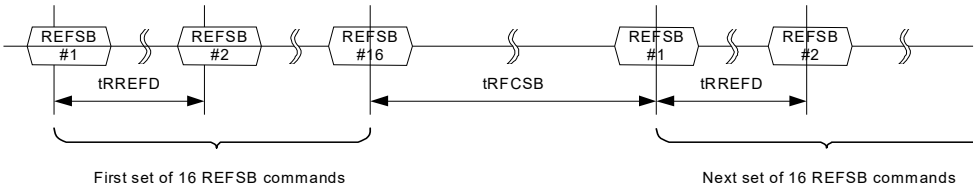


Figure 31. Sets of Single Bank Refresh Commands (16-Bank HBM Devices assumed)

Table 35 - REFRESH and SINGLE BANK REFRESH Command Scheduling Requirements

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Note
REFRESH	REFRESH	t_{RFC}	
	SINGLE BANK REFRESH (any bank)	t_{RFC}	
	ACTIVATE	t_{RFC}	
SINGLE BANK REFRESH	REFRESH	t_{RFCSB}	
	SINGLE BANK REFRESH (different bank)	t_{RREFD}	
	SINGLE BANK REFRESH (any bank)	t_{RFCSB}	3
	ACTIVATE (same bank)	t_{RFCSB}	
	ACTIVATE (different bank with imPRE)	$Max\{(t_{RREFD}-t_{RP}), 4_{tCK}\}$	1
	ACTIVATE (different bank without imPRE)	t_{RREFD}	1
ACTIVATE	REFRESH	t_{RC}	2
	SINGLE BANK REFRESH (same bank)	t_{RC}	2
	SINGLE BANK REFRESH (different bank)	t_{RRD}	1
ACTIVATE with imPRE	REFRESH	$t_{RC} + t_{RP}$	2
	SINGLE BANK REFRESH (same bank)	$t_{RC} + t_{RP}$	2
	SINGLE BANK REFRESH (different bank)	$t_{RRD}+t_{RP}$	1

Note1 : t_{FAW} parameter must be observed as well.

Note2 : A bank must be in the idle state with tRP satisfied before it is refreshed.

Note3 : t_{RFCSB} parameter must be observed when the first REFSB command completes a set of 8, 16 or 32 single bank refresh operations and the second REFSB command initiates the next set of 8, 16 or 32 single bank refresh operations

6.3.3. Column Commands

The column commands consist of NOP, Read, Read with Auto Precharge, Write, Write with Auto Precharge, and MRS. The Column commands utilize C[7:0] inputs. Unlike some row commands, all column commands are transmitted in a single clock cycle.

6.3.3.1. Column No Operation Command (CNOP)

The COLUMN NO OPERATION (CNOP) command as shown in Figure 32 is used to instruct the HBM device to perform a NOP as column command; this prevents unwanted column commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated on all C[7:0] inputs when the parity calculation is enabled in the MR0.

CNOP is assumed on subsequent timing diagrams unless other column commands are explicitly shown.

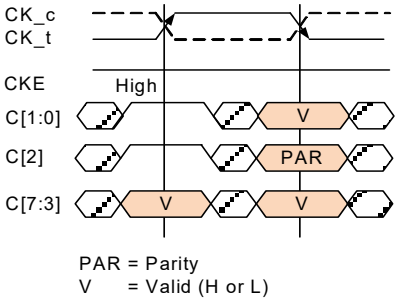


Figure 32. CNOP Command

6.3.3.2. Read Command (RD,RDA)

A read burst is initiated with a READ command as shown in Figure 33. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the READ command when the parity calculation is enabled in the Mode Register.

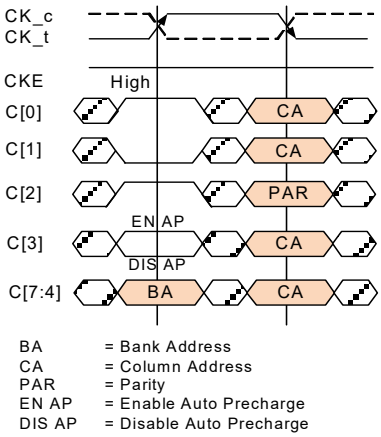


Figure 33. READ Command

The length of the burst initiated with a READ command is either two or four, depending on the burst length programmed in the BL field of MR3 OP[7] (See Table 12). The column address is unique for this burst of two or four. There is no interruption nor truncation of read bursts.

The read latency (RL) is defined from the rising CK_t edge on which the READ command is issued to the rising CK_t edge from which the tDQSCK delay is measured measured, with the number of clock cycles as programmed in the RL field of MR2 OP[7:3](See Table 11). The first valid data is available RL × t_{CK} + t_{DQSCK} + t_{DQSQ} after the rising CK_t edge when the READ command was issued.

The output drivers are enabled nominally two clock cycles (odd bytes) and one clock cycle (even bytes) prior to the first valid data bit; they will drive Hi-Z nominally one half clock cycle after the completion of the burst provided no other READ command has been issued.

The read data strobe provides a fixed one-cycle preamble and fixed one-cycle postamble; the first RDQS edge occurs (RL-1) × t_{CK} + t_{DQSCK} after the rising CK_t edge when the READ command was issued. The first data bit of the read burst is synchronized with the second rising edge of the RDQS_t strobe. Each subsequent dataout is edge-aligned with the data strobe. Pin timings for the data strobe are measured relative to the crosspoint of RDQS_t and its complement, RDQS_c.

6.3.3.2.1. Clock to Read Data Strobe Timings

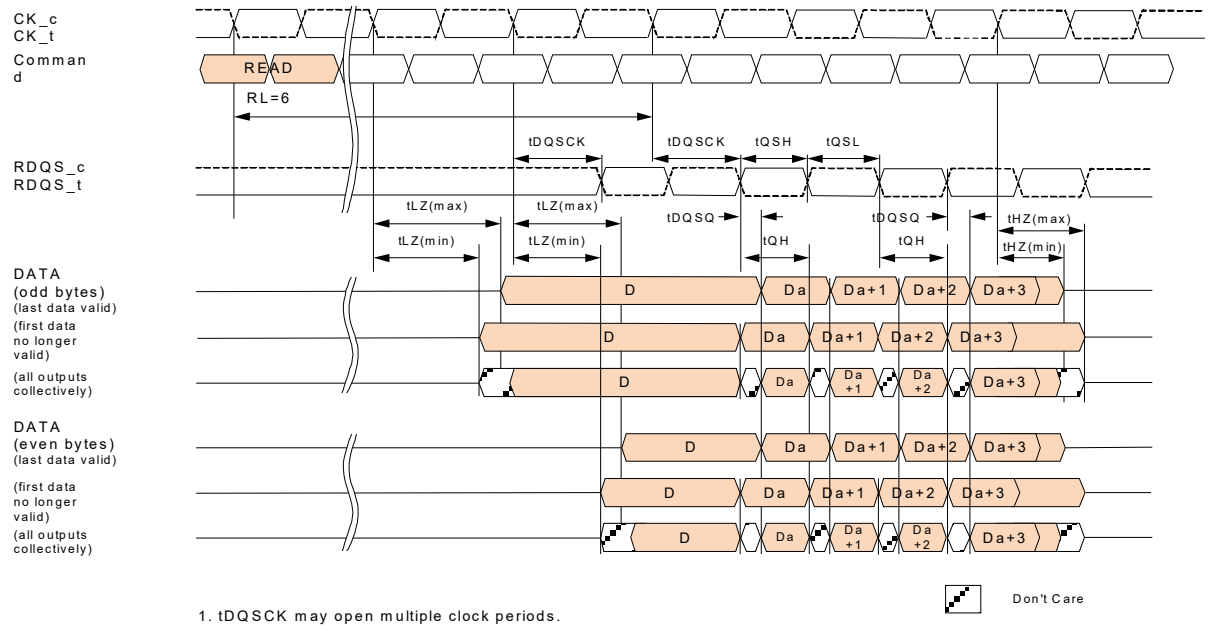
The clock to read data strobe (RDQS) relationship is shown in Figure 34. Related parameters:

- t_{DQSCK}(min/max) describes the allowed range for a rising or falling RDQS edge relative to CK_t, CK_c.
- t_{DQSCK} is the actual position of a RDQS edge relative to CK_t,CK_c.
- t_{QSH} describes the RDQS HIGH pulse width.
- t_{QSL} describes the RDQS LOW pulse width.
- t_{LZ}(min/max) describe the allowed range for the data output HIGH-Z to low impedance transition relative to CK_t, CK_c.
- t_{HZ}(min/max) describe the allowed range for the data output low impedance to HIGH-Z transition relative to CK_t, CK_c.

6.3.3.2.2. Read Data Strobe and Data Out Timings

The read data strobe (RDQS) to data out (DQ, DMI) relationship is shown in Figure 34. Related parameters:

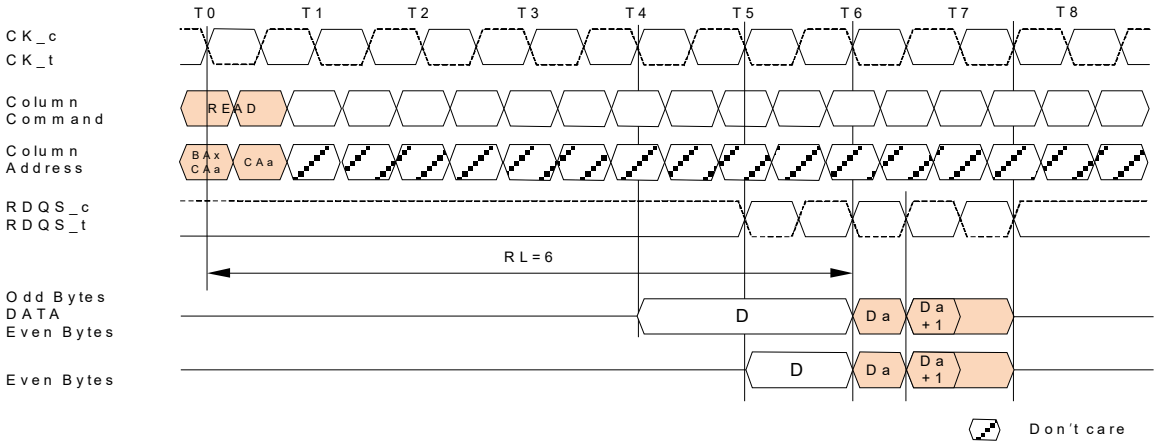
- t_{DQSQ} describes the latest valid transition of any associated DQ or DMI pin for both rising and falling RDQS edges.
- t_{QH} describes the earliest invalid transition of any associated DQ or DMI pin for both rising and falling RDQS edges.



1. tDQSCK may open multiple clock periods.
2. A burst length of 4 is shown.
3. Early/late data transition of a DQ or DM or DBI can vary within a burst.

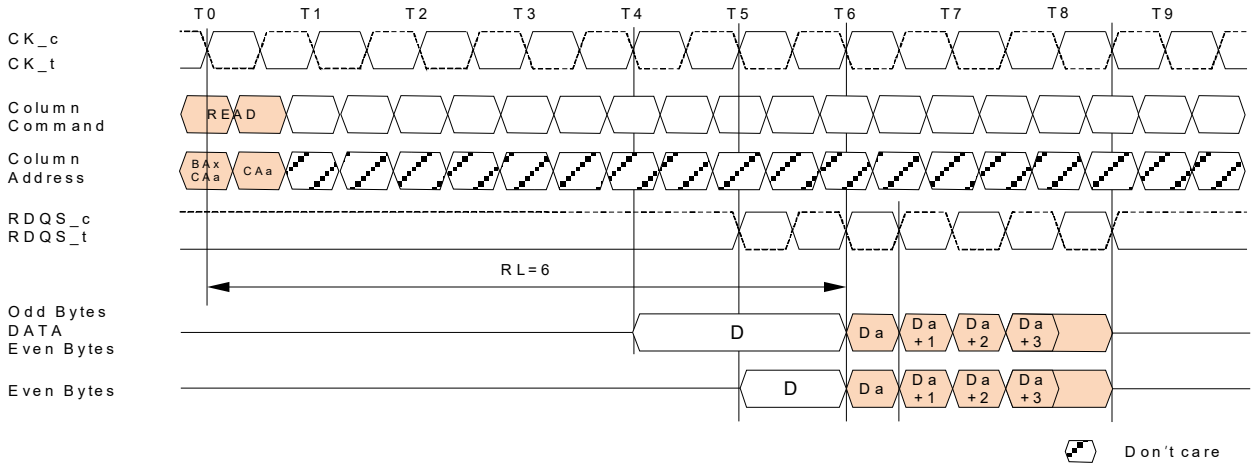
Figure 34. Clock to RDQS and Data Out Timings

Single read bursts are shown in Figure 35 for BL=2 and Figure 36 for BL=4.



1. BAx = bank address x' CAa =column address a.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da,a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK, tLZ, tHZ = 0 is shown for illustration purpose.

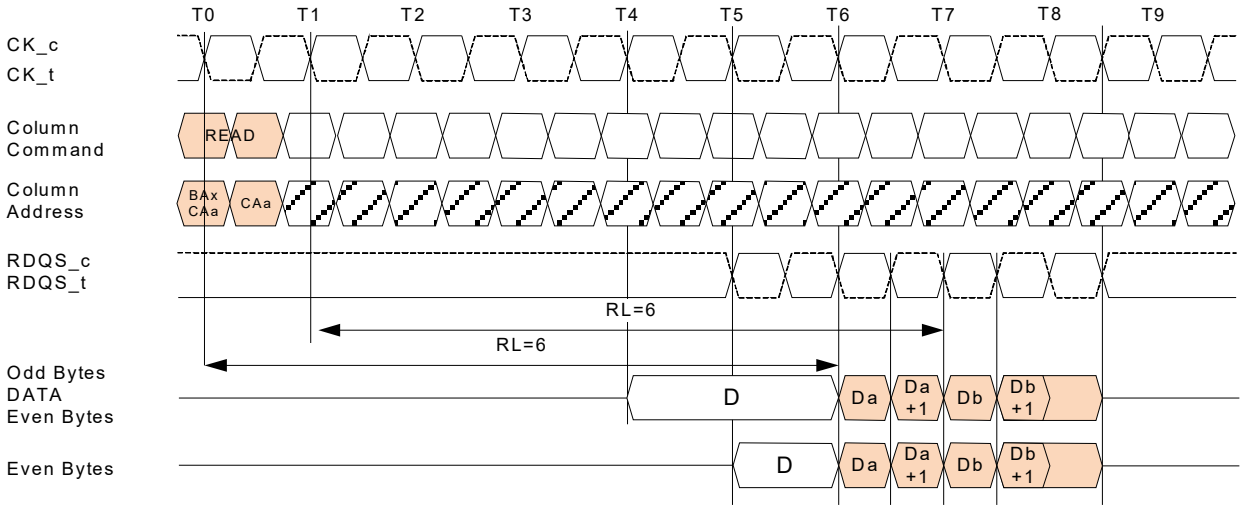
Figure 35. Single Read Burst with BL=2



1. BAx = bank address x' CAa =column address a.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da,a+1,a+2,a+3 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK, tLZ, tHZ = 0 is shown for illustration purpose.

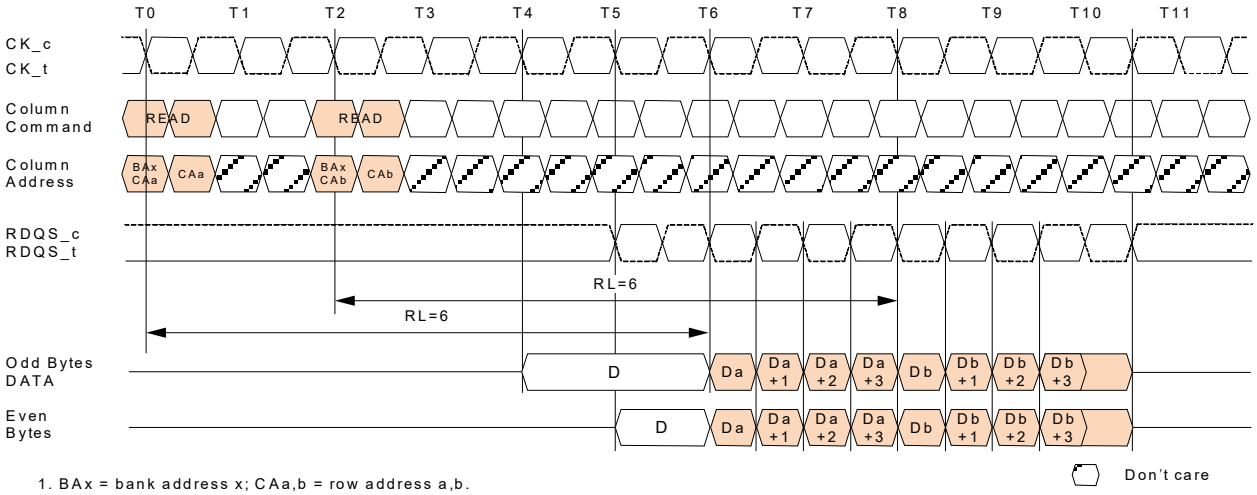
Figure 36. Single Read Burst with BL=4

Data from any read burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained as shown in Figure 37 for BL=2 and Figure 38 for BL=4. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t_{CCD} timing and the programmed burst length (BL). If that READ command is to another idle bank then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met.



1. BAx = bank address x' CAa =column address a,b.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da,Da+1,Db, Db+1 = data-out for READ command a,b.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK, tLZ, tHZ = 0 is shown for illustration purpose.

Figure 37. Seamless Read Bursts with BL=2

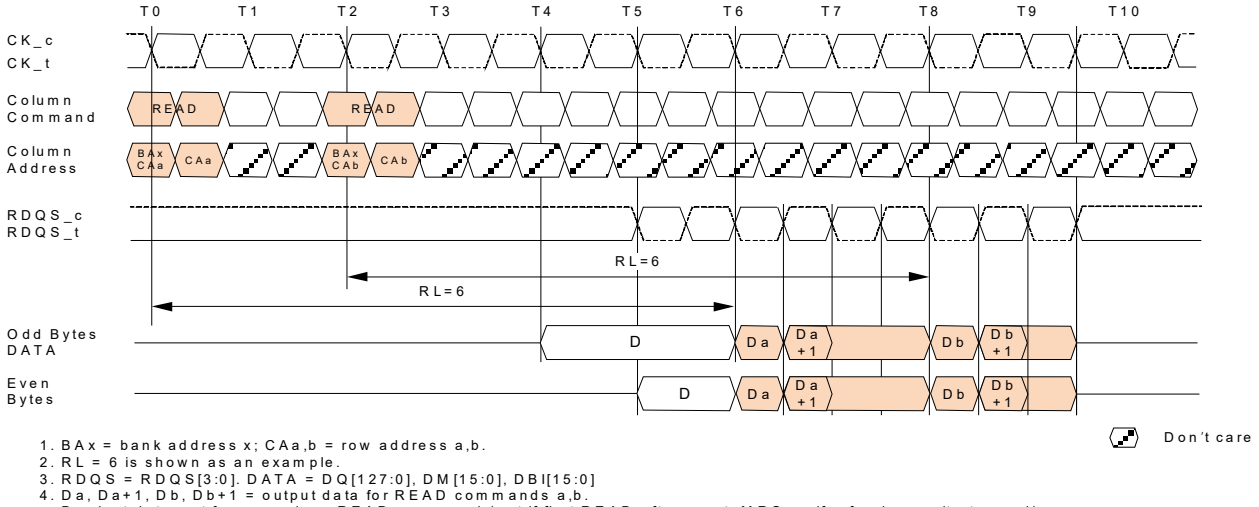


1. BAx = bank address x; CAa,b = row address a,b.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]. DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1 … DA+3, Db, Db+1 … Db+3 = output data for READ commands a,b.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read.
5. iDQSCK, tLZ, tHZ = 0 is shown for illustration purposes.

Figure 38. Seamless Read Bursts with BL=4

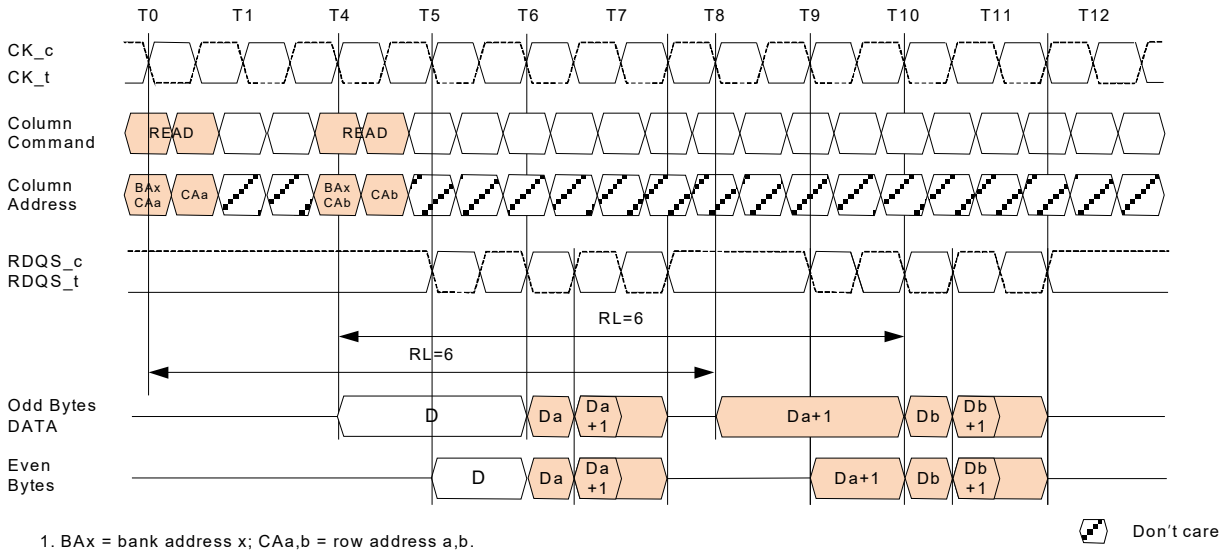
Examples of non-seamless read bursts with BL=2 are shown in Figure 39 for t_{CCD}=2 and Figure 40 for t_{CCD}=4. The RDQS cycle at clock edge T7 in Figure 39 represents the read postamble of the first read burst as well as the read preamble of the second read burst. The chosen t_{CCD} value leads to a continuous series of RDQS pulses over both read bursts, and the data bus does not return to HIGH-Z between the read bursts.

With tCCD=4 as shown in Figure 40 the timing of each of the two read bursts is identical to a single read burst as shown in Figure 35. The data bus returns to HIGH-Z between the read bursts, and the last data out of the first read burst (Da+1) is re-driven at clock edge T8 (for odd bytes) and T9 (for even bytes) preceding the second read burst.



1. BAx = bank address x; CAa,b = row address a,b.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]. DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1, Db, Db+1 = output data for READ commands a,b.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. iDQSCK, tLZ, tHZ = 0 is shown for illustration purposes.

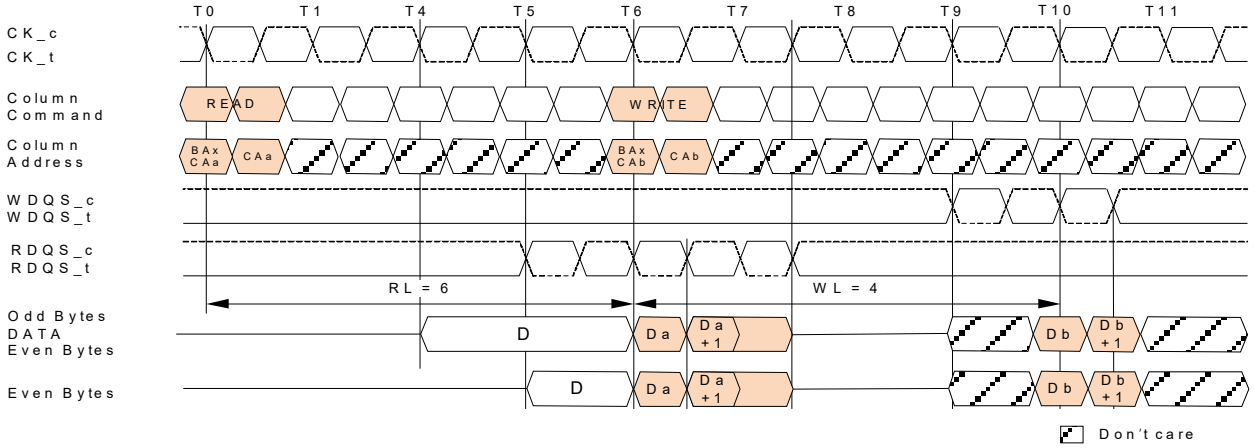
Figure 39. Non-Seamless read Bursts with tCCD=2 and BL=2



1. BAx = bank address x; CAa,b = row address a,b.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]. DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1, Db, Db+1 = output data for READ commands a,b.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. iDQSCK, tLZ, tHZ = 0 is shown for illustration purposes.

Figure 40. Non-Seamless Read Bursts with tCCD=4 and BL=2

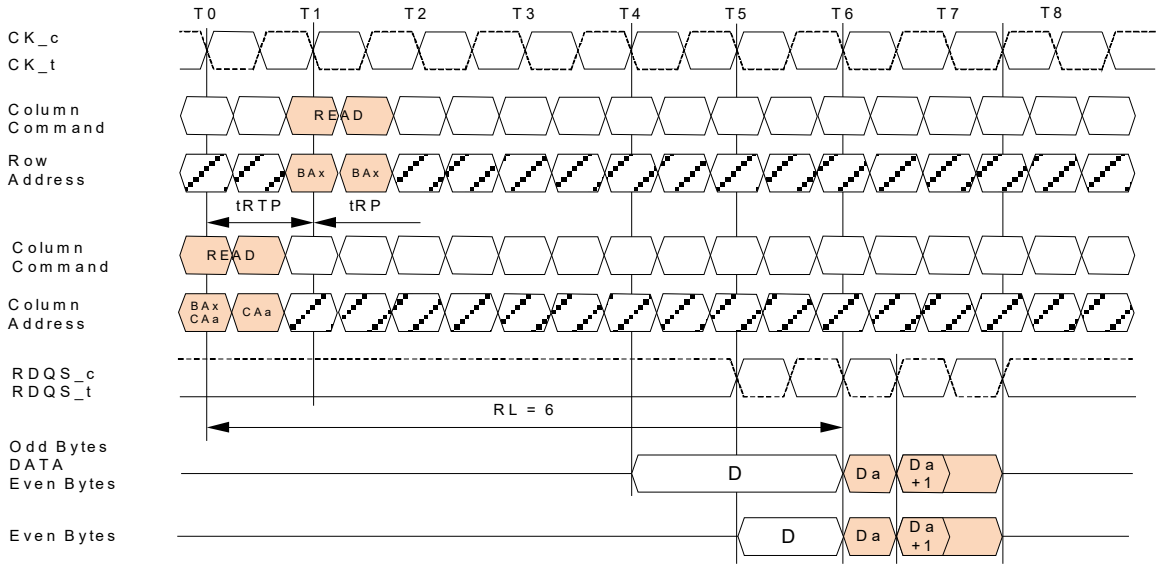
A WRITE can be issued any time after a READ command as long as the bus turn around time t_{RTW} is met as shown in Figure 41 for BL=2. If that WRITE command is to another idle bank, then an ACTIVATE command must precede the WRITE command and t_{RCDWR} also must be met.



1. BAx = bank address x' CAa = column address a.
2. RL = 6 and WL = 4 are shown as examples.
3. RDQS = RDQS[3:0]; WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or wirte-to-read).
5. Db,b+1 = data0in for WRITE command b.
6. tDQSCK, tLZ, tHZ, tDQSS = 0 is shown for illustration purposes.
7. tRTW is not a device limit but determined by the system bus turnaround time.
8. DBI(ac) could be on or off.

Figure 41. Read to Write

A PRECHARGE can be issued t_{RTP} after the READ command as shown in Figure 42 for BL=2. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until t_{RP} is met.



1. BAx = bank address x' CAa = column address a.
2. RL = 6 and WL = 4 are shown as examples.
3. RDQS = RDQS[3:0]; WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK, tLZ, tHZ = 0 is shown for illustration purposes.
6. tRTP = tRTPL when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise tRTP ? tRTPS.

Figure 42. Read to Precharge

6.3.3.3. Write Command (WR, WRA)

A Write burst is initiated with a WRITE command as shown in Figure 43. The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the WRITE command when the parity calculation is enabled in the MR0 (Table 9)

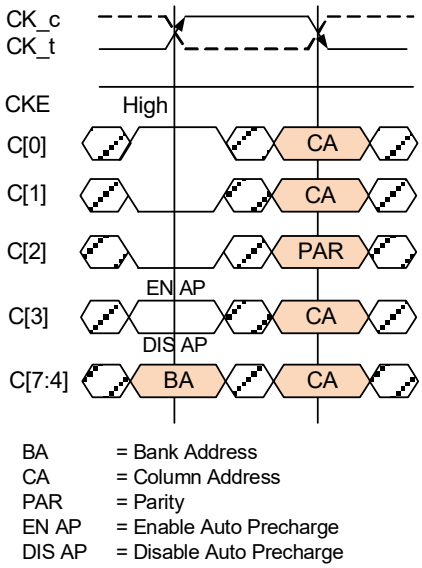


Figure 43. WRITE Command

The length of the burst initiated with a WRITE command is either two or four, depending on the burst length programmed in the BL field of MR3 OP[7]. The column address is unique for this burst of two or four. There is no interruption nor truncation of Write bursts.

The write latency (WL) is defined from the rising CK_t edge on which the WRITE command is issued to the rising CK_t edge from which the t_{DQSS} delay is measured, with the number of clock cycles as programmed in the WL field of MR2 OP[2:0]. The first valid data must be driven WL × t_{CK} + t_{DQSS} after the rising CK_t edge when the WRITE command was issued.

The write data strobe provides a fixed one-cycle preamble and no postamble; the first WDQS edge must be driven (WL-1) × t_{CK} + t_{DQSS} after the rising CK_t edge when the WRITE command was issued. The first data-in of the write burst must be driven center-aligned with the second rising edge of the WDQS_t strobe. Each subsequent data-in must be applied center-aligned with the data strobe edges. Pin timings for the data strobe are measured relative to the crosspoint of WDQS_t and its complement, WDQS_c.

6.3.3.3.1. Clock to Write Data Strobe Timings

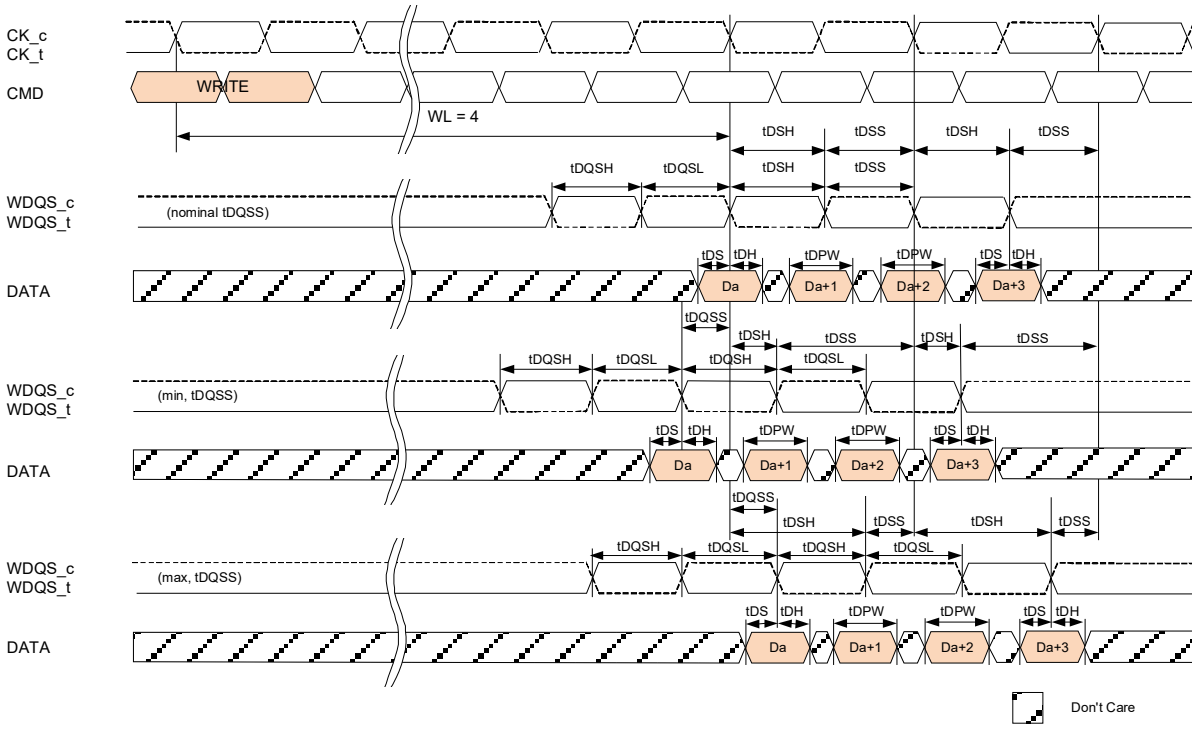
The clock to write data strobe (WDQS) relationship is shown in Figure 44. Related parameters:

- t_{DQSS} (min/max) describes the allowed range for a rising or falling WDQS edge relative to CK_t, CK_c.
- t_{DQSS} is the actual position of a WDQS edge relative to CK_t, CK_c.
- t_{DQSH} describes the WDQS HIGH pulse width.
- t_{DQSL} describes the WDQS LOW pulse width.
- t_{DSS} describes falling WDQS edge to rising clock edge setup time.
- t_{DSH} describes falling WDQS edge from rising clock edge hold time.

6.3.3.3.2. Write Data Strobe and Data In Timings

The write data strobe (WDQS) to data in relationship is shown in Figure 44. Related parameters:

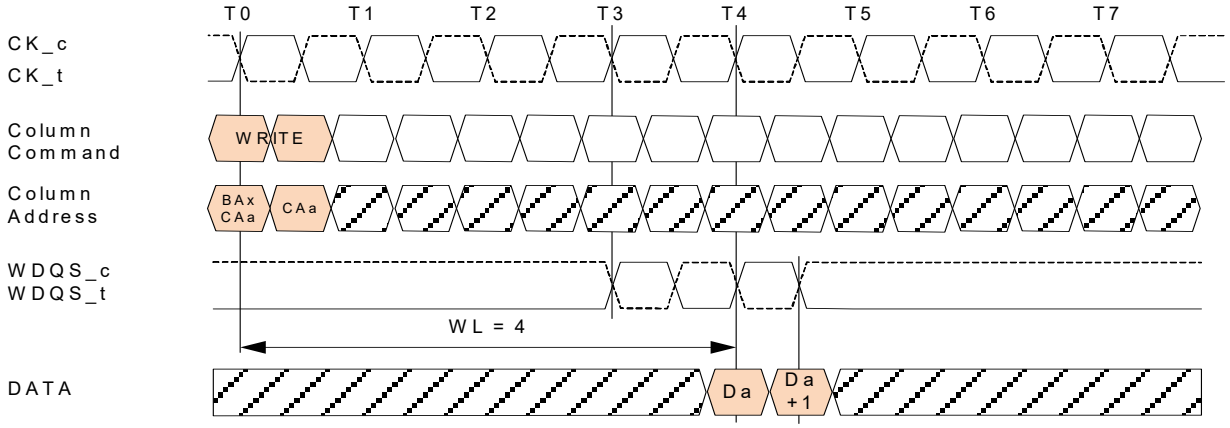
- t_{DS} describes the required setup time of any associated input data pin for both rising and falling WDQS edges.
- t_{DH} describes the required hold time of any associated input data pin for both rising and falling WDQS edges.



1. A burst length of 4 is shown.
2. tDS, tDH, tDPW apply to each input individually.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]

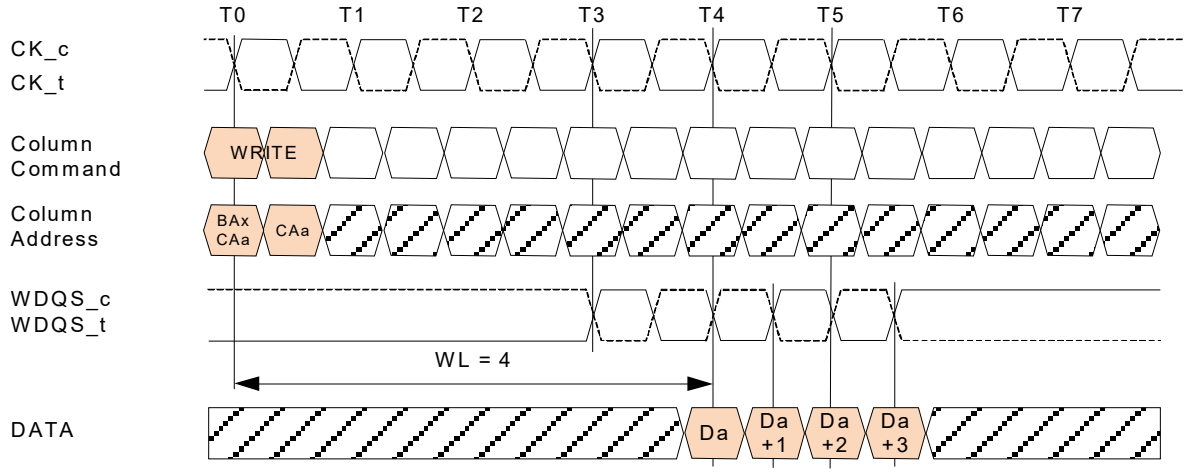
Figure 44. Clock to WDQS and Data input Timings

Single write bursts are shown in Figure 45 for BL=2 and Figure 46 for BL=4



1. BAx = bank address x' CAa =column address a.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.

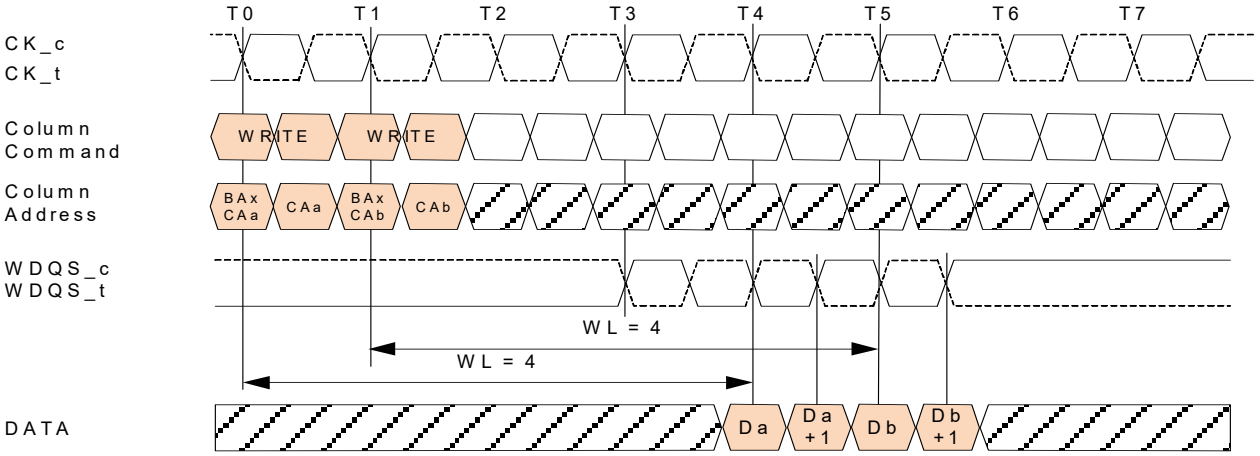
Figure 45. Single Write Burst with BL=2



1. BAx = bank address x' CAa =column address a.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1, Da+2, DA+3 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.

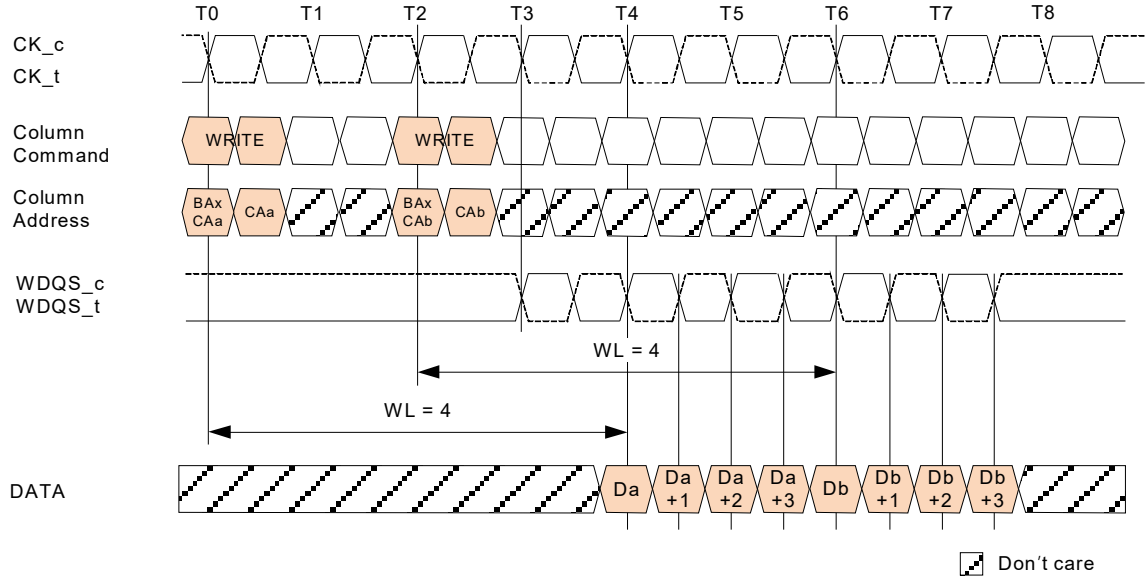
Figure 46. Single Write Burst with BL=4

Data from any write burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained as shown in Figure 47 for BL=2 and Figure 48 for BL=4. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the t_{CCD} timing and the programmed burst length (BL). If that WRITE command is to another idle bank then an ACTIVE command must precede the WRITE command and t_{RCDWR} also must be met.



1. BAx = bank address x' CAa =column address a.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1, Db, Db+1 = data-in for WRITE command a,b.
5. tDQSS = 0 is shown for illustration purposes.

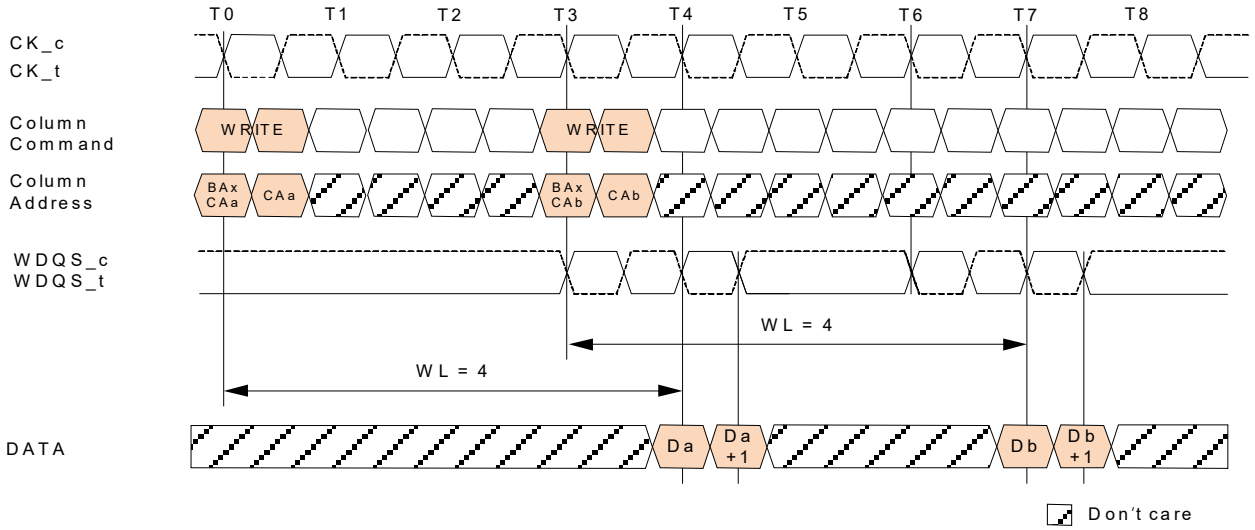
Figure 47. Seamless Write Bursts with BL=2



1. BAx = bank address x' CAa =column address a.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0], DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1 ... Da+3, Db, Db+1 ... Db+3 = data-in for WRITE command a,b.
5. tDQSS = 0 is shown for illustration purposes.

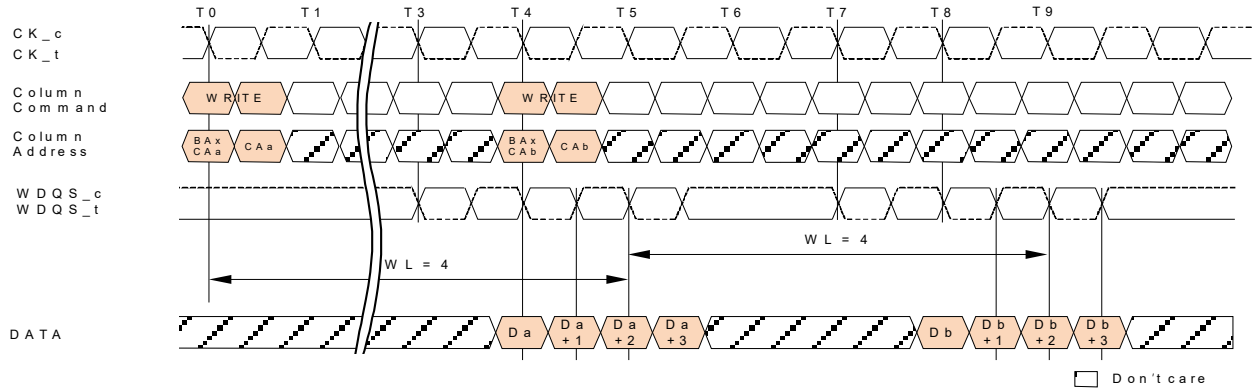
Figure 48. Seamless Write Bursts with BL=4

Examples of non-seamless write bursts are shown in Figure 49 for BL=2 and Figure 50 for BL=4



1. BAx = bank address x' CAa =column address a.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0], DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1, Db, Db+1 … Db+3 = data-in for WRITE command a,b.
5. tDQSS = 0 is shown for illustration purposes.

Figure 49. Non-Seamless Write Bursts with BL=2



1. BAx = bank address x; CAab =column address a,b.
2. WL = 4 are shown as examples.
3. WDQS = WDQS[3:0], DATA = DQ[127:0], DM[15:0], DBI[15:0]
4. Da, Da+1..Da+3, Db, Db+1 … Db+3 = data-in for WRITE command a,b.
5. tDQSS = 0 is shown for illustration purposes.

Figure 50. Non-Seamless Write Bursts with BL=4

A READ can be issued any time after a WRITE command as long as the bus turn around time t_{WTR} is met as shown in Figure 51 for BL=2. If that READ command is to another idle bank, then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met. The bus is preconditioned for the first read burst by being driven LOW two clock cycles (even bytes) and one clock cycle (odd bytes) prior to the first valid data element of the read burst when RDBI is enabled in MR0 OP[0].

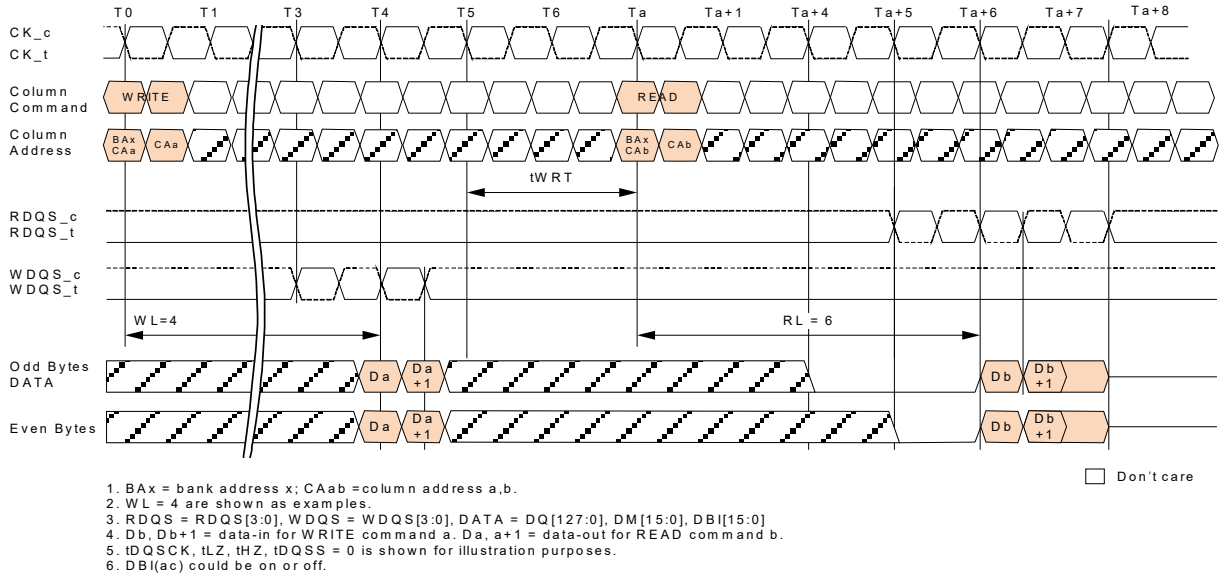


Figure 51. Write to Read

The write recovery time t_{WR} must have elapsed before a PRECHARGE command can be issued to that bank as shown in Figure 52 for BL=2; the t_{WR} interval begins with the completion of the write burst at WL + BL/2 clock cycles after the WRITE command was issued. Also, t_{RAS} must be met when the PRECHARGE is issued. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until tRP is met.

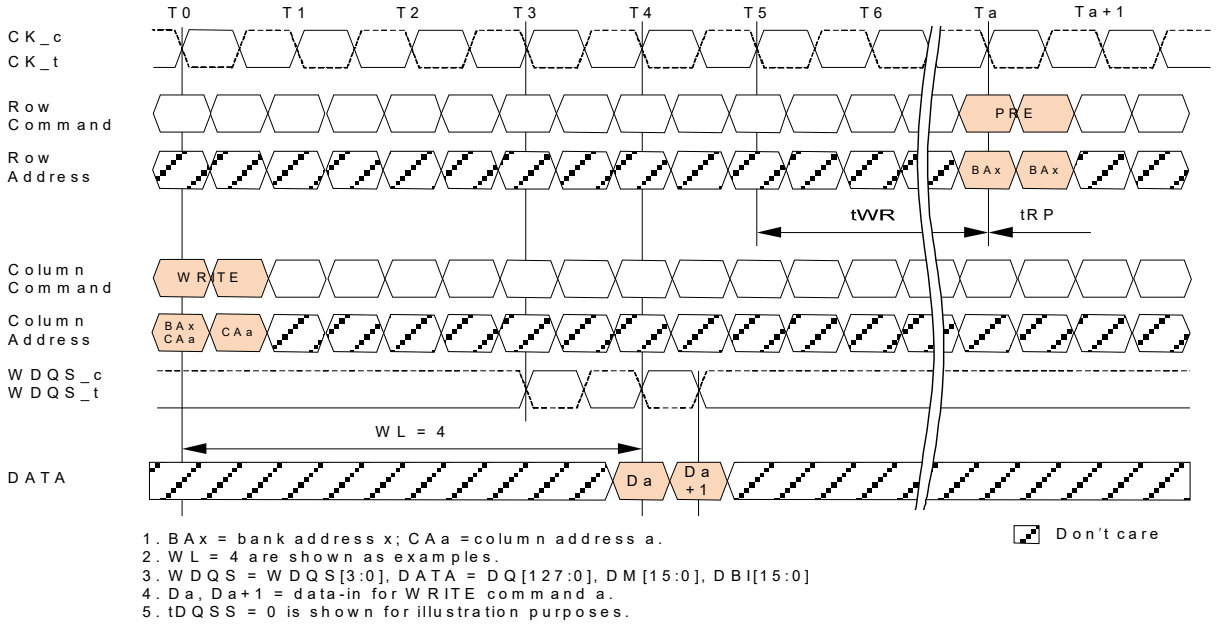


Figure 52. Write to Precharge

6.3.3.4. Mode Register Set (MRS)

The MODE REGISTER SET (MRS) command is used to load the Mode Registers of the HBM device. The command is received on the column command inputs C[7:0] as shown in Figure 53 and requires a RNOP command on the row command inputs R[5:0]

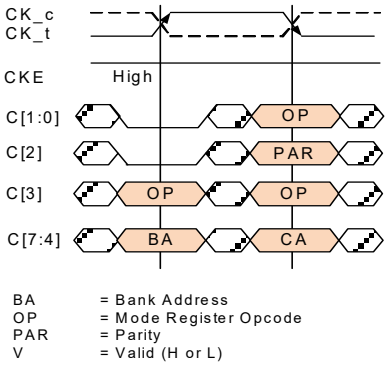


Figure 53. MODE REGISTER SET Command

Inputs BA[3:0] select the Mode Register, and the inputs OP[7:0] determine the op-code to be loaded. See HBM Mode Register Overview (Table 8) for Mode Register definitions.

The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress. The MODE REGISTER SET command cycle time tMRD is required to complete the write operation to the Mode Register and is the minimum time required between two MRS commands. The MRS command to Non-MRS command delay, t_{MOD}, is required by the HBM device to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding RNOP and CNOP.

Parity is evaluated on all R[5:0] and C[7:0] inputs when the parity calculation has already been enabled in the

Mode Register prior to this MODE REGISTER SET command. When parity calculation is enabled by a MODE REGISTER SET command, the HBM requires all subsequent commands including RNOP and CNOP to be issued with correct parity until t_{MOD} has expired for the MODE REGISTER SET command that disables the parity calculation.

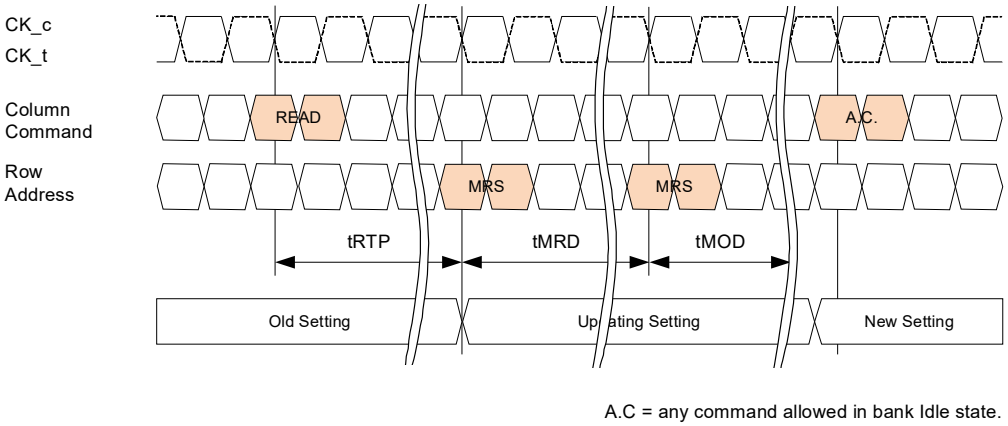


Figure 54. Mode Register Set Timings

6.3.4. Power-Mode Commands

6.3.4.1. Power-Down (PDE,PDX)

HBM devices require CKE to be HIGH at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For Reads, a burst completion is defined as when the last data element has been transmitted on the data outputs; for Writes, a burst completion is defined as when the last data element has been written to the memory array with t_{WR} satisfied.

Power-Down is entered when CKE is registered LOW along with RNOP and CNOP commands as shown in Figure 55.

CKE must not go LOW when read or write operations are in progress. A read operation is completed when the last data element including parity (when enabled) and RDQS postamble has been transmitted on the outputs. A write operation is completed when the last data element including parity (when enabled) has been written to the memory array with t_{WR} satisfied; for Writes with auto-precharge, the number of clock cycles programmed in the Mode Register for WR must have elapsed instead.

CKE can go LOW while any other operations such as row activation, precharge, auto precharge, or refresh are in progress, but the power-down IDD specification will not apply until such operations are complete.

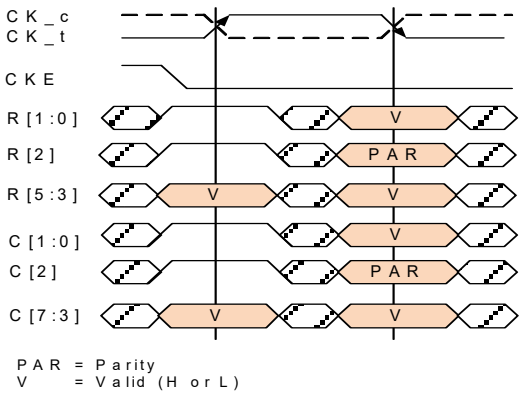


Figure 55. POWER-DOWN ENTRY Command

If Power-Down occurs when all banks are idle, this mode is referred to as Precharge Power-Down; if Power-Down occurs when there is a row active in any bank, this mode is referred to as Active Power-Down. Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, RESET_n and CKE. To ensure that there is enough time to account for the internal delay on the CKE signal path, RNOP and CNOP commands are required for t_{CPDED} period after power-down entry.

While in power-down, CKE LOW must be maintained at the device inputs. The clock may be stopped or the clock frequency may be changed under the following conditions:

- The clock is held stable for t_{CKSRE} cycles and, in case of a preceding ACTIVATE, REFRESH or SINGLE BANK REFRESH command, until the number of clock cycles programmed in the Mode Register for RAS have elapsed;
- In case of clock stop CK_t is held LOW and CK_c is held HIGH;
- In case of a clock frequency change t_{CK}(min) is met for each clock cycle

•The clock is stable with t_{CH}(min) and t_{CL}(min) satisfied at least t_{CKSRX} cycles prior to power-down exit.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is limited by the refresh requirements of the device.

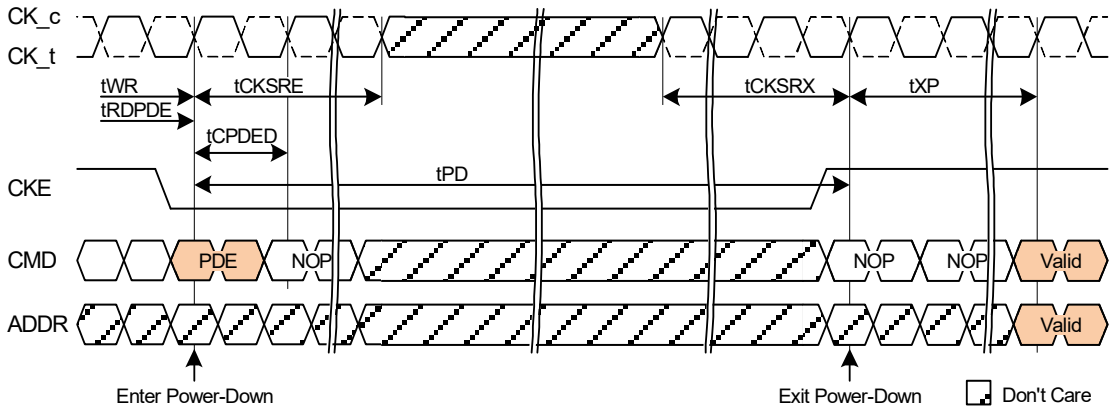
While in power-down the device will maintain the internal DBI state for the DBI(ac) calculation when DBI is enabled in the Mode Register. It will also continue driving RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and TEMP and CATTRIP to valid HIGH or LOW levels.

Power-down is synchronously exited when CKE is registered HIGH (in conjunction with RNOP and CNOP commands). A valid executable command may be applied t_{XP} cycles later. The minimum power-down duration is specified by t_{PD}.

If enabled, parity is evaluated for the POWER-DOWN ENTRY command. The HBM device requires RNOP and CNOP commands with valid parity for the entire t_{CPDED} period, while it will suspend parity checking after power-down entry and drive AERR and DERR to a static LOW.

Parity is not evaluated for the POWER-DOWN EXIT command. The HBM device requires RNOP and CNOP commands with valid parity for the entire t_{XP} period, while within t_{XP} period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time

Power-Down is entered when CKE is registered LOW along with RNOP and CNOP commands as shown in Figure 56. RNOP and CNOP commands are required for t_{CPDED} period after power-down entry.



1. Only RNOP and CNOP commands allowed during tCPDED and tXP periods.
2. Write bursts must have been completed with tWR satisfied prior to power-down entry.
3. Read bursts must have been completed with tRDPDE satisfied prior to power-down entry.
4. Address inputs are "Don't Care" for power-down entry and exit, however the inputs are evaluated for parity during tCPDED and tXP periods when the parity calculation is enabled in the Mode Register.
5. Parity check is not guaranteed and AERR may not be set correctly during tCPDEC and tXP periods. AERR is shown with tPARAC=0 for illustration purpose.

Figure 56. Power-Down Entry and Exit

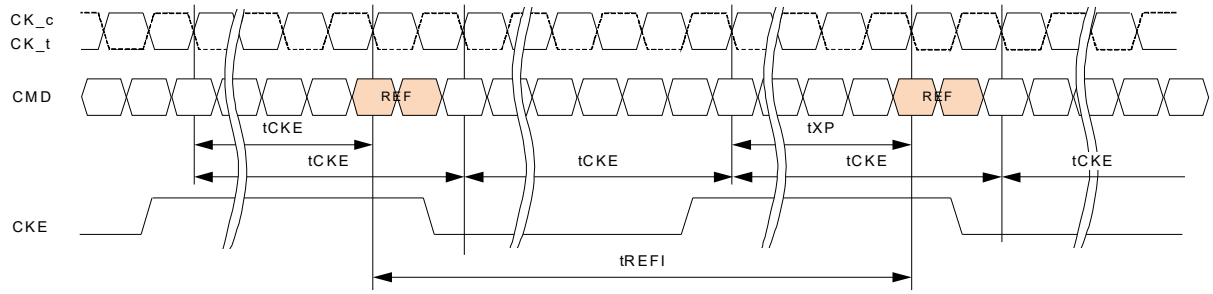


Figure 57. CKE Intensive Environment

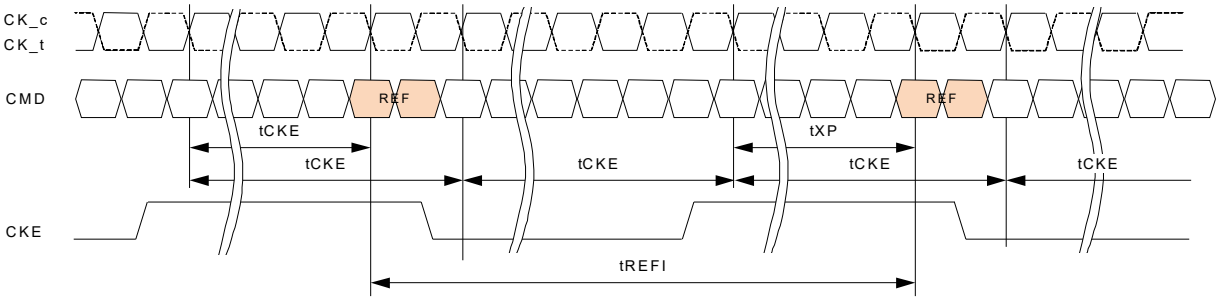
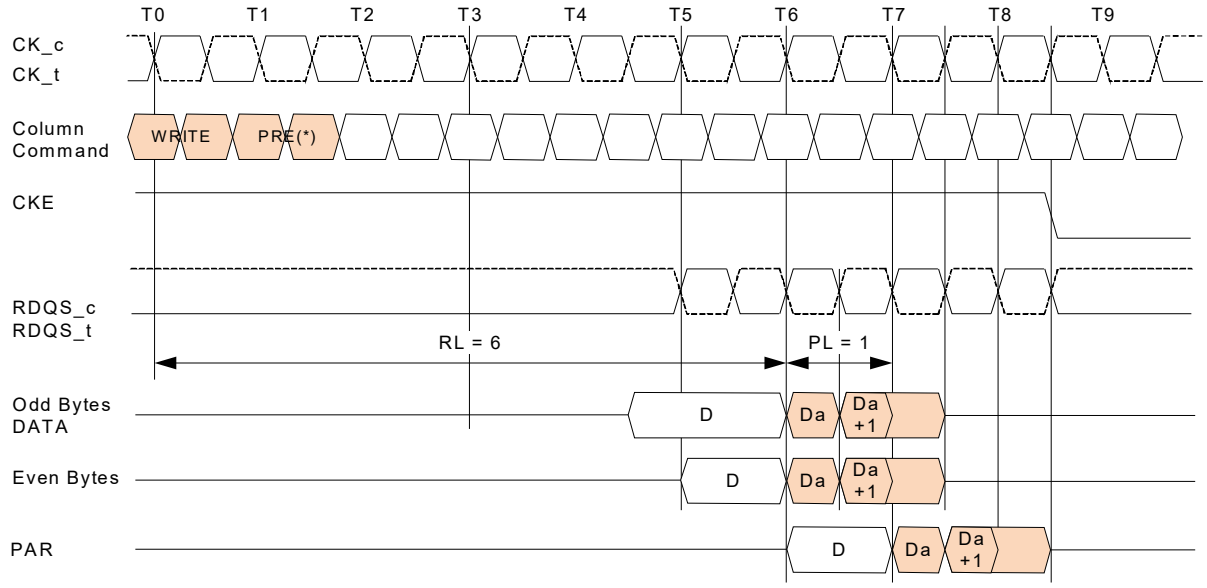
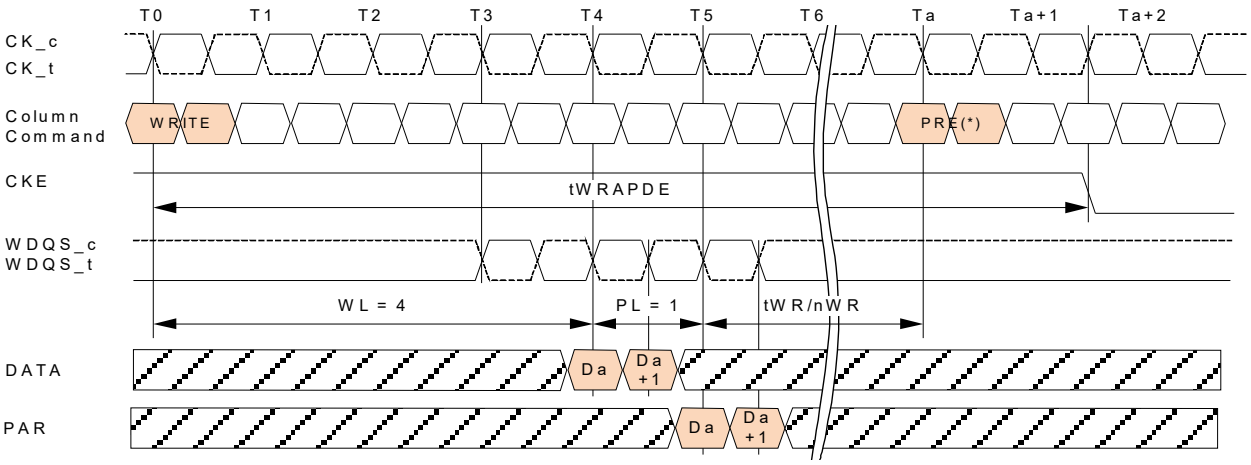


Figure 58. REFRESH to REFRESH Timing in CKE Intensive Environments



1. PRE indicates the internal auto-precharge for RDQ commands.
2. BL = 2, RL = 6 and PL = 1 are shown as examples.
3. CKE must be held high until the end of the read burst operation.

Figure 59. READ or READ with Auto Precharge to Power-Down Entry Timing



1. PRE indicates the internal auto-precharge for WRA commands.
2. BL = 2, WL = 4 and PL = 1 are shown as examples.
3. CKE must be held high until the end of the write burst operation.
4. tWR is the analog value used with WR commands
5. nWR is the number of clock cycles programmed for WR in the Mode Register and used with WRA commands.

Figure 60. WRITE or WRITE with Auto Precharge to Power-Down Entry Timing

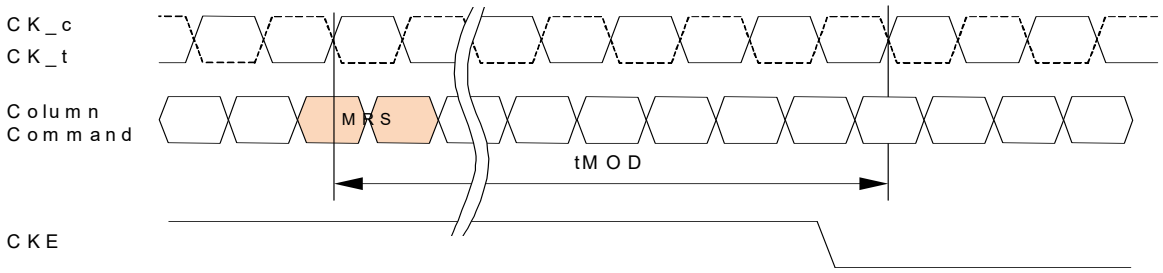
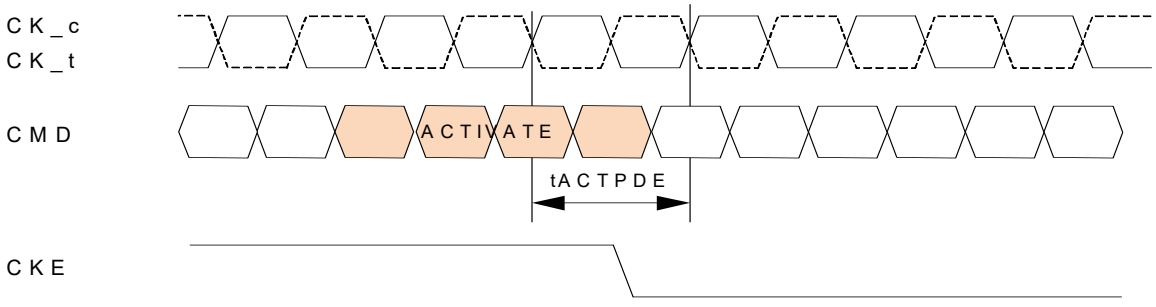
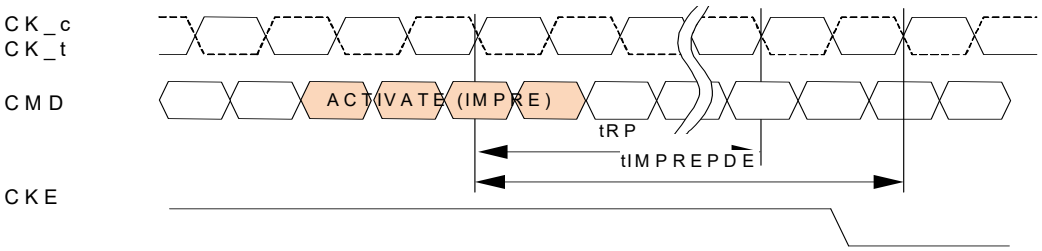


Figure 61. MODE REGISTER SET to Power-Down Entry Timing



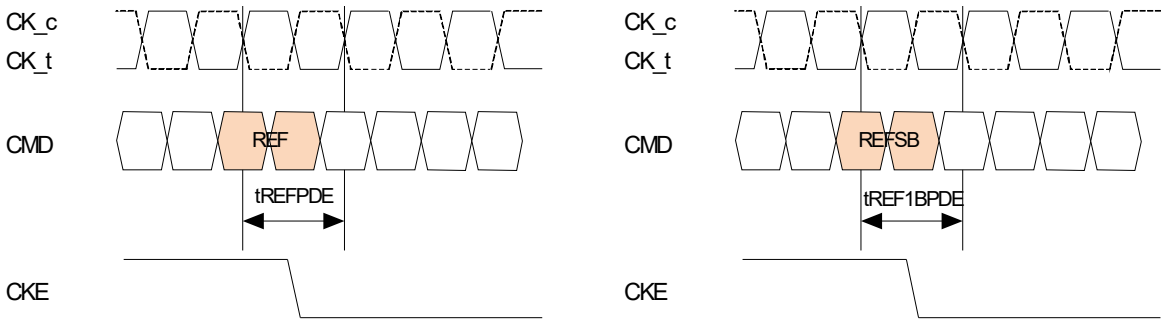
1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

Figure 62. ACTIVATE to Power-Down Entry Timing



1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

Figure 63. ImPRE to Power-Down Entry Timing



1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

Figure 64. REFRESH or SINGLE BANK REFRESH to Power-Down Entry Timing

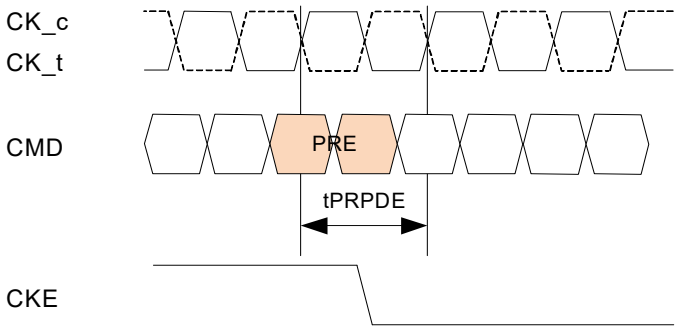


Figure 65. PRECHARGE to Power-Down Entry Timing

6.3.4.2. Self-Refresh(SRE,SRX)

Self-refresh can be used to retain data in the HBM device, even if the rest of the system is powered down. When in the self-refresh mode, the HBM device retains data without external clocking. The SELF REFRESH ENTRY command is like a REFRESH command except that CKE is pulled LOW. The command is received on the row command inputs R[5:0] as shown in Figure 66 and requires a CNOP command on the column command inputs C[7:0].

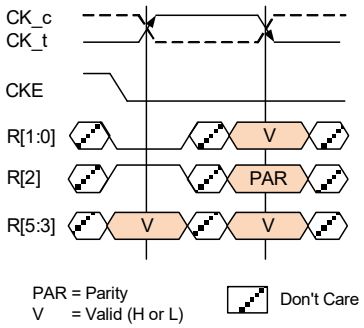


Figure 66. SELF-REFRESH-ENTRY Command

Self-refresh entry is only allowed when all banks are precharged with t_{RP} satisfied, the last data elements from a preceding READ command have been pushed out (t_{RDSRE}), or t_{MOD} from a preceding MODE REGISTER SET command is met. RNOP and CNOP commands are required after entering self-refresh mode until t_{CPDED} is met.

Once the SELF-REFRESH-ENTRY command is registered, CKE must be held LOW to keep the device in self-refresh mode. When the device has entered the self-refresh mode, all external control signals except CKE and RESET_n are “Don’t care”. For proper self-refresh operation, all power supply pins (VDDC, VDDQ, VSS, VSSQ, VPP) must be at valid levels. The HBM device initiates a minimum of one internal refresh within t_{CKE} period once it enters self-refresh mode.

The clocks are internally disabled during self-refresh operation to save power. The minimum time that the HBM device must remain in self-refresh mode is t_{CKESR}. The user may halt the external clock or change the external clock frequency t_{CKSRE} after self-refresh entry is registered. However, the clock must be restarted and stable t_{CKSRX} before the device can exit self-refresh operation.

While in self refresh the device will continue driving RDQS_t and RDQS_c to LOW and HIGH static levels, respectively, and TEMP and CATTRIP to valid HIGH or LOW levels.

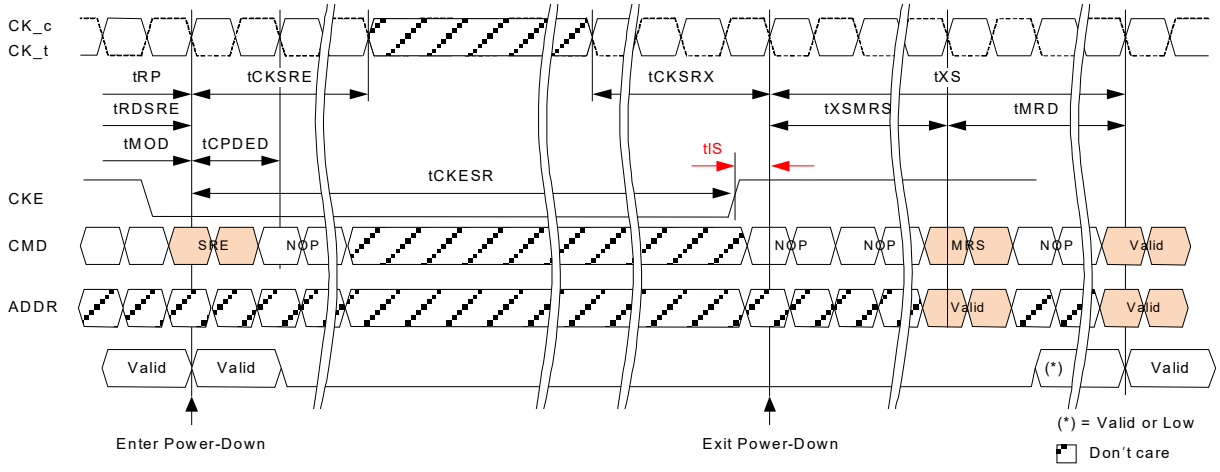
If enabled, parity is evaluated for the SELF REFRESH ENTRY command. The HBM device requires RNOP and CNOP commands with valid parity for the entire t_{CPDED} period, while it will suspend parity checking after self refresh entry and drive AERR and DERR to a static LOW.

Parity is not evaluated for the SELF REFRESH EXIT command. The HBM device requires RNOP and CNOP commands with valid parity for the entire t_{XS} period, while within t_{XS} period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time.

The procedure for exiting self-refresh requires a sequence of events. First, the CK_t/CK_c clock must be stable

prior to CKE going back HIGH. A delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

Upon exit from self-refresh, the HBM device can be put back into self-refresh mode after waiting at least t_{XS} period and issuing one extra REFRESH command.



1. Only RNOP and CNOP commands allowed during tCPDED and tXS periods, except for MRS commands which are allowed tXSMRS after self-refresh exit.
2. Write bursts must have been completed with tRP satisfied prior to self-refresh entry.
3. Read bursts must have been completed with tRDPDE satisfied prior to self-refresh entry.
4. Address inputs are "Don't Care" for self-refresh entry and exit.
5. AERR, DERR are driven LOW when parity check is suspended during self refresh. Signals are shown with tPARAC=0 and tPARDQ=0 for illustration purpose.

Figure 67. Self-Refresh Entry and Exit

6.4. Parity

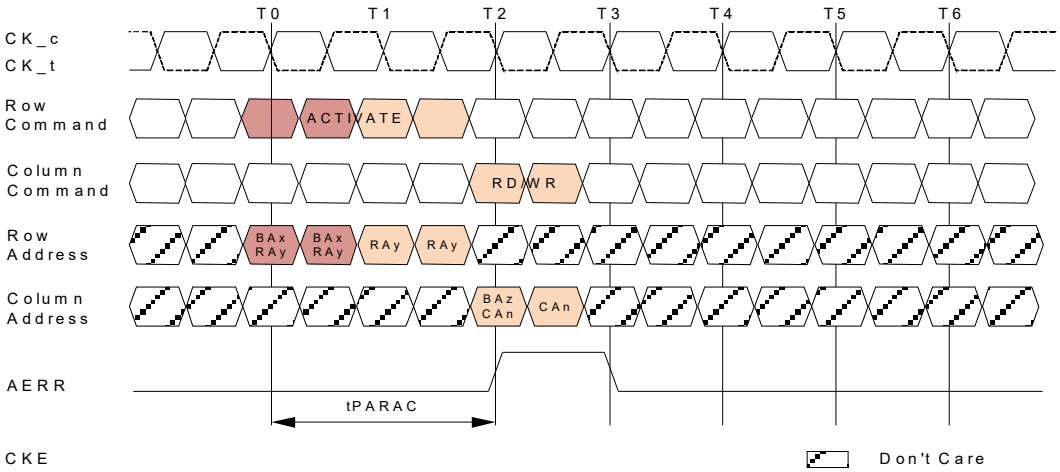
6.4.1. Command/Address Parity

The HBM device includes a per-channel Command/Address parity checking function. There is one AERR output pin per AWORD. The HBM device accepts a parity input from the memory controller per the respective Row or Column command truth table, compares it with the data received on the rising and falling CK clock edges of the respective R[5:0] or C[7:0] inputs for that clock cycle, and indicates on the AERR pin whether a parity error has occurred. The HBM device executes the command(s) regardless of a command/address parity error.

The Command/Address Parity function is disabled by default. The parity function can be enabled in MR0 OP[6] (see Table 9). The HBM device may begin to check parity on the next clock cycle following the MRS command that enables the parity checking function; it guarantees to check parity t_{MOD} after that MRS command. The host controller must drive valid parity next clock cycle after parity is enabled in the mode register. The HBM device guarantees to disable parity checking t_{MOD} after an MRS command disables the parity checking function. The host controller must drive valid parity until t_{MOD} after parity is disabled in MR0 OP[6]. See also section "Power-Down (PDE,PDX)" and section "Self-Refresh(SRE,SRX)". AERR is always driven LOW by the HBM device at RESET.

For every address parity error, AERR is driven HIGH for 1 t_{CK}, t_{PARAC} after the corresponding cycle of the error inputs. In the case of consecutive errors, the AERR signal will stay HIGH during the next cycle.

Figure 68 illustrates a single parity error occurrence on the R[5:0] inputs. In this case, an error occurs in T0, the first cycle of the ACTIVATE command. After t_{PARAC}, AERR is driven HIGH for 1 t_{CK} and then LOW since no subsequent errors occur.

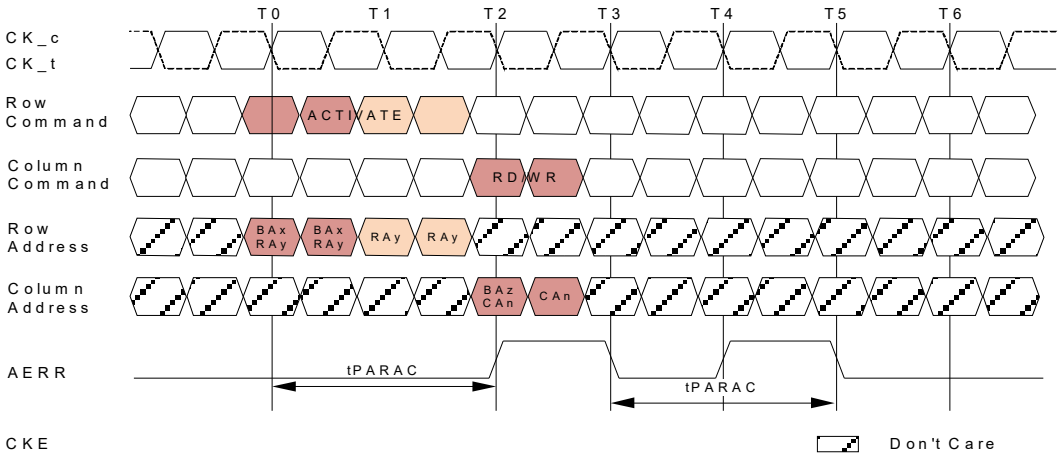


T0 : Row Cmd/Addr Error

Note 1 : For illustration purpose, tPARAC is shown with 2 tCK digital and 0 ns analog output delay.

Figure 68. Command/Address Parity Error

Figure 69 illustrates parity error occurrences on the R-inputs and the C-inputs. In this case, an error occurs in T0, the first cycle of the ACTIVATE command. After t_{PARAC}, AERR is driven HIGH for 1 t_{CK} and then LOW for 1 t_{CK}. Since an error also occurs in T2, the RD/WR command, AERR is again driven HIGH for 1 t_{CK} and then LOW since no subsequent errors occur.

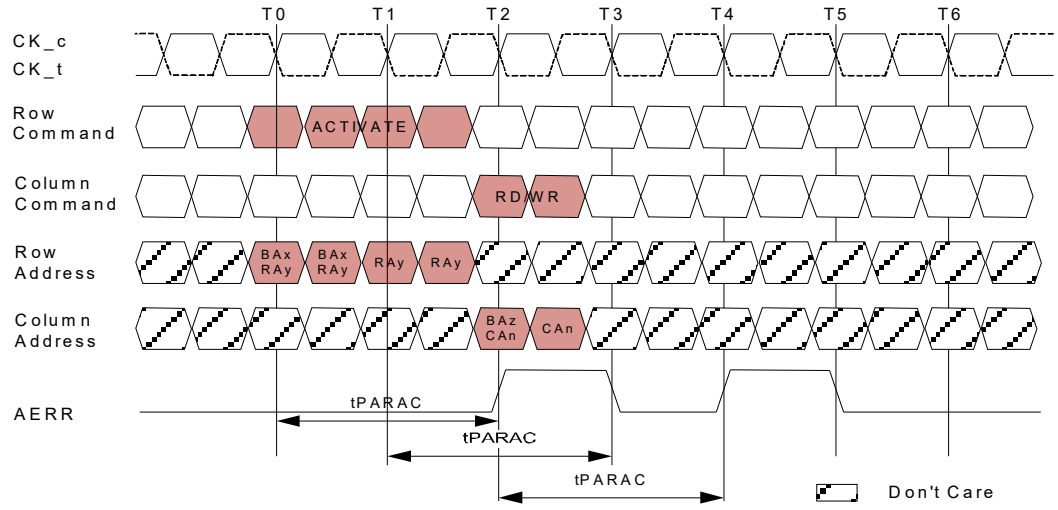


T0 : Row Cmd/Addr Error
T2 : Col Cmd/Addr Error

Note 1 : For illustration purposes. The figure is shown with 2 tCK digital and 0 ns analog output delay. Vendor datasheets should be consulted for actual value.

Figure 69. Separated Command/Address Parity Errors

Figure 70 illustrates consecutive cycle errors, such that parity errors occur during the T0, T1, and T2 cycles on either or both interfaces. Due to the common AERR output, parity error occurrences on both interfaces on the same cycle are indistinguishable.



T0, T1, T2 : Row and/or Col Cmd/Addr Error

Note 1: For illustration purposes, the figure is shwon with 2 tCK digital and 0 ns analog output delay. Vendor datasheets should be consulted for actual value.

Figure 70. Consecutive Command/Address Parity Errors

Table 36 specifies the parity function for each clock cycle.

Table 36 - Parity Function Table

Inputs	Σ of Inputs	PAR	AERR Output	Note
Row R[5:0] - Minus PAR bit	Even	L	L	1
		H	H	
	Odd	L	H	
		H	L	
Column C[7:0] - Minus PAR bit	Even	L	L	1
		H	H	
	Odd	L	H	
		H	L	

Notes:

1. See "Command Truth Table" for command and device state exceptions.

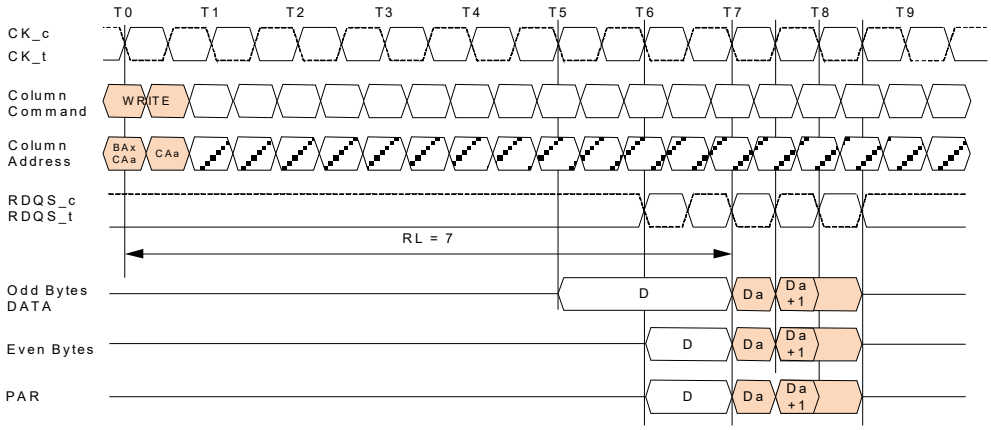
6.4.2. DQ Parity

The HBM device includes a DQ parity checking function. There is one PAR bidirectional IO and one DERR output signal per DWORD. On write transactions, the HBM device compares the PAR input with the corresponding data received on DQ, DM and DBI inputs, and indicates on the DERR pin whether a parity error has occurred. On read transactions, the HBM generates parity and transmits the parity on the PAR signal along with the corresponding data on DQ and DBI.

The DQ Parity function is disabled by default. The parity function can be enabled in MR0 OP[5] for Writes and OP[4] for Reads (see Table 9). The HBM device may begin to check parity on the next clock cycle following the MRS command that enables the parity checking function; it guarantees to check parity t_{MOD} after that MRS command. The HBM device guarantees to disable parity checking t_{MOD} after an MRS command disables the parity checking function. See also "Mode Register Set (MRS)". DERR is always driven LOW by the HBM device at RESET.

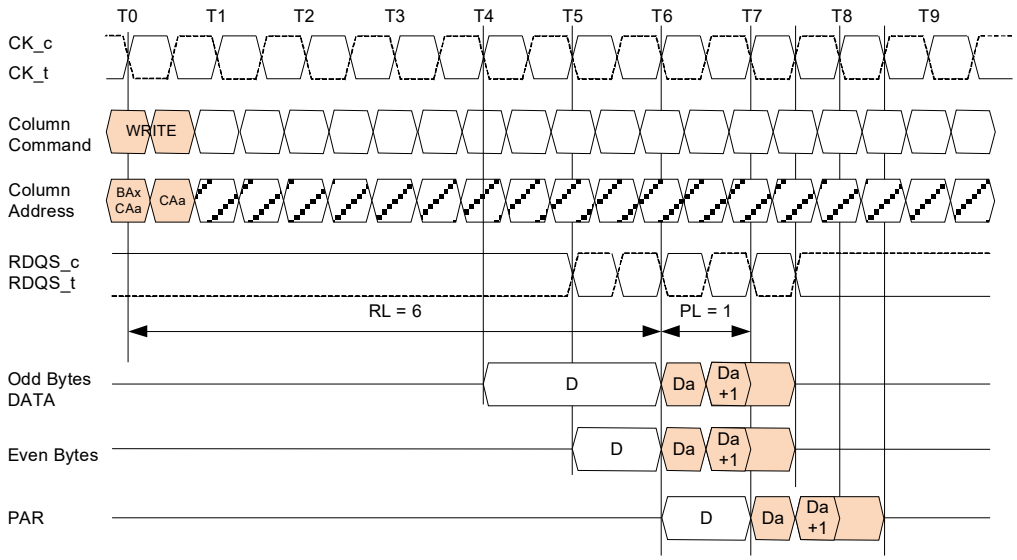
The DQ Parity function includes a programmable parity latency PL between the PAR signal and the corresponding data with 0 nCK. PL is programmed in MR4 OP[3:2] (see Table 15), and is the same for Writes and Reads. With a latency of 0 nCK the PAR signal and corresponding data are received and sent simultaneously; with all other values of PL the corresponding PAR signal will be received and sent PL cycles later. The WDQS and RDQS signals will have additional strobe cycles with the same preamble and postambles to accommodate the latching of the delayed PAR signal at both ends. The DRAM vendor's datasheet shall be consulted for the range of supported PL values.

If an error occurs in either or both UI of a write transaction, DERR is driven HIGH for 1 t_{CK} at the input clock edge t_{PARDQ} clocks after the corresponding cycle of error inputs. In case of two consecutive cycle errors, DERR will stay HIGH during the next cycle. When an error occurs, the HBM device does not block the Write data. The HBM device completes the Write transaction to the array as normal. Examples of single read bursts with BL=2 are shown in Figure 71 for the PL=0 case and Figure 72 for the PL=1 case. The PAR output is preconditioned over 1 cycle like for the even data bytes. With PL=1 an additional RDQS postamble cycle for PAR is transmitted at cycle T8.



1. BAx = bank address x; CAa = column address a.
2. RL = 7 and PL = 0 are shown as examples.
3. RDQS ? RDQS[3:0]; DATA = DQ[127:0], DBI[15:0], PAR[3:0]
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK = 0 and nomianl tLZ, tHZ is shown for illustration purposes.

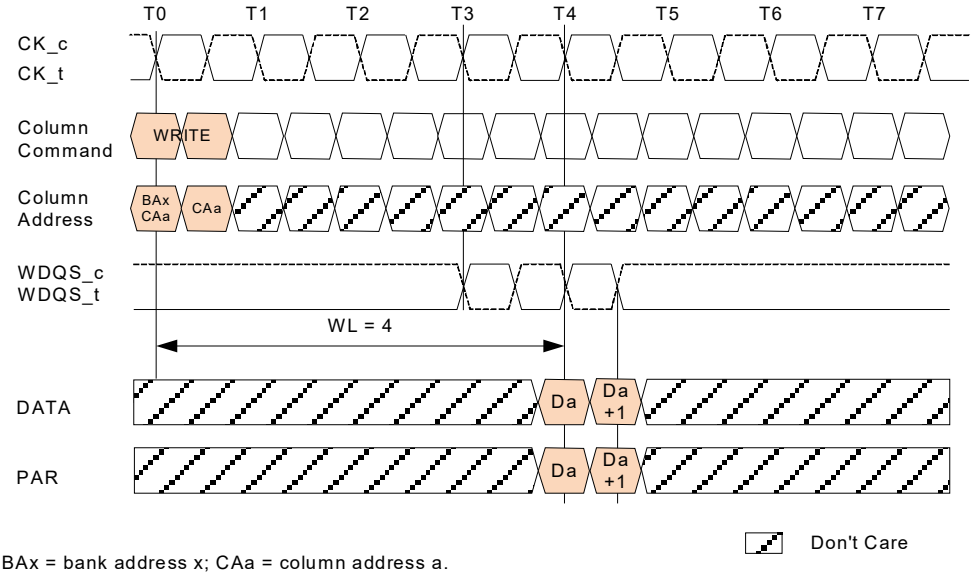
Figure 71. Read Parity Alignment with PL=0



1. BAx = bank address x; CAa = column address a.
2. RL = 6 and PL = 1 are shown as examples.
3. RDQS ? RDQS[3:0]; DATA = DQ[127:0], DBI[15:0], PAR[3:0]
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK = 0 and nomianl tLZ, tHZ is shown for illustration purposes.

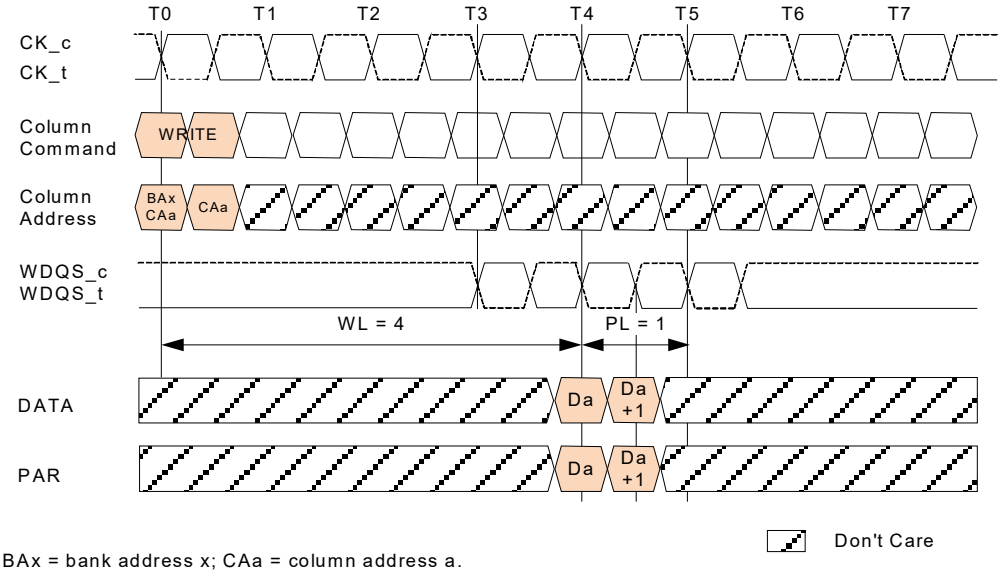
Figure 72. Read Parity Alignment with PL = 1

Examples of single write bursts with BL=2 are shown in Figure 73 for the PL=0 case and Figure 74 for the PL=1 case. With PL=1 an additional WDQS cycle for PAR is expected at cycle T5 to latch the PAR input.



1. BAx = bank address x; CAa = column address a.
2. WL = 4 and PL = 0 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0], PAR = PAR[3:0].
4. Da, Daa+1 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.

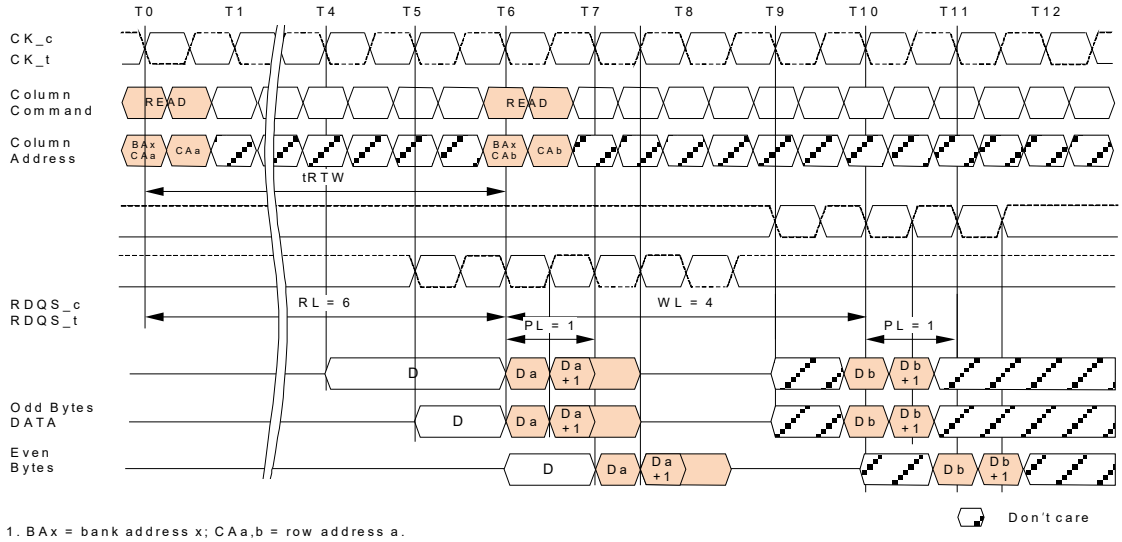
Figure 73. Write Parity Alignment with PL=0



1. BAx = bank address x; CAa = column address a.
2. WL = 4 and PL = 0 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0], PAR = PAR[3:0].
4. Da, Daa+1 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.

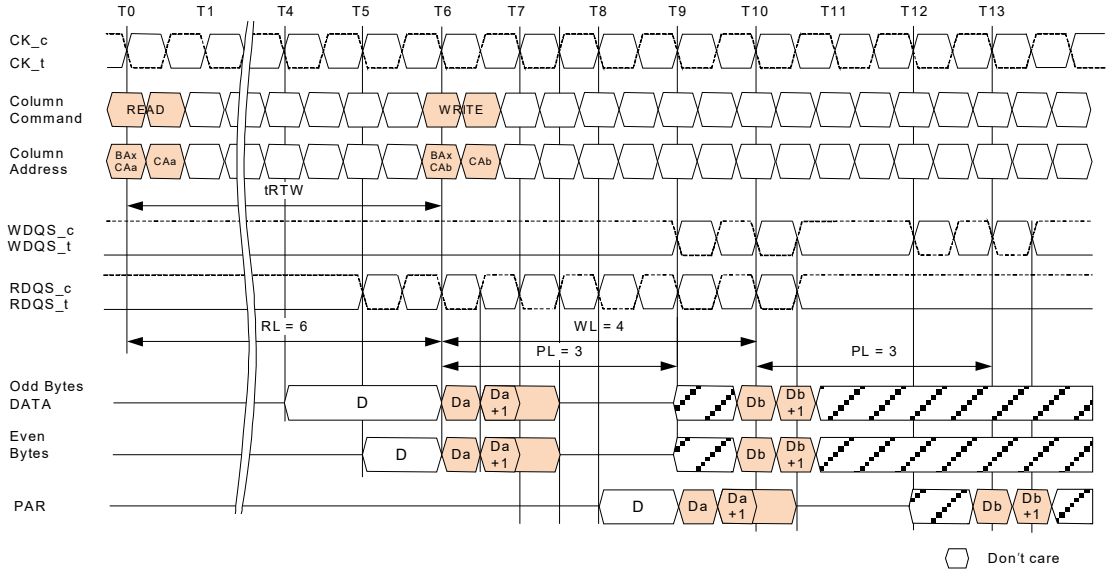
Figure 74. Write Parity Alignment with PL=1

The parity latency PL has no impact on the minimum bus turnaround time. As the PAR signal is delayed by the same number of cycles for Reads and Writes, its turnaround is only delayed as compared to the data bytes by the programmed number of cycles as illustrated in Figure 75 for PL=1 and Figure 76 for the extreme case of PL=3.



1. BAx = bank address x; CAa,b = row address a.
2. RL = 6 WL = 4 and PL = 1 are shown as an example.
3. RDQS = RDQS0, RDQS3; WDQS = WDQS3; DATA = DQ0... DQ127, DM0...DM15, DBI0...DBI15.
   PAR = PAR0...PAR3
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. Db, b+1 = data-in for WRITE command b.
6. tDQSCK, tDQSS = 0 and nominal tLZ, tHZ is shown for illustration purposes.
7. tRTW is not a device limit but determined by the system bus turnaround time.
8. DBI(ac) could be on or off.

Figure 75. Read-to-Write Bus Turnaround with PL=1



1. BAx = bank address x; CAa,b = row address a.
2. RL = 6 WL = 4 and PL = 3 are shown as an example.
3. RDQS = RDQS0, RDQS3; WDQS = WDQS3; DATA = DQ0... DQ127, DM0...DM15, DBI0...DBI15. PAR = PAR0...PAR3
4. Da, a+1 = data-out for READ command a.
   D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. Db, b+1 = data-in for WRITE command b.
6. tDQSCK, tDQSS = 0 and nominal tLZ, tHZ is shown for illustration purposes.
7. tRTW is not a device limit but determined by the system bus turnaround time.
8. DBI(ac) could be on or off.

Figure 76. Read-to-Write Bus Turnaround with PL=3

Figure 77 illustrates a single cycle DQ parity error occurrence on a write transaction. In this case, an error occurs in T0, in either or both of the UI. After t_{PARDQ}, DERR is driven HIGH for 1 t_{CK} and then LOW since no subsequent errors occur.

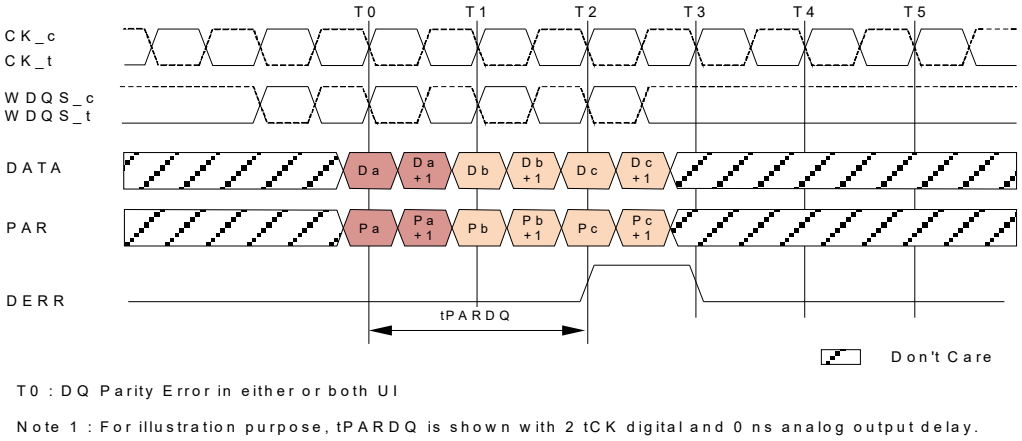


Figure 77. Write Parity Error

Figure 78 illustrates parity error occurrences on separated cycles. In this case, an error occurs in either or both UIs of T0. DERR is driven HIGH for 1 t_{CK}. Since an error also occurs in either or both UI of T2, DERR is again driven HIGH for 1 tCK and then LOW since no subsequent errors occurs.

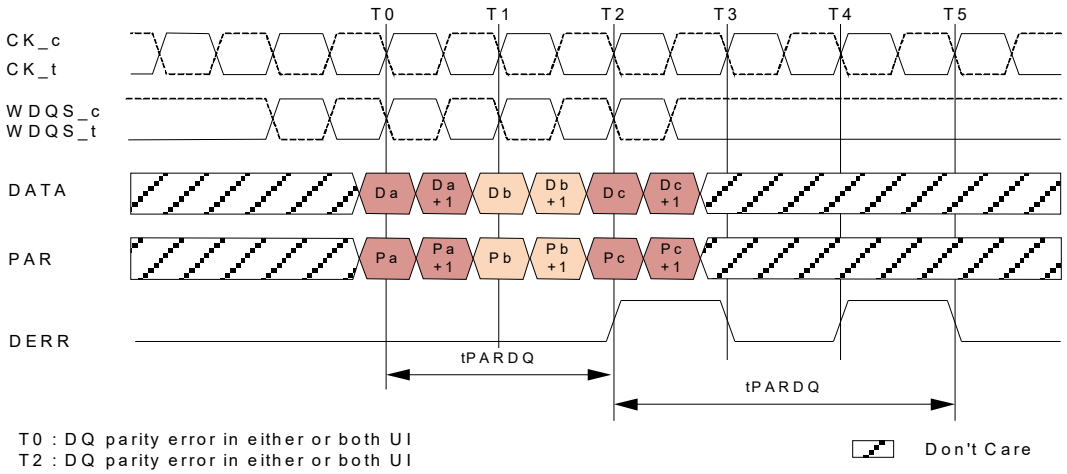
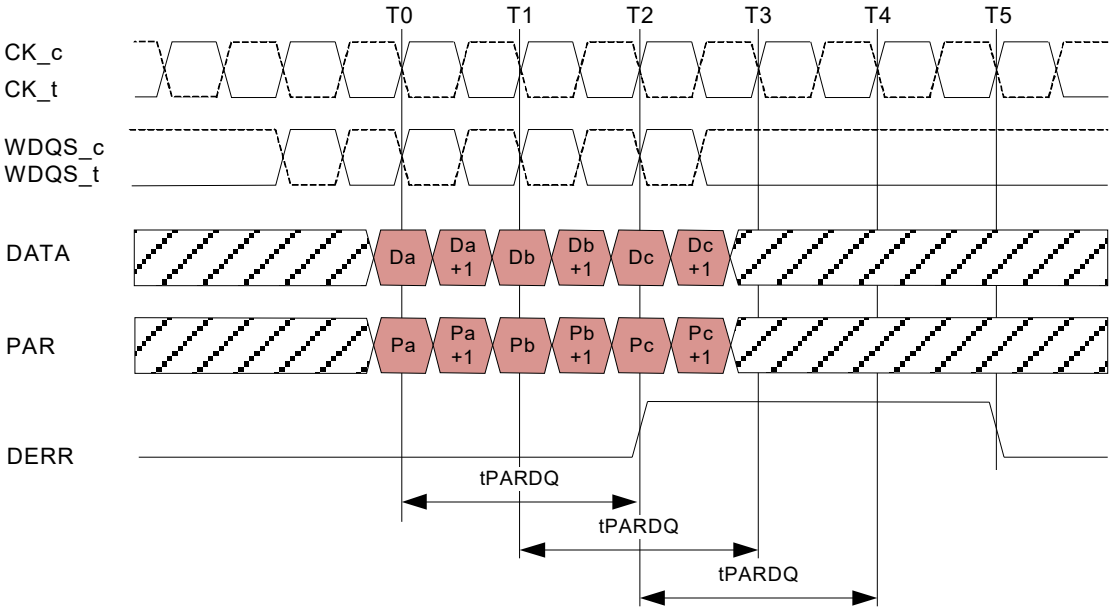


Figure 78. Separated Write Parity Error

Figure 79 illustrates consecutive cycle errors, such that parity errors occur during the T0, T1, and T2 cycles.



T0, T1, T2 : DQ parity error in either or both UI

Don't Care

Note 1 : For illustration purpose, the figure is shown with 2 tCK digital and 0 ns analog output delay. Vendor datasheets should be consulted for actual value.

Figure 79. Consecutive Wirte Parity Error

Table 37 specifies the DQ parity function for each UI of the burst.

Table 37 - DQ Parity Function Table

Mode Register Configuration			Inputs	Σ of Inputs	PAR	DQERR Output
DBI[1]	DM	ECC				
Enabled	Enabled	Disabled	DQ[31:0], DBI[3:0], DM[3:0][2]	Even	L	L
					H	H
				Odd	L	H
					H	L
Enabled	Disabled	Enabled	DQ[31:0], DBI[3:0]	Even	L	L
					H	H
				Odd	L	H
					H	L
Enabled	Disabled	Disabled	DQ[31:0], DBI[3:0]	Even	L	L
					H	H
				Odd	L	H
					H	L
Disabled	Enabled	Disabled	DQ[31:0], DM[3:0][2]	Even	L	L
					H	H
				Odd	L	H
					H	L
Disabled	Disabled	Enabled	DQ[31:0]	Even	L	L
					H	H
				Odd	L	H
					H	L
Disabled	Disabled	Disabled	DQ[31:0]	Even	L	L
					H	H
				Odd	L	H
					H	L

Note 1 Command types dependent on configuration. See Table 9 for Read DBIac and Write DBIac.
Note 2 Write command only. DM[3:0] excluded from parity function of Read command.
Note 3 Data inputs are included in the parity calculation for writes regardless whether a byte is masked by DM or not.

6.5. Clock Frequency Change Sequence

Clock Frequency changes can occur during Self-Refresh mode. When the CK_t/CK# clock is stopped after Self-Refresh Entry, it can be restarted at a different frequency. If the change in clock-rate requires changes to configuration parameters, MRS commands immediately prior to or after Self-Refresh Mode may be required.

6.6. Target Row Refresh (TRR) Mode

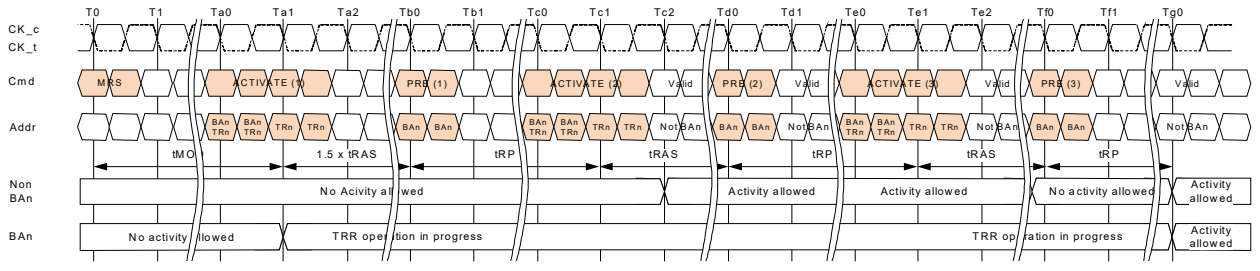
The HBM DRAM row has a limited number of times a given row can be accessed within a certain time period prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the Maximum Activate Window (t_{MAW}) before the adjacent rows needs to be refreshed regardless of how the activates are distributed over t_{MAW}. The row receiving the excessive activates is the Target Row (TRn), the two adjacent rows to be refreshed are the victim rows.

When the MAC limit is reached on TRn, either the SDRAM must receive roundup (t_{MAW}/t_{REFI}) Refresh Commands (REF) before another row activate is issued, or the HBM DRAM should be placed into Target Row Refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the Activates from two target rows on a victim row should not exceed MAC value as well.

Table 16 shows fields required to support the new TRR settings. Setting MR5 OP[7] = 1 enables TRR mode and setting MR5 OP[7] = 0 disables TRR mode. MR5 OP[3:0] defines which bank (BAn) the target row is located in.

The TRR mode must be disabled during initialization as well as any other HBM DRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR5OP[7] = 0 to interrupt and reissue the TRR mode is allowed in the case, such as the DRAM detecting a Parity error during TRR mode.

When enabled; TRR mode is self-clearing; the mode will be disabled automatically after the completion of defined TRR flow; after the 3rd BAn precharge has completed plus t_{MOD}. Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR5 OP[7] = 0; if the TRR is exited via another MRS command, the value written to MR5 OP[3:0] are don't cares.



1. TRn is the targeted row.
2. BAn is the bank address of targeted row.
3. TRR mode self-clears after tMOD+tRP measured from the 3rd BAn PRECHARGE at clock edge Tg0.
4. TRR mode or any other activity can be re-engaged after tRP+tMOD from the 3rd Ban PRECHARGE, PREALL may be issued instead of PREn. TRR mode is cleared after 3rd PRE to bank BAn.
5. ACTIVATE commands to BAn during TRR mod do not provide refreshing support, i.e. the refresh counter is unaffected.
6. The HBM DRAM must restore the degraded row caused by excessive activation of the targeted row TRn necessary to meet refresh requirements.
7. A new RTT mode must wait tMOD+tRP time after the 3rd PRECHARGE.
8. ACT and PRE are the only allowed commands to BAn during TRR mode.
9. REFRESH commands are not allowed during TRR mode. REFSB commands to non-BAn banks are allowed during TRR mode.
10. All HBM DRAM timings such as tFAW are to be met during RTT mode. Issuing ACT(1), ACT(2), ACT(3) counts towards tFAW budget.

Figure 80. TRR Mode

6.6.1. TRR Mode Operation

1. The timing diagram in Figure 80 depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three corresponding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. The Precharge All (PREA) command issued while the HBM DRAM is in TRR mode will also perform precharge to BAn and counts toward a PREn command. Implict Precharge is not supported in TRR mode.

2. Prior to issuing the MRS command to enter TRR mode, the HBM DRAM should be in the idle state. A MRS command must be issued with MR5 OP[7] = 1, MR5 OP[3:0] containing the targeted bank in which the targeted row is located. All other MR5 bits should remain unchanged.

3. No activity is to occur in the DRAM until t^{MOD} has been satisfied. Once t_{MOD} has been satisfied.

4. The first ACT to the BAn with the TRn address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until $[(1.5*t_{RAS}) + t_{RP}]$ is satisfied. The only commands to BAn allowed are ACT and PRE until the TRR mode has been completed.

5. After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued (1.5*tRAS) later; and then followed tRP later by the second ACT to the BAn with the TRn address. Once the 2nd activate to the BAn is issued, non BAn bank groups are allowed to have activity.

6. After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued tRAS later and then followed tRP later by the third ACT to the BAn with the TRn address.

7. After the third ACT to the BAn with the TRn address is issued, a PRE to BAn would be issued tRAS later; and once the third PRE has been issued, non BAn banks are not allowed to have activity until TRR mode is exited. The TRR mode is completed once tRP plus tMOD is satisfied.

8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any time the TRR mode is interrupted and not completed, the interrupted TRR mode must be cleared and then subsequently performed again. To clean an interrupted TRR mode, an MR5 change is required with setting MR5 OP[7] = 0, MR5 OP[3:0] are don't care, followed by three PRE to BAn, tRP time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.

9. Refresh command to the HBM DRAM or entering Self-Refresh mode is not allowed while the DRAM is in TRR mode.

6.7. Temperature Compensated Refresh Reporting

The HBM DRAM provides temperature compensated refresh related information to the controller via an encoding on the TEMP[2:0] pins. The Gray-coded encoding defines the proper refresh rate expected by the DRAM to maintain data integrity. Absolute temperature values for each encoding are vendor specific and not defined in this specification.

The encoding on the TEMP[2:0] pins is expected to reflect the required refresh rate for the hottest device in the stack and will be updated when the temperature exceeds the vendor specific trip-point levels appropriate for each refresh rate.

6.7.1. Temperature Compensated Refresh Trip Points

The HBM DRAM provides three bit port (TEMP[2:0]) that exports temperature compensated refresh status bits.

Table 38 - Temperature Compensated Refresh Trip Points

TEMP	Refresh Rate	Temperature range [Tj]
000	$4Xt_{REFI}$	~24℃
001	$2Xt_{REFI}$	25~39℃
011	$1Xt_{REFI}$	40~84℃
010	$0.5Xt_{REFI}$	85~94℃
110	$0.25Xt_{REFI}$	95~105℃

6.7.2. Catastrophic Temperature Sensor

The CATTRIP sensor logic detects if the junction temperature of any die in the HBM stack exceeds the catastrophic trip threshold value CATTEMP. CATTEMP value is 125℃. If the junction temperature anywhere in the stack exceeds the CATTEMP of the device, the HBM stack will drive the external CATTRIP pin to “1”. This indicates that catastrophic damage may occur unless power is reduced. The CATTRIP output is sticky in that to clear a CATTRIP, power-off of the device is required to return the CATTRIP output to “0”. Sufficient time should be allowed for the device to cool after a CATTRIP event. See "HBM Power-up and Initialization Sequence" for the initialization of the CATTRIP pin during powerup.

If CATTEMP is higher than maximum operating junction temperature, CATTRIP circuit will operate correctly regardless of whether the external or internal clocks have stopped. Functionality testing of CATTRIP can be verified by writing a “1” to MR7 OP[7] to force a CATTRIP and “0” to clear.

CATTRIP is a mandatory feature for the HBM device with 4 Gb/Channel or higher for Legacy mode and 2 Gb/Channel or higher for Pseudo channel mode operation.

6.8. Interconnect Redundancy Remapping

The HBM DRAM supports interconnect lane remapping to help improve SIP assembly yield and recover functionality of the HBM stack. The "SOFT_LANE_REPAIR and HARD_LANE_REPAIR" instructions are used to perform lane remapping. Lane remapping is independent for each channel.

The HBM DRAM can be programmed to retain the remapped lane information even when power is completely removed from the HBM stack.

6.8.1. AWORD Remapping

Row command bus and column command bus is allowed to remap one lane for each bus. CK_c, CK_t, CKE and AERR signals cannot be remapped. After a lane is remapped, the input buffer associated with the broken lane is turned off and the input buffer associated with the redundant pin (RR or RC) is turned on. All functionalities are preserved with row or column bus lane remapping.

6.8.1.1. Row Command Bus - Remapping Table

Table 39 - AWORD - Row Command Bus Remapping

Description	Register Encoding	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RRx
Repair Lane 0	0000	XX	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5
Repair Lane 1	0001	Rx0	XX	Rx1	Rx2	Rx3	Rx4	Rx5
Repair Lane 2	0010	Rx0	Rx1	XX	Rx2	Rx3	Rx4	Rx5
Repair Lane 3	0011	Rx0	Rx1	Rx2	XX	Rx3	Rx4	Rx5
Repair Lane 4	0100	Rx0	Rx1	Rx2	Rx3	XX	Rx4	Rx5
Repair Lane 5	0101	Rx0	Rx1	Rx2	Rx3	Rx4	XX	Rx5
Reserved	0110 to 1110	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RFU
Default - No Repair	1111	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RFU
Note 1. X = any channel [a:h] Note 2. XX = Lane is remapped Note 3. RFU = Pin is not used								

6.8.1.2. Column Command Bus - Remapping Table

Table 40 - AWORD - Column Command Bus Remapping

Description	Register Encoding	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RCx
Repair Lane 0	0000	XX	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 1	0001	Cx0	XX	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 2	0010	Cx0	Cx1	XX	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 3	0011	Cx0	Cx1	Cx2	XX	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 4	0100	Cx0	Cx1	Cx2	Cx3	XX	Cx4	Cx5	Cx6	Cx7
Repair Lane 5	0101	Cx0	Cx1	Cx2	Cx3	Cx4	XX	Cx5	Cx6	Cx7
Repair Lane 6	0110	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	XX	Cx6	Cx7
Repair Lane 7	0111	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	XX	Cx7
Reserved	1000 to 1110	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RFU
Default - No Repair	1111	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RFU
Note 1. X = any channel [a:h] Note 2. XX = Lane is remapped Note 3. RFU = Pin is not used										

6.8.1.3. AWORD Remapping Example

As an example, Ca6 and Ra0 are broken lanes for Column Command bus and Row Command bus respectively. The lanes are remapped by programming channel A LANE REPAIR WDR bits AWORD_CA[3:0] to 6h and bits AWORD_RA[3:0] to 0h.

Table 41 - Original Lane Assignment - Channel A - AWORD

	Ca7		Ca5		CKEa		Ca3		Ca1		ARFUa0
RCa		Ca6		Ca4		ARFUa1		Ca2		Ca0	
	ARFUa4		Ra5		CKa_c		Ra3		Ra1		ARFUa3
AERRa		RRa		Ra4		CKa_t		Ra2		Ra0	

Table 42 - Remapped Lane Assignment - Channel A - AWORD

	Ca6		Ca5		CKEa		Ca3		Ca1		ARFUa0
Ca7		*XX*		Ca4		ARFUa1		Ca2		Ca0	
	ARFUa4		Ra4		CKa_c		Ra2		Ra0		ARFUa3
AERRa		Ra5		Ra3		CKa_t		Ra1		*XX*	

6.8.2. DWORD Remapping

Two modes are provided to remap the data bus:

- In Mode 1 it is allowed to remap one lane per byte. No redundant pin is allocated in this mode, and DBI functionality is lost for that byte only however other bytes continue to support DBI function as long as the Mode Register setting for DBI function is enabled. If Data Parity function is enabled in the Mode Register and a lane is remapped, both DRAM and host assume DBI input as "0" for parity calculation for Read and Write operation in this mode.In Mode 1 each byte is treated independently.

- In Mode 2 it is allowed to remap one lane per double byte. One redundant pin (RD) per double byte is allocated in this mode, and DBI functionality is preserved as long as the Mode Register setting for DBI function is enabled. The use of Mode 2 has no impact on the Data Parity function.In Mode 2 two adjacent bytes (e.g. DQ[15:0]) are treated as a pair (double byte), but each double byte is treated independently.

The two modes are distinguished by the use of the "1110b" encoding as shown in the table below. The use of Mode 1 is assumed when a remapping code other than "1110b" is used. For Mode 2 it is required to program "1110b" for the intact byte within the double byte while the remapping for the broken lane in the other byte is encoded according to the table.

WDQS_c, WDQS_t, RDQS_c, RDQS_t, PAR and DERR signals cannot be remapped.

After a lane is remapped, the input buffer associated with the broken lane is turned off and the output driver is tri-stated; with Mode 2 the input buffer associated with the redundant pin (RD) is additionally turned on and the output driver is activated.

During Reads, the RD output drivers are enabled along with the DQ, DBI and DM pins of the physical byte the pin is located in: RD0, RD2, RD4 and RD6 are located within even bytes and thus enabled one clock cycle prior to the first valid data bit, and RD1, RD3, RD5 and RD7 are located within odd bytes and thus enabled two clock cycles prior to the first valid data bit.

A DWORD byte lane repair using Mode 1 leads to the loss of DBI functionality in that byte. Increased power supply noise shall be expected within the repaired and topologically adjacent byte lanes sharing common VSS and VDDQ power rails. The exact impact depends on the specific HBM design and characteristics of the power supply to the HBM device. It is suggested to characterize the effect during system qualification and e.g. restrict the allowed byte lane repairs within a region of the HBM's ball matrix.

6.8.2.1. DWORD Remapping Table

Table 43 - DWORD Remapping (1Byte)

Description	Register Encoding	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RDx0
Repair Lane 0	0000	XX	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 1	0001	DMx0	XX	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 2	0010	DMx0	DQx0	XX	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 3	0011	DMx0	DQx0	DQx1	XX	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 4	0100	DMx0	DQx0	DQx1	DQx2	XX	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 5	0101	DMx0	DQx0	DQx1	DQx2	DQx3	XX	DQx4	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 6	0110	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	XX	DQx5	DQx6	DQx7	RFU/ DBIx0
Repair Lane 7	0111	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	XX	DQx6	DQx7	RFU/ DBIx0
Repair Lane 8	1000	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	XX	DQx7	RFU/ DBIx0
Repair Lane 9	1001	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	XX	RFU/ DBIx0
Reserved	1010to1101	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU
Repair in other byte (Mode 2 only)	1110	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU
Default - No Repair	1111	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU

Note 1. X = any channel[a:h]
Note 2. XX = Lane is remapped
Note 3. RFU/DBIx0 = Pin is not used (RFU) when no lane is repaired or when Mode 1 is selected for the lane repair; the pin is DBIx0 with lane remapping in Mode 2.

6.8.2.2. DWORD Remapping Examples

As an example for Mode 1, DMa0 and DQa12 are broken lanes for byte 0 and byte 1 respectively. The lanes are remapped as illustrated in Table 45 by programming channel A LANE REPAIR WDR bits DWORD0_BYTE0[3:0] to 0h and bits DWORD0_BYTE1[3:0] to 5h.

As an example for Mode 2, DMa0 is a broken lane for byte 0 while all lanes for byte 1 are intact. The lane is remapped as illustrated in Table 46 by programming channel A LANE REPAIR WDR bits DWORD0_BYTE0[3:0] to 0h and bits DWORD0_BYTE1[3:0] to Eh.

Table 44 - Original DWORD Lane Assignment - Channel A; Byte [1:0]

	DQa7		DQa5		RDa0		DQa3		DQa1		DMa0
DBIa0		DQa6		DQa4		PARa0		DQa2		DQa0	
	DQa15		DQa13		WDQSa0_c		DQa11		DQa9		DMa1
DBIa1		DQa14		DQa12		WDQSa0_t		DQa10		DQa8	

Table 45 - Remapped DWORD Lane Assignment using Mode 1 - Channel A- Byte [1:0]

	DQa6		DQa4		RDa0		DQa2		DQa0		XX
DQa7		DQa5		DQa3		PARa0		DQa1		DMa0	
	DQa14		DQa12		WDQSa0_c		DQa11		DQa9		DMa1
DBIa15		DQa13		XX		WDQSa0_t		DQa10		DQa8	

Table 46 - Remapped DWORD Lane Assignment using Mode 2- Channel A - Byte [1:0]

	DQa6		DQa4		DBIa0		DQa2		DQa0		XX
DQa7		DQa5		DQa3		PARa0		DQa1		DMa0	
	DQa15		DQa13		WDQSa0_c		DQa11		DQa9		DMa1
DBIa1		DQa14		DQa12		WDQSa0_t		DQa10		DQa8	

The circuit diagram in Figure 81 illustrates the DQ lane remapping in more detail. Physical micro-bump DQ3 will be connected to internal logical DQ3 input and output paths when the DQ3 lane is not remapped; with re-mapping the internal DQ3 input and output paths would be routed to the physical DQ4 micro-bump.

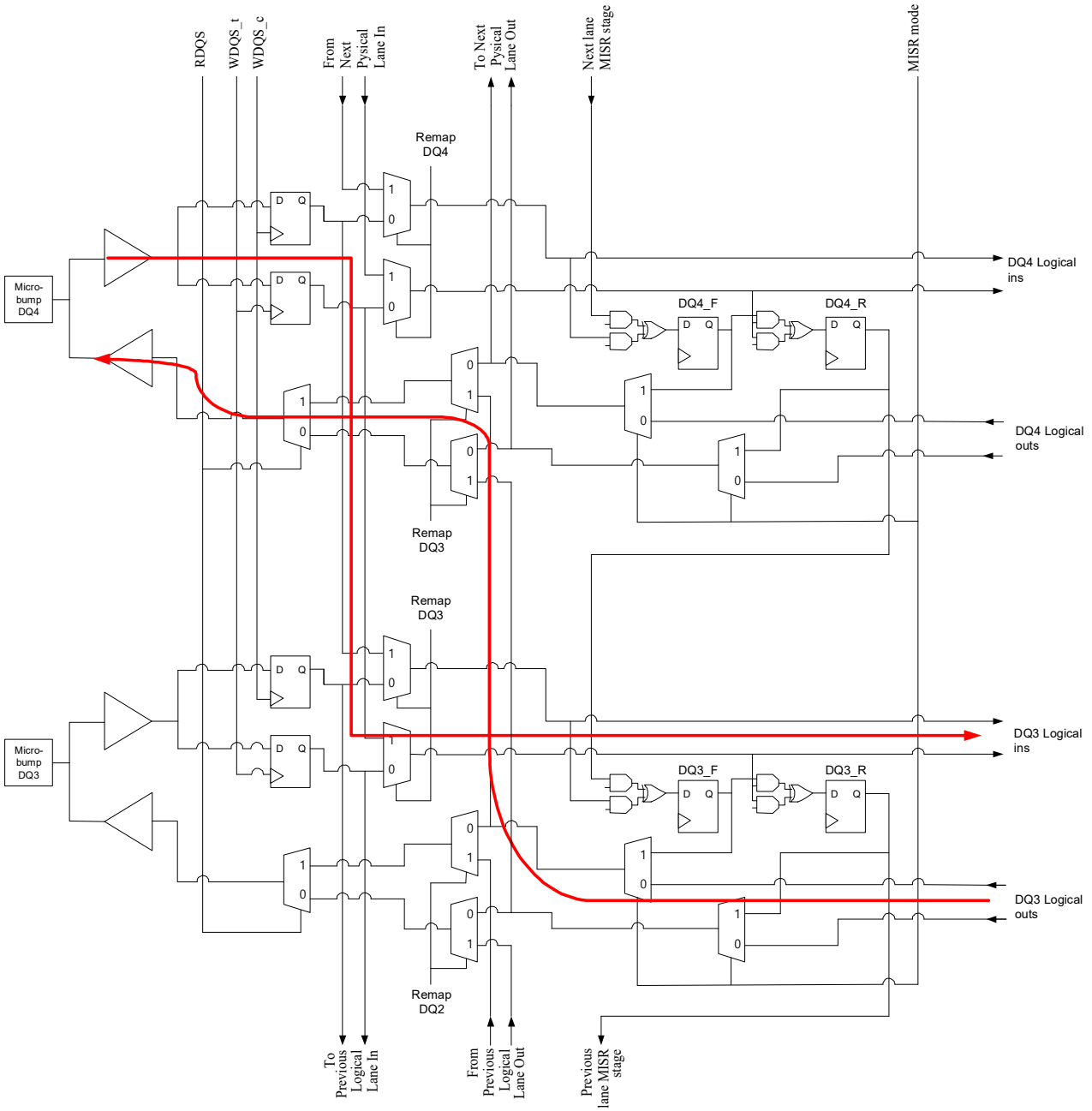


Figure 81. Example Signal Paths with Lane Repair

6.9. HBM Loopback Test Modes

A Multiple-input Shift Register (MISR) / Linear Feedback Shift Register (LFSR) circuit is defined within the HBM AWORD and DWORD IO blocks. These circuits are intended for testing and training the link between the Host and the HBM device. Referring to Figure 82, each byte within a DWORD implements a 20-bit MISR/LFSR circuit, comprised of double data rate Rise and Fall bits for each of the eight DQs plus DBI and DM signals. In operation, the MISR/LFSR circuits operate independently across the bytes. The AWORD implements a 30-bit MISR/LFSR circuit comprised of DDR Rise and Fall bits for the 15 row and column command bits, plus CKE. When the MISR registers are read via the IEEE 1500 port DWORD_MISR instruction, the four bytes per DWORD (80-bits) for the four DWORDs within a channel are serially shifted out, for a total of 320 bits. The 30-bit AWORD MISR content is read via the AWORD_MISR instruction. See Table 84 and Table 85 for the bit-orders for these MISR registers.

The term MISR modes collectively refers to all of the modes - LFSR mode, Register mode, MISR mode, and LFSR Compare mode. AWORD MISR modes and DWORD MISR modes refers to all of the modes defined for the specific bus.

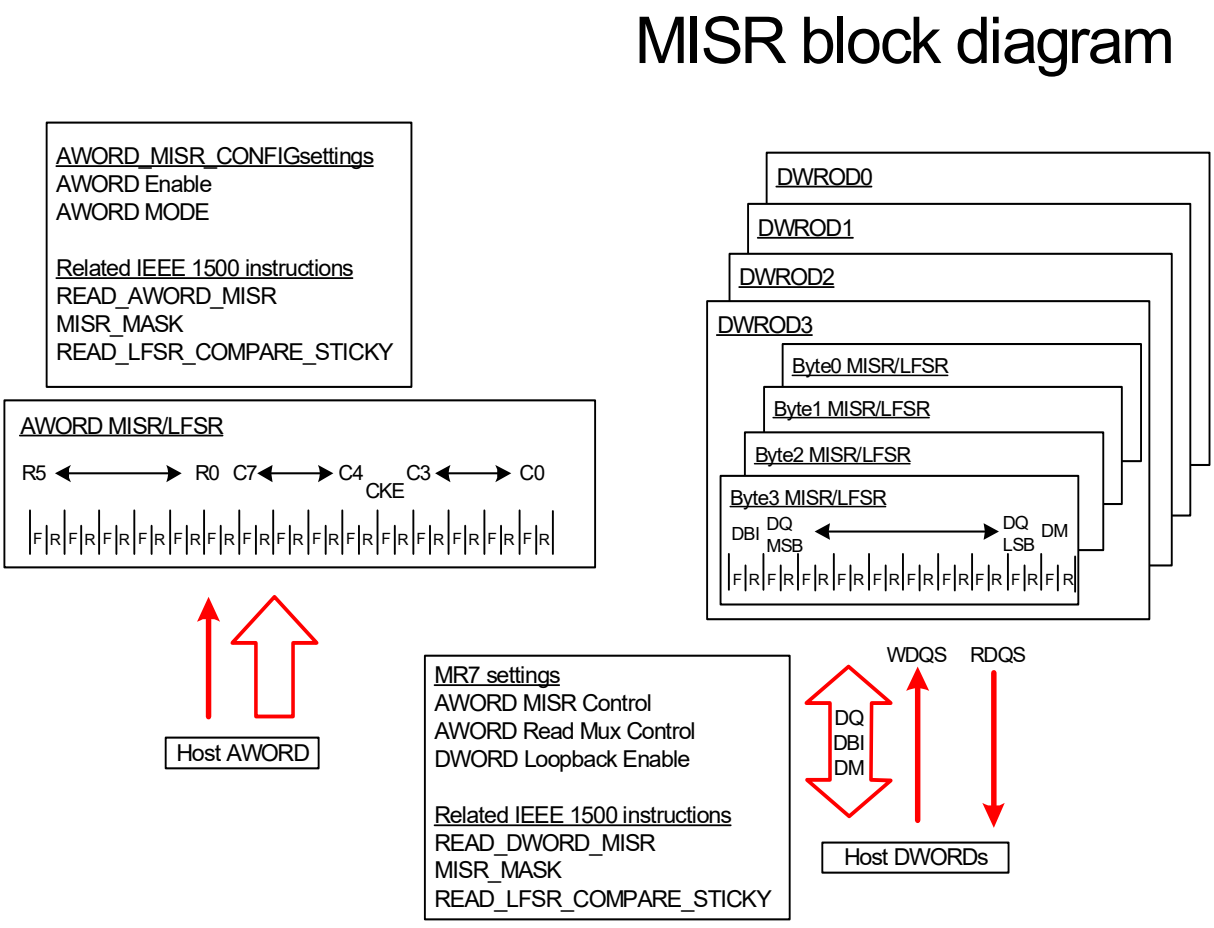


Figure 82. MISR Features Block Diagram

6.9.1. HBM Polynomial Structures

Figure 83 provides an example of a 4-bit Galois type MISR/LFSR structure that implements the following polynomial:

$$f(x) = X^4 + X^3 + 1$$

The example circuit and function table are for illustration only, and this circuit's modes are not fully representative of the actual DWORD and AWORD MISR definitions as outlined below. For example, the circuit shown in Figure 83 implements a reset function, while the AWORD and DWORD MISRs instead implement a preset function, where specific bits are set to logic 1.

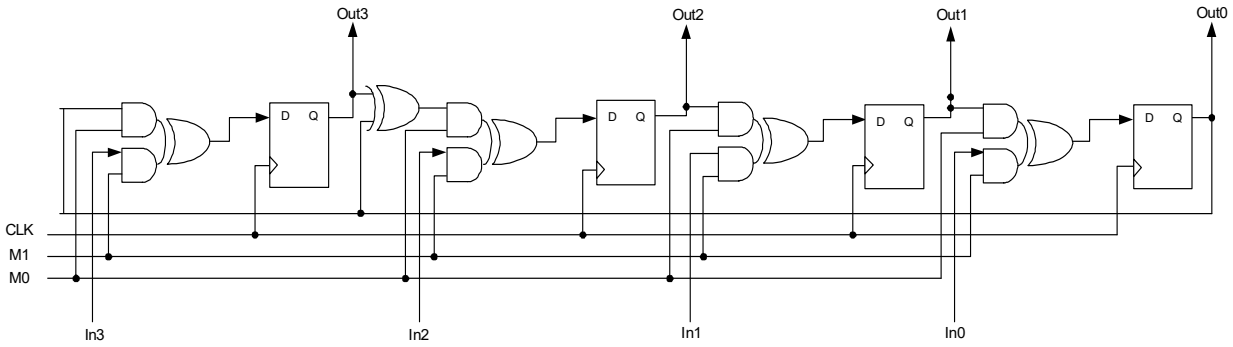


Figure 83. Example of 4 bit MISR-LFSR implementing f(x) = X^4 + X^3 +1

Table 47 - MISR Function Table

M1	M0	Function
0	0	Reset
0	1	LFSR
1	0	Register
1	1	MISR

6.9.1.1. AWORD MISR Polynomial

The AWORD MISR structure is a 30-bit MISR/LFSR with the following polynomial:

$$f(x) = X^{30} + X^{6} + X^{4} + X + 1$$

The AWORD MISR may be serially accessed via the AWORD_MISR IEEE 1500 port instruction. See Table 85 for the AWORD MISR wrapper data register bit order.

6.9.1.2. DWORD MISR Polynomial

The DWORD MISR structure is a 20-bit MISR/LFSR per byte with the following polynomial:

$$f(x) = X^{20} + X^{17} + 1$$

Note that when the DWORD MISRs are accessed via the DWORD_MISR IEEE 1500 port instructions that all of the individual byte MISRs within a channel are concatenated into a 320-bit wrapper data register. See Table 84 for the DWORD MISR bit order.

6.9.2. General Loopback Mode Features and Behavior

This section addresses features and behaviors that generally apply to all of the MISR modes.

a) **Entering the MISR modes** - MISR modes may be entered any time after completing the initialization (see "Initialization"). DWORD MISR modes are controlled via Mode Register 7 (see Table 18), while AWORD MISR modes are controlled via the IEEE 1500 port AWORD_MISR_CONFIG instruction. AWORD and DWORD MISR modes cannot be used simultaneously since the DWORD MISR modes are driven via READ and WRITE commands on the AWORD bus.

b) **Entering and exiting AWORD MISR modes** - HBM allows the AWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization, to enter the AWORD MISR modes on a given channel the host must put the HBM channel into either precharge power-down or self refresh modes. Self refresh mode may be used in order to retain memory content while using the AWORD MISR modes, as needed. Enabling the AWORD MISR modes re-enables the AWORD IO buffers that are normally disabled in power-down and self refresh modes, which may result is increased current draw over the IDD2P, IDD2P0 and IDD6x specifications. If returning to normal operation is not required, the host may assert an initialization sequence per section "Initialization" after operating the AWORD MISR modes. The sequence for entering AWORD MISR modes, and then exiting back to normal operation is as follows:

- •At any time after initializing the HBM enter the all banks idle state.
- •Enter either the Precharge Power-Down state or the Self-Refresh state. CKE = 0 while in these states.
- •Stop toggling CK (CK_t = 0, CK_c = 1).
- •Enable/enter and operate the AWORD MISR modes (AWORD_MISR_CONFIG Enable = 1 - On). Finish these operations with CK stopped (CK_t = 0, CK_c = 1) and CKE = 0.
- •Disable the AWORD MISR modes and follow the "Power-Down (PDE,PDX)" or "Self-Refresh(SRE,SRX)" exit procedures.
- •When using the AWORD MISR modes after tINIT3 within the initialization sequence, power-down or self refresh entry and exit does not apply.

If the DRAM is not required to continue with mission mode operation after AWORD MISR test, there is no requirement on row/column command bus and CKE lane state after loopback test. The AWORD MISR modes (AWORD_MISR_CONFIG Enable bit) can be reset by WRST_n during a subsequent initialization sequence.

c) **Entering and exiting DWORD MISR modes** - HBM allows the DWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization (see "Initialization"), to enter the DWORD MISR modes on a given channel the host must put the HBM channel into the all banks idle, enable the DWORD MISR modes (MR7 Loopback Enable = 1 - Enable; see Table 18), and then enter precharge power-down or self-refresh. Self-refresh may be used in order to retain memory content while using the DWORD MISR modes, as needed. Enabling the DWORD MISR modes before entering precharge power-down or self-refresh keeps the AWORD and DWORD IO buffers enabled, and may result is increased current draw over the IDD2P, IDD2P0 and IDD6x specifications.

Also see items h), k), and n) for related DWORD MISR modes configuration setting. On the column command bus only READ (RD), WRITE (WR), and Column No Operation (CNOP) commands may be issued which operate the DWORD MISR modes, and MR7 MRS commands may be issued to select the DWORD MISR modes. On the row command bus only Row No Operation (RNOP) commands may be issued. The sequence for entering DWORD MISR modes, and then exiting back to normal operation is as follows:

•At any time after initializing the HBM enter the all banks idle state.

•Set all configuration mode registers as needed for use in the DWORD MISR modes (see items h), k), and n)).Set MR7 DWORD Loopback Enable = 1 - Enable, and then wait tMOD.

•Enter either precharge power-down or self-refresh. CKE = 0 while in these states.

•Select and operate the DWORD MISR modes via MR7 settings and sending RD, WR, and CNOP commands. After completing DWORD MISR operations, send CNOP commands.

•Follow the power-down exit (PDX) or self-refresh exit (SRX) procedures,

•Set MR7 DWORD Loopback Enable = 0 - Disable, and then wait tMOD before continuing normal operation.

MRS commands are not supported until after tINIT5 in the initialization sequences; therefore, to configure and control the mode registers for DWORD MISR modes usage after tINIT3 the MODE_REGISTER_DUMP_SET instruction must be used. The sequence for entering and operating the DWORD MISR modes after tINIT3 in the initialization sequence is as follows:

- Start CK with RNOP and CNOP on the command busses, and CKE = 0.
- Using MODE_REGISTER_DUMP_SET sets all configuration mode registers as needed for use in
- the DWORD MISR modes (see items h), k), and n)), set MR7 DWORD Loopback Enable = 1 - Enable, and then wait tMOD.
- Select and operate the DWORD MISR modes via MR7 settings (using MODE_REGISTER_-DUMP_SET) and sending RD, WR, and CNOP commands.
- After completing DWORD MISR operations, send CNOP commands, set MR7 DWORD Loopback Enable = 0 - Disable using MODE_REGISTER_DUMP_SET, then wait tMOD.
- CK clocking may be stopped if desired.
- Proceed to other IEEE 1500 instructions, or proceed with the initialization sequence from Figure 5, time Td.

If the DRAM is not required to continue with mission mode operation after DWORD MISR test, there is no requirement to follow the power-down or self refresh procedures and set MR7 DWORD Loopback Enable = 0 - Disable. The Loopback Enable bit can be reset by a subsequent initialization sequence with RESET_n = LOW.

d) **CKE signal is non-functional in AWORD MISR modes** - The CKE signal is functionally disabled when AWORD MISR modes are enabled (AWORD_MISR_CONFIG Enable = 1 - On). This prevents traffic on the CKE signal from causing the HBM device to exit the power-down or self refresh states during AWORD MISR modes testing.

e) **CKE is handled as an SDR signal in AWORD MISR modes** - The AWORD MISR structure implements a Rise and a Fall bit; however the CKE signal is functionally a single data rate signal. The MISR CKE_F bit has no functional purpose other than being active in MISR compression and LFSR pattern generation.

- In AWORD MISR mode and AWORD Register mode, the CKE signal is only sampled on CK_t rising. The captured CKE state is fed into both the CKE_F and CKE_R bits of the AWORD MISR.
- In AWORD LFSR Compare mode, the CKE signal is only sampled on CK_t rising, and only compared against the LFSR CKE_R bit. The CKE_F bit is not used for comparison.
- For initialization, Preset (AWORD_MISR_CONFIG MODE[2:0] = 000 - Preset) sets the CKE bits to CKE_F=1, CKE_R=0. Setting the MISR value via the AWORD Register mode (AWORD_MISR_ CONFIG MODE[2:0] = 0010 - Register) sets both MISR CKE bits to the value latched on CK_t rising.

f) **Command decode is disabled in AWORD MISR modes** - When AWORD MISR modes are enabled the traffic sent on the AWORD bus is not limited to valid commands. To prevent undefined states and operations, when AWORD MISR modes are enabled (AWORD_MISR_CONFIG Enable = 1 - On), command decoding is disabled.

g) **With lane repairs the MISR bit positions remain with their logical signals** - The MISR bits are associated with their logic signals, not the physical microbumps (see Figure 81). For example, if DQ3 has been repaired (which routes the DQ3 data to the DQ4 microbump) the data received on the DQ4 microbump is routed to the DQ3 Rise and Fall MISR bits. Effectively, the behaviors for all MISR modes are unchanged when Mode 2 lane repairs are active - all 10 bits of the byte are captured in the MISR in the same bit locations, as if no lane repair were active.

h) **HBM DBI, Write Mask, and ECC logic circuits are not functional in the DWORD MISR modes** - The DBI and DM signals are treated as pure data signals. Their raw values are captured, compared, or sent without regard to their normal bus inversion or masking/ECC functional meaning.

- It is required to enable Write DBIac and Read DBIac in MR0 in order to enable the IO buffers on the DBI signals.
- For an HBM that supports ECC, it is required set MR4 ECC Enable = 1 and DM Disable = 1 to enable the IO buffers on the DM signals. For an HBM that does not support ECC, it is required to set MR4 ECC Enable = 0 and DM Disable = 0 to enable the input buffers on the DM signals.
- The host may write DBI encoded or non-encoded data to the HBM. In MISR mode or Register mode, the raw data received from the host well be directly captured (not DBI decoded) to the MISR register.

•For LFSR Compare mode to match, the host must send the LFSR generated raw data on all 10 signals of the byte without write DBI encoding. The HBM will not DBI decode the received data, and thus the host must send the raw LFSR data in order for LFSR Compare to match.

•For LFSR mode, the HBM will generate non-DBI encoded read data.

i) **Mode 1 lane repair handling of the DBI signal** - In a Mode 1 lane repair, the DBI signal is lost from the interface.

•In MISR mode and Register mode, logical zeroes are input into the MISR DBI Rise and Fall bits.

•In LFSR Compare mode, the HBM LFSR will predict data for the DBI signal, which would mis-compare since there is no incoming DBI data. When reading the READ_LFSR_COMPARE_ STICKY register the DBI bit for a lane with a Mode 1 repair will read as a pass (logic zero) to avoid indicating an extraneous error.

j) **DWORD read path parity traffic generation** - In DWORD read LFSR mode, the HBM parity logic is not active and the MR0 DQ Bus Read Parity settings has no effect. To generate traffic on the DWORD parity signal a copy of a nearby DQ signal is produced on the Parity signal. Logical signals DQ2, DQ34, DQ66 and DQ98 are sent on the respective DWORD block parity signals, irrespective of any lane repairs. The parity signals are driven with the DQ data without any additional cycle delay - effectively with Parity Latency = 0. A suggested host-side implementation is to use signature register circuits for checking the validity of the received parity signal. When reading data back using MR7 DWORD Read Mux Control (see "DWORD Read Register mode"), the parity signal output is unspecified.

k) **AWORD and DWORD write parity checking** - In AWORD and DWORD Register mode, MISR mode, and LFSR Compare mode the HBM parity evaluation logic is active and outputs results on AERR after tPARAC and DERR after tPARDQ, respectively (if enabled in MR0, see Table 9). The MR4 Parity Latency setting (see Table 15) must be set to a vendor implementation-specific supported PL value, which may be interface speed specific. The HBM device will process write parity per the PL setting and protocol, including any required additional WDQS cycles. A suggested host-side implementation is to use signature register circuits for checking the correctness of the AERR and DERR signals. It is also suggested that the host generate data on the DWORD Parity signals in order to exercise these signal paths and logic.

l) **Preset state AAAAAh and 2AAAAAAAh** - The Preset state for the DWORD MISR registers is AAAAAh, which initializes the Rise bit for each signal to 1'b0 and the Fall bit to 1'b1. This is a useful state for producing an alternating 0/1/0/1 pattern on all 10 bits associated with a DWORD byte when put into DWORD read Register mode (burst length 4 example). This basic pattern may be used by the host for RDQS eye centering. The AWORD MISR register is also preset to the same 0/1 pattern (2AAAAAAAh) for implementation consistency; although the AWORD cannot be enabled to drive this data pattern back to the host. Any non-zero initialization pattern is sufficient for all of the MISR modes; however, an initial pattern of all zeroes is a stuck-at-zero state for the DWORD LFSR mode. The Preset state may be overridden using the Write Register modes (see "AWORD and DWORD Write Register modes").

m)**DWORD MISR registers are optionally writeable via IEEE 1500** - Optionally, an HBM implementation may permit setting the values of the DWORD MISR registers using the DWORD_ MISR IEEE 1500 port instruction. This feature enables setting alternate seed values, usually for the DWORD Read Register mode (see "DWORD Read Register mode").

n) **The DWORD MISR modes operate only in the Legacy or Pseudo-channel mode that the given HBM DRAM design supports -**READ and W For a Legacy mode device, all 4 DWORDs respond to the column commands, exactly as in mission mode. For a PC mode device DWORDs 0 and I respond to PC0 column commands and DWORDs 2 and 3 respond to PC1 column commands, exactly as in mission mode.

o) **DWORD read and write latencies and burst length must be set properly** - READ and WRITE commands are used to generate DWORD MISR modes traffic. Normal mode DWORD read and write protocol is followed using the latency and burst length settings, as supported by the operating frequency being used.

p) **DWORD Write preamble clocks adhere to the normal protocol** - For DWORD write MISR modes (Register mode, MISR mode, and LFSR Compare mode), the host is expected to send WDQS pre-amble clocks, and the HBM samples the DWORD data, consistent with the write protocols defined in the section entitled "Write Command (WR, WRA)"

q) **DWORD Read preamble and post-amble clocks adhere to the normal protocol** - For DWORD Read LFSR mode, and when returning data with the MR7 DWORD Read Mux Control options, the HBM will produce RDQS preamble and postamble clocks, and send DWORD data, consistent with the read protocols defined in the section entitled "Read Command (RD,RDA)".

r) **AWORD MISR modes preamble clock filter** - In the AWORD MISR modes, the host is expected to stop CK toggling, enable the desired AWORD MISR mode, and then start sending CK toggles and AWORD data. To avoid timing impairment on the CK startup cycle, the HBM will treat the first received CK cycle as a preamble clock cycle and not process the data on the AWORD signals into the MISR or Register, nor compare them in LFSR Compare mode. The first clock cycle filter circuit is enabled by setting AWORD_MISR_CONFIG MODE = 3'b000 - Preset. The first data sampled by the HBM is on the second CK clock cycle. Only the very first CK clock cycle will be filtered - if the host were to stop and restart CK clocking while remaining in an AWORD MISR mode (without applying another Preset), the AWORD data will be sampled on the startup clock cycle, with possible CK edge timing impairment.

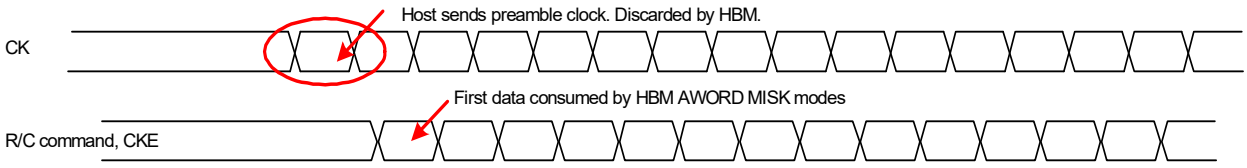


Figure 84. AWORD MISR Modes Preamble Clock Filter Behavior

r) **Cycles processed in the MISR modes** - AWORD MISR modes rely on stopping CK clocks before and after the test sequence. All AWORD cycles sent to the HBM after the filtered preamble clock cycle are processed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode), including the last cycle before CK is stopped. For DWORD MISR modes, all valid data cycles written to the HBM are pro-cessed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode) while the DWORD MISR modes are enabled, consistent with the DWORD write protocol and write latency setting. Data pin states during preamble and post-amble cycles are not processed into the MISR. For example, if 10 non-seamless Burst Length = 4 write operations are sent to the HBM in DWORD MISR mode a total of 40 data bit times (UI) will be processed into the MISR.

6.9.3. AWORD and DWORD Write MISR Modes

When the AWORD or DWORD MISR modes are active, the data on the AWORD or DWORD data signals is received based on the CK or WDQS clocks respectively, and compressed in the MISR circuits. The host is in complete control of the number of data cycles that are sent, and if successfully received by the HBM the values captured in the respective MISRs will be repeatable and deterministic.

The IEEE 1500 MISR_MASK instruction may be used for forcing individual MISR inputs to logic 0 in the process of searching for a bad host-to-HBM signal interconnect. Masking a given signal has the effect of forcing it to a known state as input the MISR. The host is suggested to iterate on masking individual signals and checking for expected MISR signatures. Alternately, see "AWORD and DWORD Write LFSR Compare modes".

6.9.3.1. Test Method for AWORD (Write) MISR Mode

a) After the required HBM initialization, the host asserts either precharge power-down or self-refresh mode (CKE = 0) and stops sending CK clocks to the HBM (CK_t = 0, CK_c = 1).

b) Initialize the AWORD MISR by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 3'b000 - Preset. The Preset operation also enables the preamble clock filter circuit.

c) Enable the AWORD MISR mode by setting AWORD_MISR_CONFIG Mode = 3'b011 - MISR mode.

d) The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM clocks the received data into the AWORD MISR and evaluates parity, if enabled. The ending clock state applied by the host is CK_t = 0, CK_c = 1.

e) The host reads the MISR content via the IEEE 1500 AWORD_MISR instruction.

6.9.3.2. Test Method for DWORD Write MISR mode

a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset.

b) Enable DWORD MISR mode by setting MR7 DWORD MISR Control = 'b011 - MISR mode.

c) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM clocks the received data into the DWORD MISRs and evaluates parity, if enabled.

d) The host reads the MISR content via the IEEE 1500 DWORD_MISR instruction. The MISR content is also readable via the functional interface (see "DWORD Read Register mode").

6.9.4. AWORD and DWORD Write Register modes

When the AWORD or DWORD Register modes are active, the data on the AWORD or DWORD data signals is received based on the CK or WDQS clocks respectively, and stored directly into the respective MISR registers without compression. Effectively the MISR register operates as a 2-bit storage register. On CK_t rising or WDQS_t rising the signal states on the AWORD or DWORD bus respectively are stored in the Rising bits within the MISR registers, and on the rising edges of CK_c and WDQS_c the bus signal states are stored in the Falling bits within the MISR registers. If the host sends multiple DDR cycles to the HBM, the MISRs will contain the last DDR cycle data, if successfully received by the HBM.

The Register modes are intended for basic, quick link testing and training, and for initializing the DWORD MISR seed values.

6.9.4.1. Test method for AWORD (Write) Register mode

a) After the required HBM initialization, the host asserts either Precharge Power-Down or Self-Refresh mode (CKE = 0) and stops sending CK clocks to the HBM (CK_t = 0, CK_c = 1).

b) Initialize the AWORD MISR by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 3'b000 - Preset. The Preset operation enables the preamble clock filter circuit.

c) Enable the AWORD Register mode by setting AWORD_MISR_CONFIG MODE = 3'b010 - Register mode.

d)The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM clocks the raw received data into the AWORD MISR register without MISR compression and evaluates parity, if enabled. The ending clock state applied by the host is CK_t = 0, CK_c = 1. The last clocked DDR cycle data is retained in the AWORD MISR register.

e)The host reads the MISR content via the IEEE 1500 AWORD_MISR instruction.

Note that the AWORD write register mode cannot practically be used to apply an alternate seed value into the AWORD MISR register. In the above procedure in step d) the preamble clock filter circuit is exercised and cleared. At this point while it is allowed for the host to then stop sending AWORD cycles, set the AWORD_MISR_CONFIG MODE to MISR mode or LFSR Compare mode, and then send additional AWORD cycles, there may be timing impairment for the beginning of the second set of AWORD cycles. The preamble clock filter circuit cannot be re-enabled for these additional AWORD cycles without applying the AWORD MISR Preset function, which would also overwrite the alternate seed value applied by the AWORD write register operation. There is no expected application value for using an alternate MISR seed value for the AWORD MISR functions since the AWORD bus is receive-only.

6.9.4.2. Test Method for DWORD Write Register mode

a) Enable DWORD Register mode by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b010 - Register mode. A Preset is not required prior to using Register mode.

b) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM clocks the raw received data into the DWORD MISR

registers without MISR compression and evaluates parity, if enabled. The last clocked DDR cycle data is retained in the DWORD MISR registers.

c) The host reads the MISR content via the IEEE 1500 DWORD_MISR instruction. The MISR content is also readable via the functional interface (see "DWORD Read Register mode").

6.9.5. DWORD Read Register mode

The content of various DWORD MISR mode related registers may be read over the functional interface, assuming that the read path with the host is properly trained (or used for read path training). The MR7 DWORD Read Mux Control bit field is used to select the data source. The host issues read commands and the HBM responds following the read command protocol (such as read latency and burst length) and timing (such as pre and post-amble clocks) per section "Read Command (RD,RDA)".

Intended uses for the various read data sources include the following:

- Reading the sticky error bits after an LFSR Compare mode test sequence (DWORD Read Mux Control = 2'b11 - Return LFSR_COMPARE_STICKY) - Sticky error data is a single data bit per signal and is output as static values on the interface for the full read burst length. Note that support for reading the DWORD LFSR Compare sticky error data over the functional interface is optional.

  Note that when using the LFSR mode (see "DWORD Read LFSR mode") set the DWORD Read Mux Control = 2'b01 - Return data from MISR registers.

- Reading a basic clock pattern on all or select signals for DWORD read link training (DWORD Read Mux Control = 2'b01 - Return data from MISR registers) - Which signals toggle may be set with the Preset mode or a DWORD Register write (see "AWORD and DWORD Write Register modes").

- Reading the MISR registers final values at the end of a MISR mode test sequence (DWORD Read Mux Control = 2'b01 - Return data from MISR registers) - The results of a MISR mode test sequence may be read back on the functional interface, or via the IEEE 1500 port DWORD_MISR instruction.

- Reading what has been captured in the DWORD receive path samplers - Independent from the data in the MISR registers, the last DDR cycle captured in the DWORD receive path functional latches may be read back using DWORD Read Mux Control = 2'b10 - Return data from Rx path sampler.

6.9.5.1. Test Method for DWORD Read Register mode

a) Enable the test mode and select the desired read-back register by setting MR7 DWORD Loopback Enable = 1'b1 - Enable, DWORD MISR Control = 3'b010 - Register mode, and DWORD Read Mux Control = one of the defined register sources.

b) The host sends one or more DWORD read commands. The HBM responds following the read latency and burst length setting and following the normal read protocol.

6.9.6. DWORD Read LFSR mode

When in DWORD Read LFSR mode, the HBM generates DWORD data from the LFSR in response to read commands issued by the host. LFSR data is generated consistent with only the valid UIs of the read protocol. Read Preamble and post-amble RDQS clocks are generated consistent with the read protocol. The first data cycle generated will be the LFSR initial state, based on Preset or an alternate seed value if loaded.

Note that there is no AWORD LFSR mode since the AWORD bus cannot source data to the host.

6.9.6.1. Test Method for DWORD Read LFSR mode

a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset. Optionally, load the DWORD MISR registers with an alternate seed value via the functional interface (see "AWORD and DWORD Write Register modes").

b) Enable DWORD LFSR mode by setting MR7 DWORD MISR Control = 3'b001 - LFSR mode and DWORD Read Mux Control = 2'b01 - Return data from MISR registers.

c) The host sends one or more DWORD read commands. The HBM responds following the read latency and burst length setting and following the normal read protocol, with data produced from the LFSR. A suggested host-side implementation is to use signature register circuits for checking the validity of the received data.

6.9.7. AWORD and DWORD Write LFSR Compare modes

The LFSR Compare modes enable direct identification of failing signal connections between the Host and HBM. It is assumed that the Host implements LFSR data generators that match the lengths and polyno-mials of the HBM LFSRs, and that the Host and HBM LFSRs start and run in synch. The LFSRs generate DDR data on each signal, and the compare circuitry checks for matching data for each data unit interval (UI). Any mismatch between the data received at the HBM inputs (based on the respective CK or WDQS clocking) and the data predicted by the HBM LFSR will set the sticky error bit for the respective signals. The first data cycle expected from the host and compared by the HBM will be the LFSR initial state, based on Preset or an alternate seed value if loaded.

Once a miscompare is found on a signal, its sticky error bit is set (1'b1) for the remainder of the test sequence. The sticky error bits may be read via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction or via the functional interface (optional, see "DWORD Read Register mode"). AWORD sticky error bits are only readable via the IEEE 1500 port. The sticky error bits are reset (1'b0) via the MR7 DWORD MISR Control = 3'b000 - Preset, or IEEE 1500 AWORD_MISR_CONFIG MODE = 3'b000 - Preset.

Note that with Mode 1 repairs on a given byte, the DBI sticky error bit will read as zero within the READ_LFSR_COMPARE_STICKY WDR (see item i) in section entitled "General Loopback Mode Features and Behavior").

Figure 85 illustrates the system-level configuration for LFSR Compare mode.

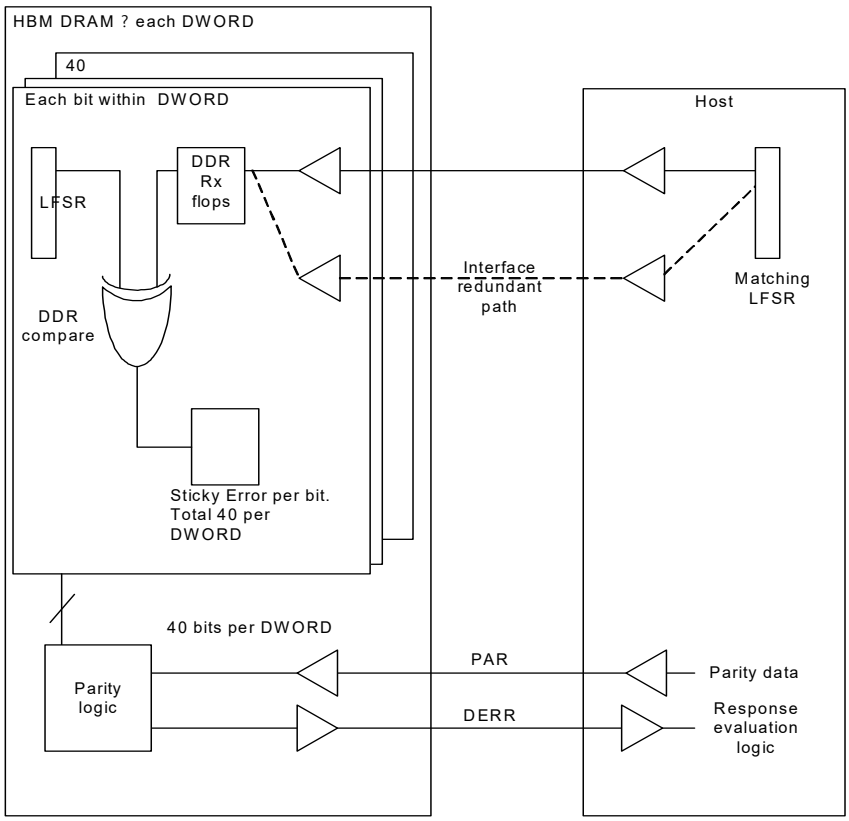


Figure 85. LFSR Compare Mode Block Diagram

Note that data produced on the DWORD Parity signals from the host to the HBM is an implementation suggestion for exercising the parity signal paths and HBM input timing and logic. The host-side implementation for parity signal generation is not specified. This figure also illustrates that a host-driven logical signal is compared with the matching logical signal data by the HBM compare circuit, regardless of any active lane repairs which may shift the physical signal routing. The AWORD LFSR Compare circuit matches the DWORD circuit except for the non-existent Parity signals.

6.9.7.1. Test method for AWORD (Write) LFSR Compare mode

a) After the required HBM initialization, the host asserts either Precharge Power-Down or Self-Refresh mode (CKE = 0) and stops sending CK clocks to the HBM (CK_t = 0, CK_c = 1).

b) Initialize the AWORD MISR (LFSR) register by setting the AWORD_MISR_CONFIG Enable = 1'b1 - On and AWORD_MISR_CONFIG MODE = 3'b000 - Preset. The Preset operation also clears the AWORD per-signal sticky error bits and enables the preamble clock filter circuit. The host-side LFSR data generator should also be initialized to the same value.

c) Enable the AWORD LFSR Compare mode by setting AWORD_MISR_CONFIG MODE = 3'b100 - LFSR Compare mode.

d) The host sends two or more CK clock cycles with LFSR-generated data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM LFSR predicts expected AWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled. The ending clock state applied by the host is CK_t = 0, CK_c = 1.

e) The host reads the Sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction.

6.9.7.2. Test Method for DWORD Write LFSR Compare mode

a) Initialize the DWORD LFSR (MISR) registers by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b000 - Preset. The Preset operation also clears the DWORD per-signal sticky error bits. The host-side LFSR data generator should also be preset/initialized to the same value.

b) Enable DWORD LFSR Compare mode by setting MR7 DWORD MISR Control = 3'b100 - LFSR Compare mode.

c) The host sends one or more DWORD write cycles with LFSR-generated data on the DWORD signals following the write latency and burst length setting and following the normal write protocol. The HBM LFSRs predict expected DWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled.

d) The host reads the sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ_LFSR_COMPARE_STICKY instruction. The sticky error bits are also readable via the functional interface (optional, see "DWORD Read Register mode").

7. Operating Conditions

7.1. Absolute Maximum DC Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicates in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 48 - Absolute Maximum DC Rating

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DDC} relative to V_{SS}	V_{DDC}	-0.3 to 1.5	V	1
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.3 to 1.5	V	1
Voltage on V_{PP} relative to V_{SS}	V_{PP}	-0.3 to 3.0	V	1
Storage Temperature	$T_{STORAGE}$	-40 to 100	°C	2

Notes 1. See "HBM Power-up and Initialization Sequence" for relationship between power supplies.
Notes 2. Storage temperature is the case surface temperature on the center/top side of the HBM device. For the measurement conditions, please refer to JESD51-2 standard.

7.2. Recommended DC Operating Condition

Table 49 Specifies the operating condition for VDDC, VDDQ and VPP supply voltages

Table 49 - Recommended DC Operating Condition

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Core Supply Voltage	V_{DDC}	1.14	1.2	1.26	V	1,2
Supply Voltage for I/O	V_{DDQ}	1.14	1.2	1.26	V	1,2
Pump Voltage	V_{PP}	2.375	2.5	2.75	V	2

Notes 1. VDDC and VDDQ supplies are independent and must not be tied together internally on the HBM DRAM. HBM DRAM must tolerate seperate VDDC and VDDQ power supply regulators.
Notes 2. The voltage ranges are defined at the HBM DRAM micropillars. DC bandwidth is limited to 20 MHz.

7.3. Operating Temperature

Table 50 - Operating Temperature

Parameter		Symbol	Minimum	Maximum	Unit	Notes
Operating Temperature	Standard	T_N	0	84	°C	1
Operating Temperature	Extended1	T_{E1}	85	94	°C	1, 2
Operating Temperature	Extended2	T_{E2}	95	105	°C	1, 2

Notes 1. Operating Temperature is any dimensional points of the HBM core die.
Notes 2. Optional and the HBM DRAM may require additional Refresh cycle.

8. Electrical Characteristics

8.1. Leakage Current

Table 51 - Input Leakage Current

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Input Leakage Current For R[5:0], C[7:0], CKE, CK_t, CK_c. Any input 0 V ≤ VIN ≤ VDDQ. (All inputs pins including IEEEP1500 not under test = 0 V)	I_L	-5	5	uA	

8.2. Capacitance

Table 52 - Input Capacitance

Parameter	Symbol	1 Gbps		2 Gbps		Unit	Notes
		Min	Max	Min	Max		
HBM Pad Capacitance - DQs, DBI, DM, PAR	C_{IO}	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Row & Column Address	C_{ADDR}	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Read Strobe	C_{RDQS}	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Write Strobe	C_{WDDQ}	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Clock	C_{CK}	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - DERR, AERR	C_{ERROR}	-	0.6	-	0.4	pF	1
Notes 1. This parameter is not subject to production test. It is verified by design and characterization. The measurement method is TBD.							

8.3. AC & DC Characteristics

Table 53 - Input Receiver Voltage Level Specification

Parameter	Symbol	Min	Max	Unit	Note
Input HIGH Voltage	VIH	0.7*VDDQ		V	1
Input LOW Voltage	VIL		0.3*VDDQ	V	1
Input HIGH Voltage for RESET_n and WRST_n	VIHR	0.8 * VDDQ	-	V	
Input LOW Voltage for RESET_n and WRST_n	VILR	-	0.2 * VDDQ	V	
Notes 1. CMOS input receivers enabled (default mode of operation). For CK_t, CK_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS_t, WDQS_c, WRCK, SELECTWIR, SHIFTWR, CAPTUREWR, UPDATEWR and WSI inputs. Notes 2. VREF based input receiver enabled (optional, see MR15). For CK_t, CK_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS_t and WDQS_c inputs.					

8.4. Transmit drive currents

HBM drivers have programmable current settings with 20% accuracy. Driver targets, in mA are shown in Table 54 below.

Table 54 - Transmit Driver Current Specification

Nominal (mA)	Min (mA)	Max (mA)	Note
6.0	4.8	7.2	
9.0	7.2	10.8	
12.0	9.6	14.4	
15.0	12.0	18.0	
18.0[1]	14.4	21.6	1
Notes 1. Implementation support limited to 2 Gbps target EOL data rate products.			

8.5. Output Timing Reference Load

C = CTOTAL - CIO; where CTOTAL = 2.4 pF.

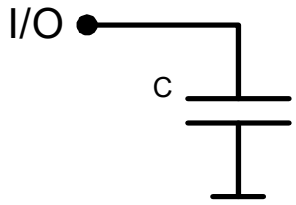


Figure 86. Timing Reference Load

8.6. Output Voltage Level

Table 55 - Output Voltage Level

Parameter	Symbol	Min	Max	Unit	Notes
Ouput HIGH Voltage	V_{OH}	$0.7*_{VDDQ}$		V	
Output LOW Voltage	V_{OL}		$0.3*V_{DDQ}$	V	

8.7. Output Rise and Fall time

$T_R = \{ C_{TOTAL} * (V_{OH} - V_{OL}) \} / I$; $T_F = \{ C_{TOTAL} * (V_{OH} - V_{OL}) \} / I$;

Where I = Transmit Drive Current in mA.

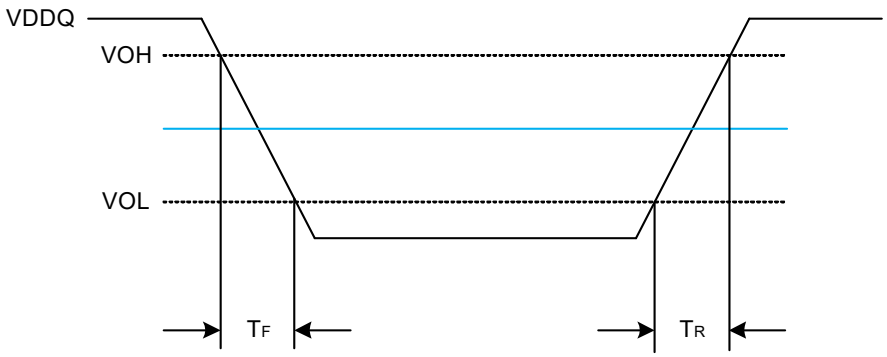


Figure 87. Output Rise and Fall Definition

8.8. Overshoot / Undershoot

Table 56 - Overshoot/Undershoot Specification for R[5:0], C[7:0], DATA[127:0], DM[15:0], DBI[15:0]

Parameter	1.0Gbps(BOL)	2.0Gbps(EOL)	Unit
Maximum peak amplitude allowed for overshoot area	0.35	0.35	V
Maximum peak amplitude allowed for undershoot area	0.35	0.35	V
Maximum overshoot area above VDDQ	0.18	0.09	V-ns
Maximum undershoot area below VSSQ	0.18	0.09	V-ns

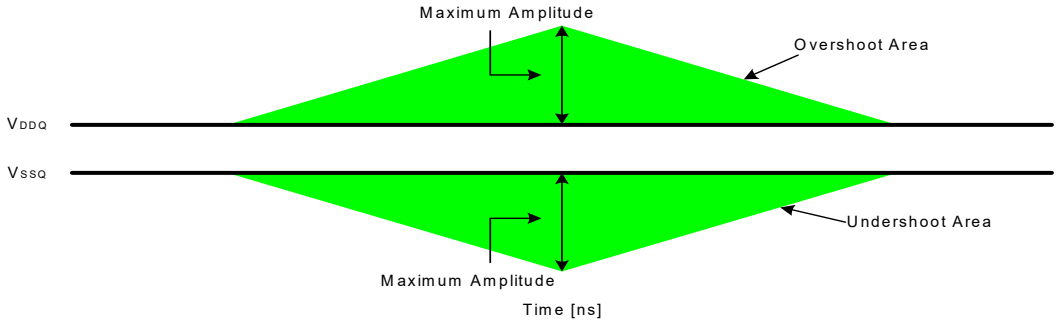


Figure 88. Overshoot, Undershoot Definition

9. IDD Specification

9.1. IDD and IDDP Specification Parameters and Test Conditions

This chapter defines operating current measurement conditions and loop pattern.

- I_{DD} currents are measured as time-averaged currents with all V_{DDC} microbumps of the HBM device under test tied together.
- I_{DDP} currents use the same definitions as I_{DD} except that the current on the V_{PP} supply is measured. All VPP microbumps of the HBM device under test tied are together for I_{DDP} current measurements.
- I_{DDQ} currents are not included in the measurements. Instead, DRAM vendors shall provide simulated values using the IDD4R measurement-loop pattern as defined in Table 61 and Table 62
- I_{DD} and I_{DDP} measurements are taken with all channels of the HBM device simultaneously executing the same pattern. However, I_{DD} values in the this datasheet is given per channel.

For I_{DD} measurements, the following definitions apply:

- "0" and "LOW" is defined as V_{IN} <= V_{IL}(max);
- "1" and "HIGH" is defined as V_{IN} >= V_{IH}(min);
- WL and RL are programmed to appropriate values;
- DBI(ac) is enabled for Reads and Writes;
- DM and parity are disabled;
- ECC is enabled if supported by the device;
- Bank groups are enabled if required for device operation at tCK(min);
- Each data byte consists of eight DQs, one DM and one DBI pin;
- CNOP/RNOP commands and all address inputs stable during idle command cycles;
- Some I_{DD} Measurement-Loop pattern use high order address bits RA13..RA15 and CA6 which are not defined for all densities. In those cases the respective undefined address bit(s) shall be kept LOW.
- Basic I_{DD} Measurement Conditions are described in Table 57.
- I_{DD} Measurements are done after properly initializing the HBM device. This includes the pre-load of the memory array with data pattern used with IDD4R measurements.
- The I_{DD} Measurement-Loop patterns shall be executed at least once before actual I_{DD} measurement is started.
- For timing parameters used with I_{DD} Measurement-Loop pattern: nRC = t_{RC}/t_{CK}; n_{RAS} = t_{RAS}/t_{CK}, nRP = t_{RP}/t_{CK}, nRFC = t_{RFC}/t_{CK}. If not already an integer, round up to the next integer.

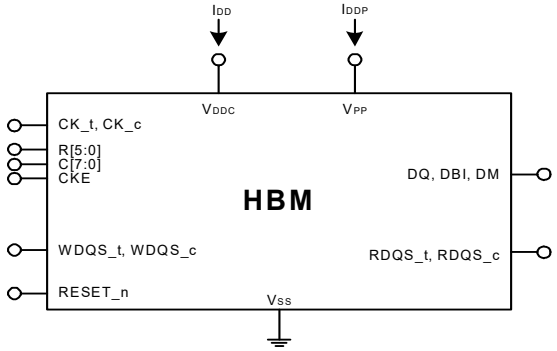


Figure 89. Measurement Setup for IDD and IDDP Measurements

Table 57 - Basic IDD measurement conditions

Parameter/Condition	Symbol
One Bank Activate Precharge Current: $t_{CK} = t_{CK}(min)$; t_{RC}, t_{RAS} and t_{RP} as defined in Table 58; CKE is HIGH; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW; bank and row addresses with ACT and PRE commands as defined in Table 59 or Table 60	I_{DD0}
Precharge Power-down Current: $t_{CK} = t_{CK}(min)$; all banks are idle; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD2P}
Precharge Power-down Current with clock stop: CK_t is LOW; CK_c is HIGH; all banks are idle; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD2P0}
Precharge Standby Current: $t_{CK} = t_{CK}(min)$; all banks are idle; CKE is HIGH; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD2N}
Active Power-down Current: $t_{CK} = t_{CK}(min)$; one bank is active; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD3P}
Active Power-down Current with clock stop: CK_t is LOW; CK_c is HIGH; one bank is active; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD3P0}
Active Standby Current: $t_{CK} = t_{CK}(min)$; one bank is active; CKE is HIGH; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I_{DD3N}
Read Burst Current: $t_{CK} = t_{CK}(min)$; CKE is HIGH; all banks activated; continuous read burst across bank groups as defined in Table 61 or Table 62 I_{OUT} = 0mA	I_{DD4R}
Write Burst Current: $t_{CK} = t_{CK}(min)$; CKE is HIGH; all banks activated; continuous write burst across bank groups as defined in Table 63 or Table 64	I_{DD4W}
All-bank Refresh Average Current: $t_{CK} = t_{CK}(min)$; $t_{RFC} = t_{REFI}(min)$; CKE is HIGH between valid commands; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW	I_{DD5A}
All-bank Refresh Burst Current: $t_{CK} = t_{CK}(min)$; t_{RFC} as defined in Table 58; CKE is HIGH between valid commands; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW	I_{DD5B}
Self Refresh Current: CKE is LOW; R and C inputs are LOW; DQ, DM and DBI inputs are LOW	I_{DD6x}
Reset Low Current: RESET_n is LOW; CK_t, CK_c, WDQS_t, WDQS_c and CKE are LOW; R and C inputs are LOW; DQ, DM and DBI inputs are LOW; Note: RESET Low current reading is valid once power is stable and RESET_n has been LOW for at least 1ms	I_{DD8}

Table 58 - Timings used for IDD Measurement-Loop pattern

Parameters		Value	Unit
t_{RC}		45	ns
t_{RAS}		29	ns
t_{RP}		16	ns
t_{RFC}	4 Gb	260	ns
	8 Gb	350	ns
Note DRAM vendors may decide to use different values for t_{RAS} and t_{RP}; however, $n_{RAS} + n_{RP} = n_{RC}$ must be achieved.			

Table 59 - IDD0 Measurement-Loop Pattern - Legacy Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)
0	0	ACT	CNOP	00h	05555h	N/A
	1		CNOP			N/A
	2	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRAS)				
	nRAS + 1	PRE	CNOP	00h	N/A	N/A
	nRAS + 2	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRC -1)				
1	nRC	repeat sub-loop 0 pattern until cycle (2*nRC -1); use BA = 05h and RA = 0AAAAh instead				
2	2*nRC	repeat sub-loop 0 pattern until cycle (3*nRC -1); use BA = 02h and RA = 05555h instead				
3	3*nRC	repeat sub-loop 0 pattern until cycle (4*nRC -1); use BA = 07h and RA = 0AAAAh instead				
4	4*nRC	repeat sub-loop 0 pattern until cycle (5*nRC -1); use BA = 01h and RA = 05555h instead				
5	5*nRC	repeat sub-loop 0 pattern until cycle (6* nRC -1); use BA = 06h and RA = 0AAAAh instead				
6	6*nRC	repeat sub-loop 0 pattern until cycle (7* nRC -1); use BA = 03h and RA = 05555h instead				
7	7*nRC	repeat sub-loop 0 pattern until cycle (8* nRC -1); use BA = 04h and RA = 0AAAAh instead				
8 to 15	for 16-bank devices: repeat sub-loops 0 to 7 pattern; use BA3 = 1 instead					

Table 60 - IDD0 Measurement-Loop Pattern - Pseudo Channel Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)
0	0	ACT - PC0	CNOP	00h	05555h	N/A
	1		CNOP			N/A
	2	ACT - PC1	CNOP	00h	05555h	N/A
	3		CNOP			N/A
	4	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRAS)				
	nRAS + 1	PRE-PC0	CNOP	00h	N/A	N/A
	nRAS + 2	RNOP	CNOP	N/A	N/A	N/A
	nRAS + 3	PRE-PC1	CNOP	00h	N/A	N/A
	nRAS + 4	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRC -1)				
1	nRC	repeat sub-loop 0 pattern until cycle (2*nRC -1); use BA = 05h and RA = 0AAAAh instead				
2	2*nRC	repeat sub-loop 0 pattern until cycle (3*nRC -1); use BA = 02h and RA = 05555h instead				
3	3*nRC	repeat sub-loop 0 pattern until cycle (4*nRC -1); use BA = 07h and RA = 0AAAAh instead				
4	4*nRC	repeat sub-loop 0 pattern until cycle (5*nRC -1); use BA = 01h and RA = 05555h instead				
5	5*nRC	repeat sub-loop 0 pattern until cycle (6* nRC -1); use BA = 06h and RA = 0AAAAh instead				
6	6*nRC	repeat sub-loop 0 pattern until cycle (7* nRC -1); use BA = 03h and RA = 05555h instead				
7	7*nRC	repeat sub-loop 0 pattern until cycle (8* nRC -1); use BA = 04h and RA = 0AAAAh instead				
8 to 15	for 16-bank devices: repeat sub-loops 0 to 7 pattern; use BA3 = 1 instead					

Table 61 - IDD4R Measurement-Loop Pattern - Legacy Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)	Data Pattern (1 Byte)
0	0	RNOP	READ	00h	05555h	0101010b	00h, 55h
	1	RNOP	READ	05h	0AAAAh	1010101b	FFh, AAh
	2	RNOP	READ	02h	05555h	0101010b	00h, 55h
	3	RNOP	READ	07h	0AAAAh	1010101b	FFh, AAh
	4	RNOP	READ	01h	05555h	0101010b	00h, 55h
	5	RNOP	READ	06h	0AAAAh	1010101b	FFh, AAh
	6	RNOP	READ	03h	05555h	0101010b	00h, 55h
	7	RNOP	READ	04h	0AAAAh	1010101b	FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						

Table 62 - IDD4R Measurement-Loop Pattern - Pseudo Channel Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)	Data Pattern (1 Byte)
0	0	RNOP	READ - PC0	00h	05555h	0101010b	00h, 55h, FFh, AAh
	1	RNOP	READ - PC1	00h	05555h	0101010b	00h, 55h, FFh, AAh
	2	RNOP	READ - PC0	05h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	3	RNOP	READ - PC1	05h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	4	RNOP	READ - PC0	02h	05555h	0101010b	00h, 55h, FFh, AAh
	5	RNOP	READ - PC1	02h	05555h	0101010b	00h, 55h, FFh, AAh
	6	RNOP	READ - PC0	07h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	7	RNOP	READ - PC1	07h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	8	RNOP	READ - PC0	01h	05555h	0101010b	00h, 55h, FFh, AAh
	9	RNOP	READ - PC1	01h	05555h	0101010b	00h, 55h, FFh, AAh
	10	RNOP	READ - PC0	06h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	11	RNOP	READ - PC1	06h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	12	RNOP	READ - PC0	03h	05555h	0101010b	00h, 55h, FFh, AAh
	13	RNOP	READ - PC1	03h	05555h	0101010b	00h, 55h, FFh, AAh
	14	RNOP	READ - PC0	04h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	15	RNOP	READ - PC1	04h	0AAAAh	1010101b	00h, 55h, FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						

Table 63 - IDD4W Measurement-Loop Pattern - Legacy Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)	Data Pattern (1 Byte)
0	0	RNOP	WRITE	00h	05555h	0101010b	00h, 55h
	1	RNOP	WRITE	05h	0AAAAh	1010101b	FFh, AAh
	2	RNOP	WRITE	02h	05555h	0101010b	00h, 55h
	3	RNOP	WRITE	07h	0AAAAh	1010101b	FFh, AAh
	4	RNOP	WRITE	01h	05555h	0101010b	00h, 55h
	5	RNOP	WRITE	06h	0AAAAh	1010101b	FFh, AAh
	6	RNOP	WRITE	03h	05555h	0101010b	00h, 55h
	7	RNOP	WRITE	04h	0AAAAh	1010101b	FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						

Table 64 - IDD4W Measurement-Loop Pattern - Pseudo Channel Mode

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA)	Row Address (RA)	Col Address (CA)	Data Pattern (1 Byte)
0	0	RNOP	WRITE - PC0	00h	05555h	0101010b	00h, 55h, FFh, AAh
	1	RNOP	WRITE - PC1	00h	05555h	0101010b	00h, 55h, FFh, AAh
	2	RNOP	WRITE - PC0	05h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	3	RNOP	WRITE - PC1	05h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	4	RNOP	WRITE - PC0	02h	05555h	0101010b	00h, 55h, FFh, AAh
	5	RNOP	WRITE - PC1	02h	05555h	0101010b	00h, 55h, FFh, AAh
	6	RNOP	WRITE - PC0	07h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	7	RNOP	WRITE - PC1	07h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	8	RNOP	WRITE - PC0	01h	05555h	0101010b	00h, 55h, FFh, AAh
	9	RNOP	WRITE - PC1	01h	05555h	0101010b	00h, 55h, FFh, AAh
	10	RNOP	WRITE - PC0	06h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	11	RNOP	WRITE - PC1	06h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	12	RNOP	WRITE - PC0	03h	05555h	0101010b	00h, 55h, FFh, AAh
	13	RNOP	WRITE - PC1	03h	05555h	0101010b	00h, 55h, FFh, AAh
	14	RNOP	WRITE - PC0	04h	0AAAAh	1010101b	00h, 55h, FFh, AAh
	15	RNOP	WRITE - PC1	04h	0AAAAh	1010101b	00h, 55h, FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						

9.2. IDD and IPP Specifications

IDD and IPP values are valid for the full operating range of voltage and temperature unless otherwise noted.

Table 65.1. HBM2 Gen2 8Hi

SYMBOL	2.0Gbps			2.4Gbps			Unit	Notes
	IDD (Max)	IDDQ (Max)	IPP (Max)	IDD (Max)	IDDQ (Max)	IPP (Max)		
IDD0	1140	370	80	1190	400	80	mA	
IDD2P	700	270	40	700	270	40	mA	
IDD2P0	700	260	40	700	260	40	mA	
IDD2N	970	390	40	1020	410	40	mA	
IDD3P	700	270	60	700	270	60	mA	
IDD3P0	700	260	60	700	260	60	mA	
IDD3N	1070	390	60	1150	410	60	mA	
IDD4R	6680	2660	330	7710	3090	350	mA	
IDD4W	6550	1530	330	7560	1760	350	mA	
IDD5A	1080	400	70	1130	420	70	mA	
IDD5B	1890	400	420	1940	430	420	mA	
IDD6N(0~85C)	800	270	80	800	270	80	mA	
IDD6E(0~95C)	1120	270	190	1120	270	190	mA	
IDD8	690	260	40	690	260	40	mA	

Table 65.2. HBM2 Gen2 4Hi

SYMBOL	2.0Gbps			2.4Gbps			Unit	Notes
	IDD (Max)	IDDQ (Max)	IPP (Max)	IDD (Max)	IDDQ (Max)	IPP (Max)		
IDD0	1040	370	70	1090	400	70	mA	
IDD2P	590	270	30	590	270	30	mA	
IDD2P0	590	260	30	590	260	30	mA	
IDD2N	860	390	30	920	410	30	mA	
IDD3P	600	270	50	600	270	50	mA	
IDD3P0	600	260	50	600	260	50	mA	
IDD3N	970	390	50	1040	410	50	mA	
IDD4R	6580	2660	320	7620	3090	340	mA	
IDD4W	6450	1530	320	7470	1760	340	mA	
IDD5A	760	310	50	780	320	50	mA	
IDD5B	1160	320	220	1180	330	220	mA	
IDD6N(0~85C)	630	250	50	620	250	50	mA	
IDD6E(0~95C)	790	250	110	780	250	110	mA	
IDD8	580	250	30	580	250	30	mA	

Table 65 - IDD & IDDP Specification Example

9.3. IDD6 Specification

Table 66 - IDD6 Specification

Symbol	Temperature Range	Value	Unit	Notes
IDD6N	0°C - 85°C		mA	2, 3, 7
IDD6E	0°C - T_E		mA	1, 3, 4, 7
IDD6R	0°C - T_R		mA	3, 5, 7
IDD6A	0°C - T_a		mA	3, 5, 5, 6
	T_b - $T_{y\ (optional)}$		mA	3, 5, 5, 6
	T_z - $T_{OPERmax}$		mA	3, 5, 5, 6, 8

NOTE 1 Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
NOTE 2 Applicable for MR0 settings OP[2]=0.
NOTE 3 Supplier data sheets include a max value.
NOTE 4 IDD6E is only specified for devices which support the Extended Temperature Range feature.
NOTE 5 The number of discrete temperature ranges supported and the associated T_a - T_z, and $T_{OPERmax}$ values are supplier/design specific. Temperature ranges are intended to denote the nominal trip points for the internal temperature sensor to bracket discrete self refresh rates internal to the DRAM. Refer to supplier datasheet for more information. IDD6A is only specified for devices which support the temperature Controlled Self Refresh feature enabled by MR0 with OP[2]=1
NOTE 6 T_R represents the temperature used to reflect the current consumed in a typical room temperature environment.
NOTE 7 $T_{OPERmax}$ represents the max temperature supported by the DRAM when TCSR is enabled.

10. AC Timings

Table 67 - Timing Parameters

PARAMETER	Symbol	Speed Bin 2.0 Gbps/pin		Speed Bin 2.4 Gbps/pin		Unit	Note
		MIN	MAX	MIN	MAX		
CK Timings							
CK frequency	f_{CK}	50	1000	50	1200	MHz	
CK clock frequency with bank groups disabled	f_{CKBG}	50	500	50	500	MHz	4,5
CK clock period	t_{CK}	1	20	0.83	20	ns	6
CK clock HIGH-level width	t_{CH}	0.47	0.53	0.47	0.53	tCK	
CK clock LOW-level width	t_{CL}	0.47	0.53	0.47	0.53	tCK	
Command and Address Input Timings							
CKE, command and address input setup time based on VIH/VIL	t_{IS}	100		83		ps	7
CKE, command and address input hold time based on VIH/VIL	t_{IH}	100		83		ps	7
CKE, command and address input setup time based on VIHD/VILD	t_{IS2}	108		TBD		ps	7
CKE, command and address input hold time based on VIHD/VILD	t_{IH2}	108		TBD		ps	7
Command/Address input pulse width	t_{IPW}	300		250		ps	7
Input and Output Timings							
WDQS_t rising edge to CK_t rising edge delay	t_{DQSS}	-0.2	0.2	-0.2	0.2	tCK	
WDQS_t, WDQS_c differential input HIGH pulse width	t_{DQSH}	0.45	-	0.45	-	tCK	
WDQS_t, WDQS_c differential input LOW pulse width	t_{DQSL}	0.45	-	0.45	-	tCK	
WDQS_t falling edge to CK_t rising edge setup time	t_{DSS}	0.2	-	0.2	-	tCK	
WDQS_t falling edge from CK_t rising edge hold time	t_{DSH}	0.2	-	0.2	-	tCK	
DQ, DM, DBI input to WDQS_t, WDQS_c rising or falling edge setup time based on VIH/VIL	t_{DS}	100	-	83	-	ps	7
DQ, DM, DBI input to WDQS_t, WDQS_c rising or falling edge hold time based on VIH/VIL	t_{DH}	100	-	83	-	ps	7
DQ, DM, DBI input to WDQS_t, WDQS_c rising or falling edge setup time based on VIH/VILD	t_{DS2}	108	-	TBD	-	ps	7

Table 67 - Timing Parameters

PARAMETER	Symbol	Speed Bin		Speed Bin		Unit	Note
		2.0 Gbps/pin		2.4 Gbps/pin			
		MIN	MAX	MIN	MAX		
DQ, DM, DBI input to WDQS_t, WDQS_c rising or falling edge hold time based on VIH/VILD	t_{DH2}	108	-	TBD	-	ps	7
DQ, DM, DBI input pulse width	t_{DPW}	300		250		ps	7
RDQS_t, RDQS_c tising edge outputaccess time from CK_t, CK_c rising edge	t_{DQSCK}	0.6	3.5	0.6	3.5	ns	8
RDQS_t, RDQS_c differential output HIGH time	t_{QSH}	0.38	-	0.38	-	tCK	8
RDQS_t, RDQS_c differential output LOW time	t_{QSL}	0.38	-	0.38	-	tCK	8
RDQS_t, RDQS_c edge to DQ, DBI skew, DM, Parity	t_{DQSQ}	-	85	-	85	ps	8
DQ, DBI output hold time from RDQS_t, RDQS_c	t_{QH}	0.38		0.38		tCK	8
DQ, DBI high impedance to low impedance time from CK_t, CK_c	t_{LZ}	t_{DQSCK}(min) - t_{QH}(min)	t_{DQSCK}(max) - t_{DQSQ}(max)	t_{DQSCK}(min) - t_{QH}(min)	t_{DQSCK}(max) - t_{DQSQ}(max)	ns	8
DQ, DBI low impedance to high impedance time from RDQS_t, RDQS_c	t_{HZ}	t_{DQSCK}(min)	t_{DQSCK}(max)+ t_{DQSQ}(max)	t_{DQSCK}(min)	t_{DQSCK}(max)+ t_{DQSQ}(max)	ns	8

Table 68 - Timing Parameters (Part 2)

PARAMETER		Symbol	Speed Bin 2.0 Gbps/pin		Speed Bin 2.4 Gbps/pin		Unit	Note
			Min	Max	Min	Max		
Row Access Timings								
Active to Active command period		t_{RC}	45	-	45		ns	
Active to PRECHARGE command period		t_{RAS}	29	9*t_{REFI}	29	9*t_{REFI}	ns	9
Active to READ command delay		t_{RCDRD}	16	-	16		ns	
Active to WRITE command delay		t_{RCDWR}	14	-	14		ns	
Active bank A to Active or Single Bank Refresh bank B command delay same bank group		t_{RRDL}	max(3ns, 2tCK)	-	max(3ns, 2tCK)		ns	10
Active bank A to Active or Single bank Refresh bank B command delay different bank group		t_{RRDS}	max(3ns, 2tCK)	-	max(3ns, 2tCK)		ns	11
Four bank activate window (Same PC)		t_{FAW}	16	-	16		ns	12
READ to PRECHARGE command delay same bank with bank groups enabled	BL=4	t_{RTPL}	max(5tCK, 5ns+2tCK)	-	max(5tCK, 5ns+2tCK)		ns	13, 14
READ to PRECHARGE command delay same bank with bank groups disabled	BL=4	t_{RTPS}	max(5tCK, 5ns+1tCK)	-	max(5tCK, 5ns+1tCK)		ns	15
PRECHARGE command period		t_{RP}	16	-	16		ns	
WRITE recovery time		t_{WR}	16+1tCK	-	16+1tCK		ns	
Auto precharge write recovery + precharge time		t_{DAL}	WR+roundup(t_{RP}/t_{CK}(avg))		WR+roundup(t_{RP}/t_{CK}(avg))		nCK	16
Column Access Timings								
RD bank A to RD bank B command delay (Same bank group)	BL=4	t_{CCDL}	4	-	4		nCK	14, 17, 18
RD bank A to RD bank B command delay (Different bank group)	BL=4	t_{CCDS}	2	-	2		nCK	19, 20
RD bank A to RD bank B command delay (Different SID)	BL=4	t_{CCDR}	3	-	3		nCK	21
Internal WRITE to READ command delay (Same bank group)		t_{WTRL}	max(5tCK, 5ns+1tCK)	-	max(5tCK, 5ns+1tCK)		ns	14, 17
Internal WRITE to READ command delay (Different bank group)		t_{WTRS}	max(5tCK, 4ns+1tCK)	-	max(5tCK, 4ns+1tCK)		ns	19
READ or RDTR to WRITE or WRTR command delay (READ to WRITE command delay)		t_{RTW}	RL+BL/2-WL+tDQSCK(max)+tDQSQ(max)+tDQSS(min)+0.5tCK, and round up to the next integer	-	RL+BL/2-WL+tDQSCK(max)+tDQSQ(max)+tDQSS(min)+0.5tCK, and round up to the next integer		ns	22

Power-Down and Refresh Timings								
Power down entry to exit time		t_{PD}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	ns	
Power down exit time		t_{XP}	max(4tCK, 7.5ns)	-	max(4tCK, 7.5ns)	-	nCK	
CKE min high and low pulse width		t_{CKE}	max(5tCK, 7.5ns)		max(5tCK, 7.5ns)		ns	
Implicit Precharge to POWER-DON ENTRY command delay		$t_{IM-PREPDE}$	(t_{RP}/t_{CK})+1		(t_{RP}/t_{CK})+1		nCK	
Command path disable delay		t_{CPDED}	2	-	2	-	nCK	
Activate to Power-Down-Entry command delay		t_{ACTPDE}	1	-	1	-	nCK	23
Precharge to Power-Down-Entry command delay		t_{PRPDE}	1	-	1	-	nCK	
Refresh to Power-Down-Entry command delay		t_{REFPDE}	1	-	1	-	nCK	23
Single Bank Refresh to Power-Down-Entry command delay		$t_{REFSB-PDE}$	1	-	1	-	nCK	23
Mode Register Set to Power-Down-Entry command delay		t_{MRSPDE}	t_{MOD}(min)	-	t_{MOD}(min)	-	nCK	
Read or Read w/AP to Power-Down-Entry command delay		t_{RDPDE}	RL+PL+BL/2+1	-	RL+PL+BL/2+1	-	nCK	
Write to Power-Down-Entry command delay		t_{WRPDE}	WL+PL+BL/2+1+(t_{WR}/t_{CK})	-	WL+PL+BL/2+1+(t_{WR}/t_{CK})	-	nCK	24
Write w/AP to Power-Down-Entry command delay		t_{WRAPDE}	WL+PL+BL/2+1+WR	-	WL+PL+BL/2+1+WR	-	nCK	25
Self-Refresh Timings								
CKE min. LOW width for self-refresh entry to exit		t_{CKESR}	t_{CKE}(min)+1nCK	-	t_{CKE}(min)+1nCK	-	nCK	
Valid CK Clock required after self refresh or power-down entry		t_{CKSRE}	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	nCK	
Valid CK Clock required before self refresh power down exit		t_{CKSRX}	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	nCK	
Read of Read w/AP to SELF REFRESH ENTRY command delay		t_{RDSRE}	RL+PL+BL/2+1	-	RL+PL+BL/2+1	-	nCK	
Exit self-refresh command delay		t_{XS}	max(5tCK, t_{RFC}(min)+10ns)	-	max(5tCK, t_{RFC}(min)+10ns)	-	ns	
Exit self-refresh to Mod register Set command delay		t_{XSMRS}	t_{XS}	-	t_{XS}	-	ns	
Refresh Timings								
REFRESH command period	4Gb per Channel, So 4Hi case	t_{RFC}	260	-	260	-	ns	26
	8Gb per Channel, So 8Hi case		350	-	350	-	ns	26
Single Bank Refresh Command period (same bank)		t_{RFCSB}	120		120		ns	

Single Bank Refresh Command period (different bank)		t_{RREFD}	max(8ns, 4tCK)		max(8ns, 4tCK)		ns	
Average periodic refresh interval for Refresh command	4Gb per Channel, So 4Hi case	t_{REFI}		3.9		3.9	us	26, 27
	8Gb per Channel, So 8Hi case			3.9		3.9	us	26, 27
Average periodic refresh interval for Single bank refresh command	4Gb per Channel, So 4Hi case	t_{REFISB}		0.24		0.24	us	26, 28
	8Gb per Channel, So 8Hi case			0.12		0.12	us	26, 28
Miscellaneous Timings								
Mode Register Set command update delay		t_{MOD}	max($12t_{CK}$, 15ns)	-	max($12t_{CK}$, 15ns)	-	ns	
Mode Register Set command cycle time		t_{MRD}	4	-	4	-	ns	
Internal VREFD offset single step settling time		t_{VREFD}		-		-	ns	
Internal VREFD offset full step settling time		t_{FVREFD}		-		-	ns	
DERR and AERR output pulse width			-	1	-	1	ns	
ADD/CMD parity error output delay		t_{PARAC}	$2t_{CK}$ + 0.4ns	$2t_{CK}$+2.5ns	$2t_{CK}$ + 0.4ns	$2t_{CK}$+2.5ns	ns	29
Write data parity error output delay		t_{PARDQ}	0.4	4	0.4	4	ns	30
Read Latency	DBI on	RL	24	27	28	29	n_{CK}	
Write Latency		WL	7	8	7	8	n_{CK}	

Note:

1. AC timing parameters apply to each channel of the HBM device independently. No timing parameters are specified across channels, and all channels operate independently of each other.

2. SK Hynix HBM2 Gen1. support 1.6 Gbps only.

3. All parameter assume proper device initialization.

4. HBM devices must support device operation with bank groups disabled up a 500MHz or the maximum rated operating clock frequency, whatever is the lower value.

5. Bank Group Frequency ranges (not to scale):



6 Parameter t_{CK} is calculated as the average clock period across any consecutive 1,000 cycle window, where each clock period is calculated both from rising CK_t edge to rising CK_t edge and falling CK_t edge to falling CK_t edge.

7 Parameter is based on VIH and VIL. Vref based setup/hold times are calculated by adding ΔtDS or ΔtDH to these numbers according to table69 and the figre below.

8 Parameter is measured with Output Timing reference load and Read DBI enabled.

9 For Reads and Writes with auto precharge enabled the device will hold off the internal precharge until tRAS(min) has been satisfied or the number of clock cycles as programmed for RAS in MR3 have elapsed.

10 Parameter applies when bank groups are enabled and consecutive commands access the same bank group.

11 Parameter applies when bank groups are disabled or consecutive commands access different bank groups.

12 Not more than 4 ACTIVATE or SINGLE BANK REFRESH commands are allowed within tFAW period.

13 Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.

14 SK Hynix HBM2 does not support legacy mode.

15 Parameter applies when bank groups are disabled and READ and PRECHARGE commands access the same bank.

16 tDAL = (tWR/tCK) + (tRP/tCK). For each of the terms, if not already an integer, round up to the next integer.

17 Parameter applies when bank groups are enabled and consecutive commands access the same bank group.

18 tCCDL is either for seamless consecutive READ or seamless consecutive WRITE commands.

19 Parameter applies when bank groups are disabled or consecutive commands access different bank groups.

20 tCCDS is either for seamless consecutive READ or seamless consecutive WRITE commands.

21 tCCDR is a vendor specific parameter for 8-High HBM devices (DEVICE_ID WDR bit[7] = 1) that should be used for seamless consecutive READ commands between different stack IDs (SID) instead of tCCDS. The tCCDR(min) value is vendor specific and a range of 2 to 4nCK is supported. The vendor datasheet should be consulted for details. For seamless WRITE commands the normal tCCDS parameter applies. tCCDR does not apply to DWORDMISR operations when DWORD Loopback is enabled in MR7

22 tRTW is not a DRAM device limit but determined by the system bus turnaround time. Avoid bus contention by setting tRTW (min) = RL+BL/2-WL+tDQSCK(max)+tDQSQ(max)+tDQSS(min)+0.5tCK, and round up to the next integer

23 Upon entering power-down the CK clock may be stopped after the number of clock cycles as programmed for RAS in MR3.

24 tWR is defined in ns. For calculation of tWRPDE round up tWR/tCK to the next integer.

25 WR in clock cycles as programmed in MR1.

26 Density is given per channel.

27 A maximum of 8 consecutive REFRESH commands can be posted to an HBM device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * tREFI.

28 tREFISB = tREFI / N;N = no. of banks.

29 tPARAC may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The nominal AERR HIGH time in case of a parity error is 1 nCK.

30 tPARDQ may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The nominal DERR HIGH time in case of a parity error is 1 nCK.

Table 69 - Derating Value Table for Setup/Hold Timings

Slew Rate [V/ns]	CMOS Input Receiver (V_{IH}=0.7*V_{DDQ}, V_{IL}=0.3*V_{DDQ})		VREF Based Input Receiver (V_{IHD}=V_{REF}+0.2V, V_{ILD}=V_{REF}-0.2V)		Unit
	ΔtDS	ΔtDH	ΔtDS	ΔtDH	
2	120	120	100	100	ps
3	80	80	67	67	ps
4	60	60	50	50	ps
5	48	48	40	40	ps
6	40	40	33	33	ps
7	34	34	29	29	ps
8	30	30	25	25	ps
9	27	27	22	22	ps
10	24	24	20	20	ps

11. Package (Die) Specification

11.1. Signals

Table 70 - I/O Signal Description

Signals	Type	Description
CK[a:h]_t, CK[a:h]_c	Input	Clock: CK_t and CK_c are differential clock inputs. Row and column command and address inputs are latched on the rising and falling edges of CK_t. CKE is latched on the rising edge of CK_t only. All latencies are referenced to the rising edge of CK_t.
CKE[a:h]	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, device input buffers, and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operations (all banks idle), or Active Power-Down (row activated in any bank). CKE must be maintained HIGH throughout read and write accesses.
C[a:h]0 - C[a:h]7	Input	Column command and address: the command code, bank and column address for Write and Read operations and the Mode Register address and code to be loaded with Mode Register Set commands are received on the C0-C7 inputs.
R[a:h]0 - R[a:h]5	Input	Row command and address: the command code, bank and row address for Activate, Precharge and Refresh commands are received on the R0-R5 inputs.
DQ[a:h]0 - DQ[a:h]127	I/O	Data Input/Output: 128-bit data bus
DBI[a:h]0 - DBI[a:h]15	I/O	Data Bus Inversion: DBI0 is associated with DQ0-DQ7, DBI1 is associated with DQ8-DQ15, ... , and DBI15 is associated with DQ120-DQ127.
DM[a:h]0 - DM[a:h]15	I/O	Data Mask: DM0 is associated with DQ0-DQ7, DM1 is associated with DQ8-DQ15, ... , and DM15 is associated with DQ120-DQ127.
PAR[a:h]0 - PAR[a:h]3	I/O	Data Parity: one data parity bit per DWord. PAR0 is associated with DQ0-DQ31, PAR1 is associated with DQ32-DQ63, PAR2 is associated with DQ64-DQ95, and PAR3 is associated with DQ96-DQ127.
DERR[a:h]0 - DERR[a:h]3	Output	Data parity error: one data parity error bit per DWord. DERR0 is associated with DQ0-DQ31, DERR1 is associated with DQ32-DQ63, DERR2 is associated with DQ64-DQ95, and DERR3 is associated with DQ96-DQ127.
AERR[a:h]	Output	Address parity error. One address parity error bit for row and column address and command per channel.
WDQS[a:h]0_t - WDQS[a:h]3_t, WDQS[a:h]0_c - WDQS[a:h]3_c	Input	Write Data Strobe: WDQS_t and WDQS_c are differential strobe inputs. Write input data are latched on the rising and falling edges of WDQS_t,WDQS_c. One WDQS pair per DWord. WDQS0_t,WDQS0_c are associated DQ0-DQ31, WDQS1_t,WDQS1_c are associated DQ32-DQ63, WDQS2_t,WDQS2_c are associated DQ64-DQ95, and WDQS3_t,WDQS3_c are associated DQ96-DQ127.
RDQS[a:h]0_t - RDQS[a:h]3_t, RDQS[a:h]0_c - RDQS[a:h]3_c	Output	Read Data Strobe: RDQS_t and RDQS_c are differential strobe outputs. Read output data are sent on the rising and falling edges of RDQS_t,RDQS_c. One RDQS pair per DWord. RDQS0_t,RDQS0_c are associated DQ0-DQ31, RDQS1_t,RDQS1_c are associated DQ32-DQ63, RDQS2_t,RDQS2_c are associated DQ64-DQ95, and RDQS3_t,RDQS3_c are associated DQ96-DQ127.
DA[59:0]	I/O	Direct Access Input/Output: These pins are provided for direct access test. They must be routed directly to an external package I/O pin. The function is defined by the memory vendor.
RESET_n	Input	RESET: RESET_n LOW asynchronously initiates a full chip RESET of the HBM device.
NC		No connect pad: electrically isolated
WRCK	Input	IEEE-1500 Wrapper Serial Port Clock
WRST_n	Input	IEEE-1500 Wrapper Serial Port RESET
SelectWIR	Input	IEEE-1500 Wrapper Serial Port Instruction Register Select
ShiftWR	Input	IEEE-1500 Wrapper Serial Port Shift
CaptureWR	Input	IEEE-1500 Wrapper Serial Port Capture
UpdateWR	Input	IEEE-1500 Wrapper Serial Port Update
WSI	Input	IEEE-1500 Wrapper Serial Port Data
WSO[a:h]	Output	IEEE-1500 Wrapper Serial Port Data Out Channels [h:a]
RSVD0 - RSVD5		Reserved pad: reserved for future use for TEST (DRAM Vendor Probe only point)
RD[a:h]0 - RD[a:h]7	I/O	Redundant microbumps in DWORD
RC[a:h]	Input	Redundant column command and address microbump in AWORD
RR[a:h]	Input	Redundant row command and address microbump in AWORD

Table 70 - I/O Signal Description

Signals	Type	Description
ARFU[a:h]0 - ARFU[a:h]3		Resreved for future use; Unused microbumps in AWORD
MRFU0 - MRFU23		Reserved for future use, Unused microbumps in Mid-stack region
NOBUMP		Depopulated pad: reserved as test pad for probing
TEMP[2:0]	Output	DRAM Temperature Report
CATTRIP	Output	DRAM Catastrophic Temperature Report
VDDC, VPP, VDDQ	Supply	Power supply

NOTE 1 Index [a:h] represents the channel indicator “a” to “h” of the HBM device; signal names including the channel indicator are used whenever more than one channel is referenced, as e.g., with the HBM ballout. The channel indicator is omitted whenever features and functions common to all channels are described.

NOTE 2 A 4-channel HBM device comprises channels a to d.

NOTE 3 HBM devices supporting less than 8 channels are allowed to have input/output buffers physically present at the pins associated with the unavailable channels, however these input/output buffers will be disabled. The host shall leave those pins floating. The availability of each channel [a:h] has to be coded in IEEE1500 "DEVICE_ID Wrapper Data Register"bits [15:8]

NOTE 4 All power supply microbumps defined in the "HBM Stack Height" must be present and connected with their respective power nets even if the related channel is not present or marked non-working.

11.2. MicroBump Positions

The MicroBump pattern of the DRAM stack employs a face-centered rectangular (FCR) pattern as depicted in Figure 90. In an FCR pattern, a 'staggered' bump is located halfway between major row and column, hence its location is determined by X/2 and Y/2. Table 71 shows geometric parameters of the FCR MicroBump pattern. Parameter P_{Min} is the minimum bump pitch anywhere in the MicroBump field; for chosen X and Y parameters, it coincides with the vertical pitch, i.e. P_{Min} = Y.

The HBM bump matrix as shown in subsequent tables consists of 220 rows with a pitch of Y/2 and 68 columns with a pitch of X/2. The overall array size is (67 x X/2 + D) x (219 x Y/2 + D) = 3241 um x 6047.5 um. The ball matrix is center aligned with the die. The ball array center is the origin of the ball location coordinates. Ball A1 is located at the top left at X = -1608 µm, Y = +3011.25 µm.

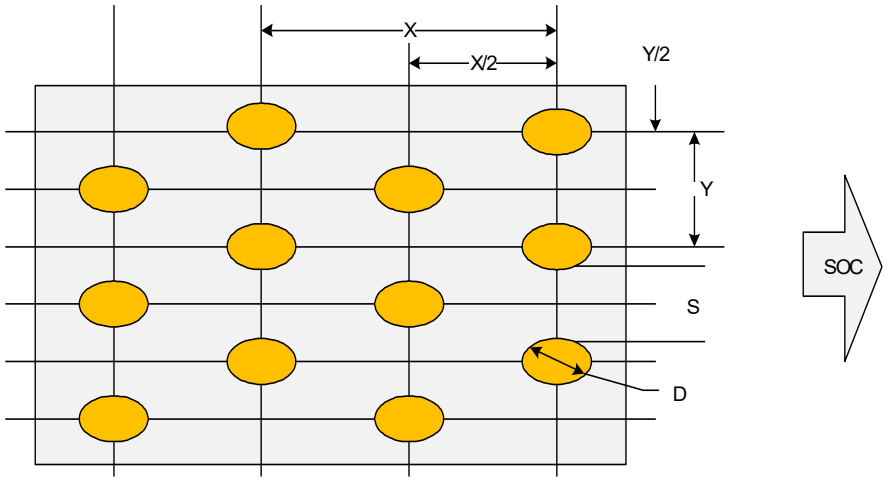


Figure 90. Staggered MicroBump Pattern

Table 71 - Geometric Parameters of the FCR MicroBump Pattern

Label	Nominal Value	Description
X	96 um	Horizontal pitch of two adjacent MicroBumps
Y	55 um	Vertical pitch of two adjacent MicroBumps
P_{Min}	55 um	Minimum pitch of the bump field; Same as Y for chosen X and Y parameters
D	25 um	MicroBump diameter
S		Bump-to-bump air gap; S = P_{Min} -D

11.3. HBM Stack Height

Table 72 - Stack Height

Configuration	Minimun	Typical	Maximum	Unit
2-High	695	720	745	um
4-High	695	720	745	um
8-High	695	720	745	um
NOTE 1 The configuration refers to the number of memory dies in the stack. The stack may include an additional base (interface) die. NOTE 2 HBM stack height refers to the "A2" dimension and is compliant to package code "W" of MO-316 Rev. A. The "A2" dimension does not include the microbumps.				

11.4. HBM Ballout

A geographical overview of the HBM bump matrix is provided in Table 73, and the detailed bump matrix in Table 74 and Table 75. Due to space constraints these tables use abbreviations for specific functions as given in Table 74 The orientation of the ballout shown is the bottom view looking at the microbumps.

HBM devices supporting less than 8 channels must have all microbumps physically present as shown in the tables below.

Table 73 - HBM Ballout - Geographical Overview (Not to scale)

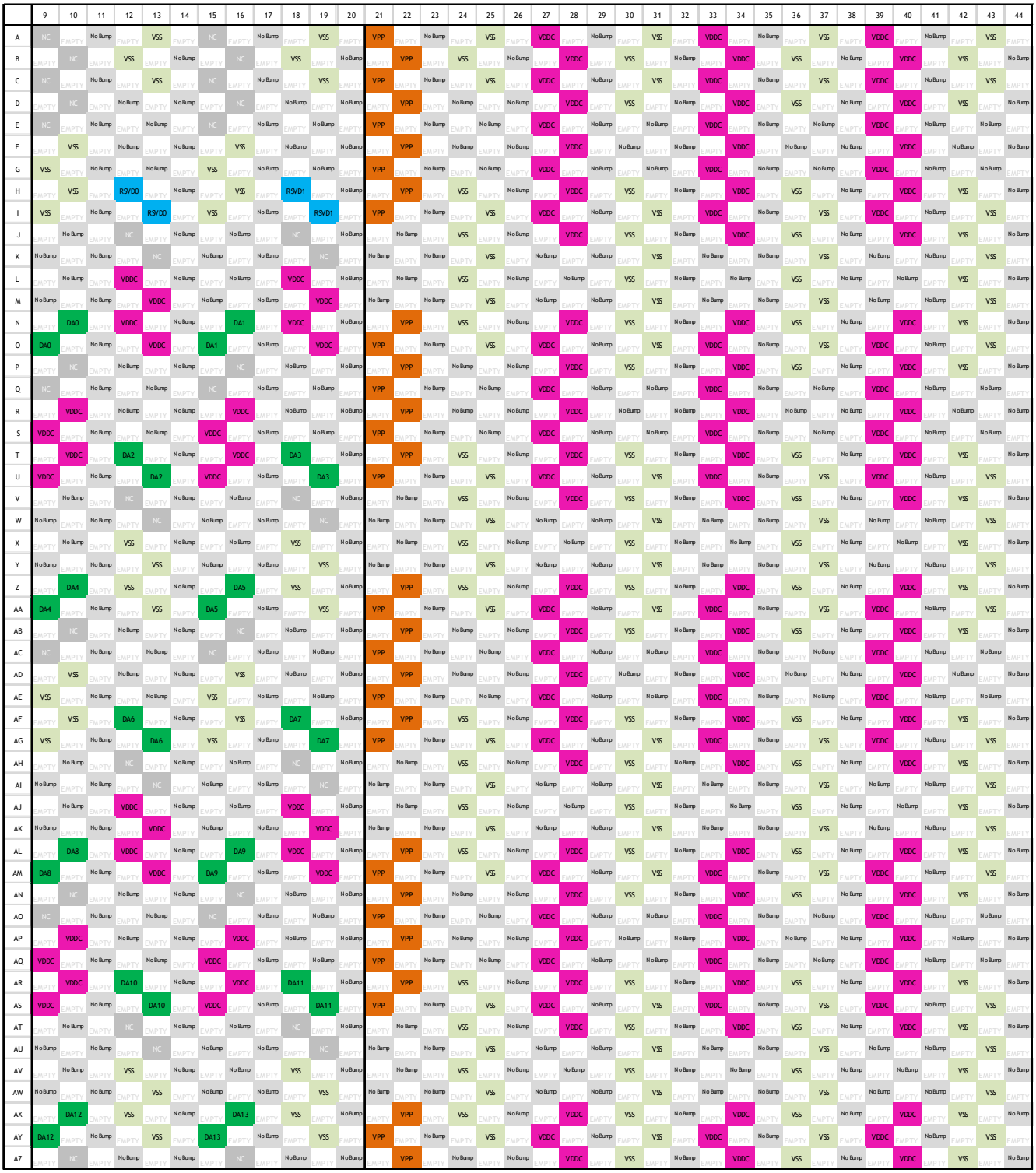
<table>
<tr><td rowspan="2">ROWS</td><td></td><td colspan="3">See Table 74</td><td colspan="2">See Table 75</td></tr>
<tr><td>Columns #</td><td>1 ~ 8</td><td>9 ~ 20</td><td>21 ~ 44</td><td>45 ~ 56</td><td>57 ~ 68</td></tr>
<tr><td></td><td>A~M</td><td rowspan="10">Mechanical Bumps</td><td rowspan="10">Direct Access Test Port</td><td rowspan="10">Power Supply Region</td><td>DWORD0_Channel_e</td><td>DWORD0_Channel_a</td></tr>
<tr><td></td><td>N~AD</td><td>DWORD0_Channel_f</td><td>DWORD0_Channel_b</td></tr>
<tr><td></td><td>AE~AT</td><td>DWORD1_Channel_e</td><td>DWORD1_Channel_a</td></tr>
<tr><td></td><td>AU~BH</td><td>DWORD1_Channel_f</td><td>DWORD1_Channel_b</td></tr>
<tr><td></td><td>BH~BP</td><td>AWORD Channel e</td><td>AWORD Channel a</td></tr>
<tr><td></td><td>BR~BY</td><td>AWORD Channel f</td><td>AWORD Channel b</td></tr>
<tr><td></td><td>CA~CM</td><td>DWORD2_Channel_e</td><td>DWORD2_Channel_a</td></tr>
<tr><td></td><td>CN~DD</td><td>DWORD2_Channel_f</td><td>DWORD2_Channel_b</td></tr>
<tr><td></td><td>DE~DT</td><td>DWORD3_Channel_e</td><td>DWORD3_Channel_a</td></tr>
<tr><td></td><td>DU~ED</td><td rowspan="2">DWORD3_Channel_f</td><td rowspan="2">DWORD3_Channel_b</td></tr>
<tr><td></td><td>EE~EH</td><td colspan="3" rowspan="3">Depopulated micropillar area
deticated for (Optional) Probe Pads</td></tr>
<tr><td></td><td>EH~EM</td><td colspan="2">Reset, IEEE1500 Port. Temperaturee</td></tr>
<tr><td></td><td>EN~ET</td><td rowspan="2">DWORD0_Channel_g</td><td rowspan="2">DWORD0_Channel_c</td></tr>
<tr><td></td><td>EU~FD</td><td rowspan="10">Mechanical Bumps</td><td rowspan="10">Direct Access Test Port</td><td rowspan="10">Power Supply Region</td></tr>
<tr><td></td><td>FE~FT</td><td>DWORD0_Channel_h</td><td>DWORD0_Channel_d</td></tr>
<tr><td></td><td>FU~GH</td><td>DWORD1_Channel_g</td><td>DWORD1_Channel_c</td></tr>
<tr><td></td><td>GJ~GY</td><td>DWORD1_Channel_h</td><td>DWORD1_Channel_d</td></tr>
<tr><td></td><td>HA~HF</td><td>AWORD Channel g</td><td>AWORD Channel c</td></tr>
<tr><td></td><td>HG~HM</td><td>AWORD Channel h</td><td>AWORD Channel d</td></tr>
<tr><td></td><td>HN~JD</td><td>DWORD2_Channel_g</td><td>DWORD2_Channel_c</td></tr>
<tr><td></td><td>JE~JT</td><td>DWORD2_Channel_h</td><td>DWORD2_Channel_d</td></tr>
<tr><td></td><td>JU~KH</td><td>DWORD3_Channel_g</td><td>DWORD3_Channel_c</td></tr>
<tr><td></td><td>KJ~KY</td><td>DWORD3_Channel_h</td><td>DWORD3_Channel_d</td></tr>
</table>

11.4.1. HBM Ballout - Power Supply and Test Region - Channels [a:b, e:f]

Table 74 - HBM Ballout Part 1 : Columns 1 to 44

	1	2	3	4	5	6	7	8
A	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
B	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
C	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
D	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
E	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
F	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
G	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
H	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
I	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
J	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
K	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
L	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
M	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
N	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
O	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
P	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
Q	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
R	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
S	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
T	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
U	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
V	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
W	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
X	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
Y	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
Z	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AA	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AB	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AC	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AD	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AE	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AF	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AG	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AH	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AI	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AJ	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AK	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AL	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AM	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AN	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AO	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AP	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AQ	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AR	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AS	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AT	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AU	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AV	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AW	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
AX	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
AY	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY

	1	2	3	4	5	6	7	8
BA	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BB	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BC	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BD	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BE	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BF	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BG	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BH	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BI	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BJ	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BK	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BL	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BM	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BN	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BO	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BP	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BQ	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BR	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BS	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BT	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BU	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BV	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BW	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BX	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
BY	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
BZ	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CA	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CB	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CC	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CD	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CE	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CF	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CG	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CH	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CI	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CJ	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CK	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CL	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CM	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CN	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CO	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CP	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CQ	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CR	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CS	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CT	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CU	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CV	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CW	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY
CX	EMPTY	NOBUMP	EMPTY	NC	EMPTY	NC	EMPTY	NOBUMP
CY	NC	EMPTY	NC	EMPTY	NOBUMP	EMPTY	NC	EMPTY



HBM Ballout - Optional Probe Area (Micropillar No Bump Area)

Table 75 - HBM Ballout part2 : Columns 45 to 68

	1	2	3	4	5	6	7	8
DA	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DB	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP
DC	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DD	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP
DE	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DF	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP
DG	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DH	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP
DI	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DJ	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP
DK	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY
DL	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP	EMPTY	NOBUMP

12. HBM DRAM Assembly

The HBM DRAM assembly is not defined by this standard. The shape and materials of the die to die, interfaces between the die in the HBM DRAM are not defined in this standard and the shape (Annular, Cone, Cylinder, etc) and materials (Cu, W) are not defined or restricted in this standard. However these interfaces must fit within the electrical requirements of the channel interface.

13. Test and Boundary Scan

HBM DRAMs provide two separate test interfaces as described below:

- a direct access (DA) test port, intended for the vendor to access the HBM device independent of the host
- an IEEE 1500 Standard test port, to be controlled by the host.

13.1. Direct Access(DA) Test Port

A DRAM direct access port is available via DA[59:0] for vendor specific test implementations. Two microbumps and a depopulated area for probing are associated with each DA pin (see "HBM Ballout").

When DA[28] = 0, DA[59:29, 27:0] drivers are in Hi-Z and input receivers are disabled allowing the bus to float. When DA[28] = 1, DA[59:29, 27:0] are enabled for vendor specific test features; and the IEEE 1500 port is disabled.

The DA[28] input is equipped with an internal pull-down resistor which ensures that DA[28] = 0 if the pin is left floating.

For implementations of multiple HBM devices in a package, there is a large burden on the package pin count to bring out separate DA[59:0] buses for each HBM device. Optionally, a user can bring out a subset of the DA[59:0] pins to connect up to 4 HBMs in a package to connect the devices in parallel (**Figure 91**).

20 DA pins are designated to connect point to point to each DRAM. 18 pins are designated to connect in parallel to up to four HBM devices on a multi drop bus. The function of each of these pins is vendor specific. **Table 76** defines which DA pins are allocated for point to point and for multi drop.

Table 76 - Direct Access (DA) Pin Allocation

Pin Group	DA Pin List	Pin Count
Point to Point	DA13, DA16, DA17, DA18, DA20, DA22, DA24, DA25, DA26, DA28, DA29, DA30, DA32, DA34, DA36, DA38, DA49, DA53, DA57, DA59	20
Multi Drop	DA4, DA5, DA6, DA8, DA10, DA12, DA14, DA21, DA40, DA42, DA44, DA46, DA48, DA50, DA52, DA54, DA56, DA58	18
Note 1 : The remaining 22 DA pins are High-Z when DA[28] = 0; the pin's state is vendor specific when DQ[28] = 1.		

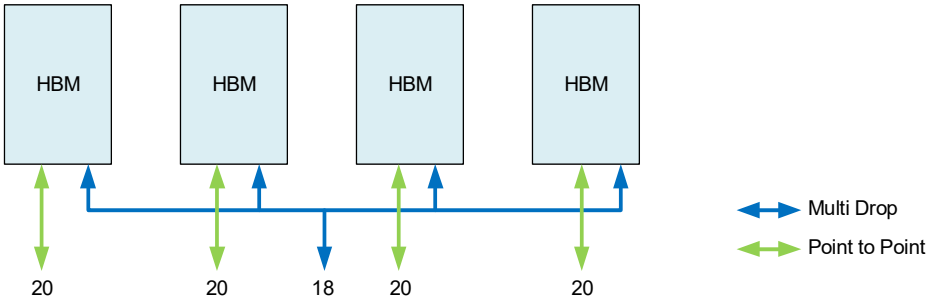


Figure 91. DA Port Connection Diagram For Multiple HBM Devices

13.1.1. DA[28] Lockout

MR8 OP[0] bit if set on channel a or e, disables DA[28] from enabling the DA direct access port. Once the bit is set to “1”, DA port will remain disabled unless power is removed from the HBM device. Any chip reset through pulling RESET_n Low or IEEE1500 "HBM RESET" instruction, or writing a “0” via an MRS command or IEEE1500 instruction "MODE REGISTER DUMP SET" will not clear the bit.

13.2. IEEE Standard 1500

IEEE Standard 1500 port is required for direct connection between host and HBM DRAM. The HBM DRAM provides one IEEE Standard 1500 port, extending the standard specification to replicate the WSO output per channel. This extension allows some commands to execute in parallel across channels, and eliminates the need for cross-channel arbitration for WSO.

Pin DA[28] = 0 selects the IEEE 1500 test port and DA[28] = 1 selects the DA port. It is possible to operate the HBM DRAM without using the test ports. In this case DA[28] and WRST_n must be tied LOW to prevent the device from entering test modes.

Table 77 summarizes the status of the test access port signals.

Table 77 - Test Access Port Pin Status

WRST_n	DA[28], MR8 OP[0]	Pin Name	Type	Status
L	DA[28] = L or MR8 OP[0] = H	Other IEEE1500 inputs*1	Input	X (Don't Care)
		WSO	Output	V (Valid)*2
		DA[59:29,27:0]	I/O	X (Don't Care)
H	DA[28] = L or MR8 OP[0] = H	Other IEEE1500 inputs*1	Input	Active
		WSO	Output	V (Valid)*2
		DA[59:29,27:0]	I/O	X (Don't Care)
Don't Care	DA[28] = H and MR8 OP[0] = L	Other IEEE1500 inputs*1	Input	X (Don't Care)
		WSO	Output	V (Valid)*2
		DA[59:29,27:0]	I/O	SK specific*3

NOTE 1 WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR, WSI.
NOTE 2 V = Valid Signal (either H or L, but not floating).
NOTE 3 Please refer to vendor's datasheet.

IEEE Standard 1500 operations may be asserted at any time after device initialization and during normal memory operation including when the HBM memory device is in power-down or self refresh mode. See "Interaction with Mission Mode Operation" for how the various instructions interact with normal operation, and requirements for returning to normal operation. See also "Initialization Sequence For Use Of Limited IEEE 1500 Instruction Including Lane Repairs" for a subset of operations that are allowed before the device initialization has been completed.

The implementation will feature a 12-bit Wrapper Instruction Register (WIR) format. WIR[11:8] used to address the target channel. Supported WRCK frequency range is 0-50 MHz.

Please refer to IEEE standards at ieee.org for functional standard

13.2.1. Test Access Port IO Signal

Table 78 - Signal List and Description

SYMBOL	Type	Description
WRCK	Input	Dedicated clock used to operate IEEE Std 1500 functions.
WRST_n	Input	When pulled LOW, WRST_n asynchronously puts the wrapper into its normal system mode. No WRCK clocks are required when WRST_n is LOW. See "WDR RESET State"
WSI	Input	IEEE Std 1500 wrapper serial input.
SelectWIR	Input	SelectWIR determines what type of WR operation, i.e., instruction or data, is to be performed.
CaptureWR	Input	Used to enable and control a Capture operation in the selected IEEE Std 1500 wrapper register (WR).
ShiftWR	Input	Used to enable and control a Shift operation in the selected IEEE Std 1500 wrapper register (WR).
UpdateWR	Input	Used to enable and control an Update operation in the selected IEEE Std 1500 wrapper register (WR).
WSO[h:a]	Output	IEEE Std 1500 per-channel wrapper serial output.

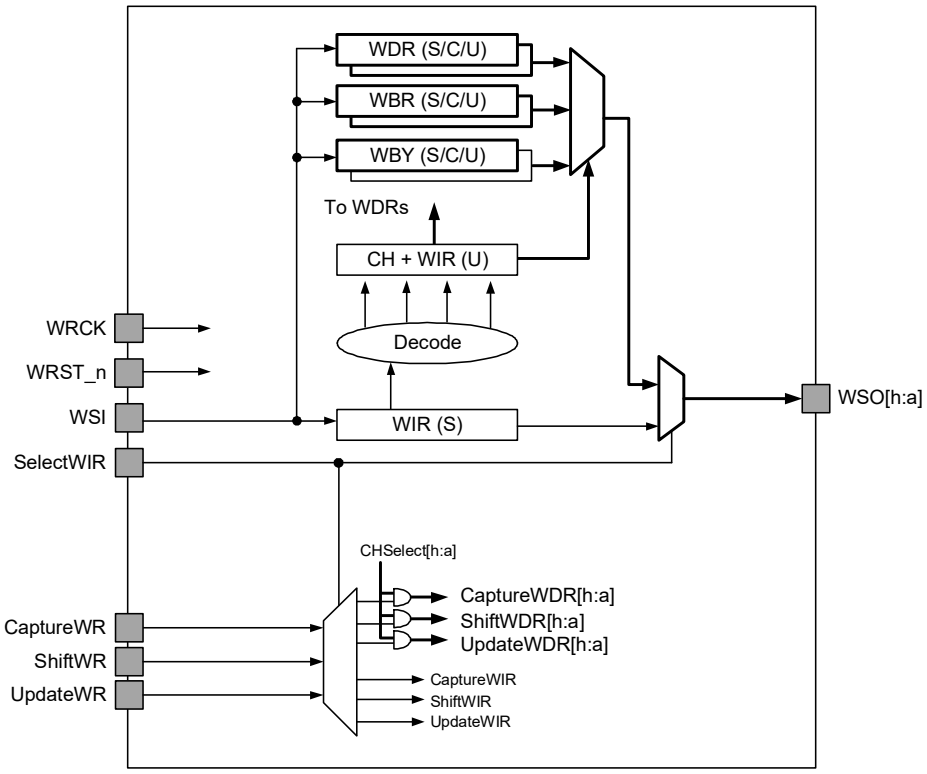


Figure 92. IEEE Std 1500 Logic Diagram

Figure 92 shows a diagram of the HBM IEEE 1500 architecture. This is a IEEE 1500 compliant architecture that uses an asymmetrical WSP (Wrapper Serial Port) with a single WSI and per channel WSOs. The standard 1500 register stack is shown in the diagram, including the WBY (Wrapper BYPASS), WBR (Wrapper Boundary Register), and WDRs (Wrapper Data Registers). The C, S and U notation for the registers refer to Capture, Shift and Update respectively, and indicate for each of the registers which functions are required for that register. So for example the WBY only requires a Shift/Capture stage, whereas the WDRs require Shift/Capture and Update stages. In HBM implementations the WBR may be implemented without an Update stage to save silicon area, however separate _TX and _RX instructions must then be provided (see Table 78) in this case.

The WSO[a:h] output drivers are permanently enabled, with their drive state being LOW, HIGH, or undefined based on the current instruction loaded into the WIR. For example, if BYPASS is the current instruction, then WSO output data is defined only after one or more WRCK clock cycles have been applied.

The 1500 WIR (Wrapper Instruction Register) logic is also shown in Figure 92. Figure 93 shows further details of the WIR implementation for the HBM IEEE 1500 architecture. The WIR and instruction opcodes are described in "Wrapper Instruction Register Encodings". The four channel select bits of the WIR shift stage in Figure 93 are decoded to generate the CHSelect[a:h] outputs. These channel ID selects are used to control the per channel operation of the instructions. When a channel is not selected for an active instruction, then the CaptureWDR[a:h], ShiftWDR[a:h] and UpdateWDR[h:a] enables of the WSP are gated off. This will disable the WDRs of unselected channels for the decoded instruction.

This gating is show at the output of the de-multiplexer in Figure 92.

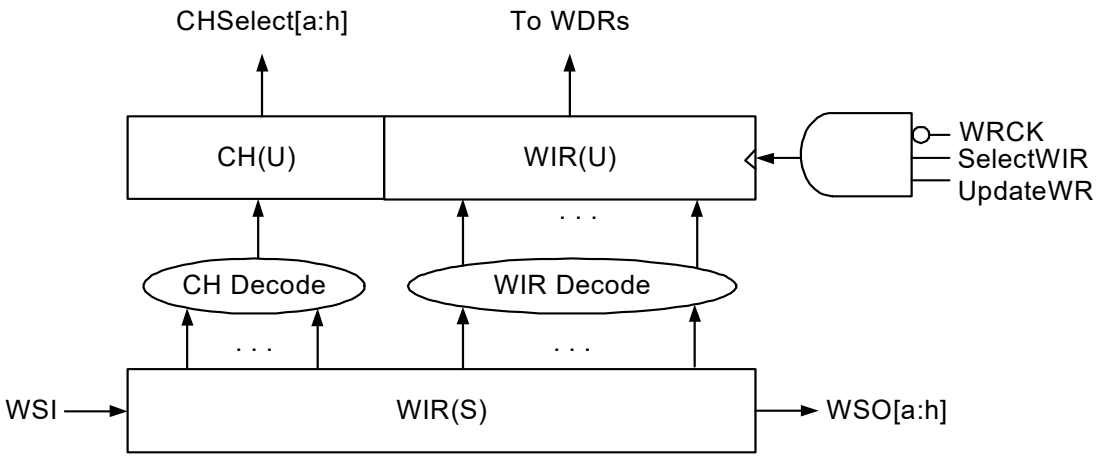


Figure 93. WIR Channel Select Logic Diagram

HBM devices are allowed to support less than 8 channels. The availability of each channel is coded in IEEE1500 "DEVICE_ID Wrapper Data Register" bits [15:8]. Unavailable channels are not required to respond to IEEE1500 instructions with the exception of the global instructions BYPASS and RESET that must be supported for all channels. This includes that all WSO[a:h] outputs are always present.

Figure 94 illustrates an IEEE1500 port operation sequence with a minimum number of WRCK cycles:

• Signal SelectWIR is set at clock edge T0. Control signals CaptureWR, ShiftWR and UpdateWR are all inactive as they are not allowed to change coincident with SelectWIR. SelectWIR must be kept stable until after completion of the complete sequence which spans until clock edge T4.
• A WDR capture operation is performed at clock edge T1 with CaptureWR sampled High at T1.
• A single WDR shift operation is performed at clock edge T2 with ShiftWR sampled High at T2.
• A WDR update operation is performed at clock edge T3b with UpdateWR sampled High at T3b. Please note that the update operation occurs on the falling WRCK clock edge.
• For some IEEE1500 port instructions a capture, shift or update event may not be specified; please refer to the description of each instruction for details.

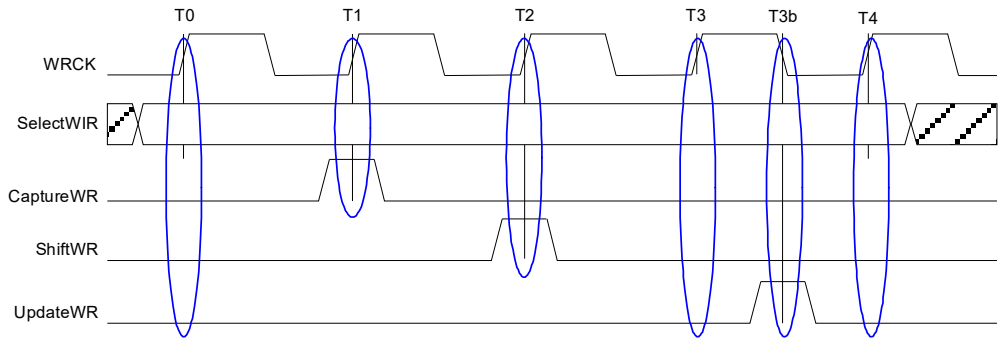


Figure 94. IEEE1500 Port Operation

13.2.2. Register Definition and Programming

Standard test registers are defined here that are accessible via IEEE Std 1500.

13.2.2.1. Wrapper Instruction Register Encodings

The HBM device is required to support a twelve bit Wrapper Instruction Register (WIR). The four most significant bits are used for channel identification and the remaining eight least significant bits encode the test instruction. When SelectWIR is asserted, the WIR will not respond to CaptureWR signal and nothing will be captured into the WIR

Table 79 - WIR Channel Selection Definition

WIR[11:8]	Channel Select
Xh	Ignored
0h	Channel a
1h	Channel b
2h	Channel c
3h	Channel d
4h	Channel e
5h	Channel f
6h	Channel g
7h	Channel h
Eh-8h	Reserved
Fh	All

Table 80 - Instruction Register Encodings

WIR[11:8]	WIR[7:0]	Instruction	Description	Data Register Type	WDR Length	Required/ Optional
Xh	00h	BYPASS	Bypass	R/W	1	Required
Fh, 7h-0h	01h	EXTEXT_RX	uBump bound-ary scan Rx test (open/ short)	R	215	Required
Fh, 7h-0h	02h	EXTEXT_TX	uBump bound-ary scan Tx test (open/ short)	W	215	Required
	03h	INTEST_RX	SK hynix Intest for HBM inputs	R	SK hynix Specific	Optional
	04h	INTEST_TX	SK hynix Intest for HBM Outputs	W	SK hynix Specific	Optional
Xh	05h	HBM_RESET	Functional reset operation of HBM	W	1	Optional
Fh, 7h-0h	06h	MBIST	DRAM resident Memory MBIST engine	R/W	SK hynix Specific	Required
7h-0h	07h	SOFT_REPAIR	Soft repair of failing DRAM bit cell	W	SK hynix Specific	Required
7h-0h	08h	HARD_REPAIR	Hard repair of DRAM fail-ing DRAM bit cell	W	SK hynix Specific	Required
Fh, 7h-0h	09h	DWORD_MISR	Return the output of DWORD MISR	R(/W)	320	Required
Fh, 7h-0h	0Ah	AWORD_MISR	Return the output of AWORD MISR	R	30	Required
Fh, 7h-0h	0Bh	CHANNEL_ID	All TX IOs from the addressed chan-nel go high.	W	1	Required
Fh, 7h-0h	0Ch	MISR_MASK	Mask MISR bit or repair ubump	W	72	Optional
Fh, 7h-0h	0Dh	AWORD_MISR_CONF IG	Set Global MRS ~ CAL, VREF, ODTS(xh) Set AC link test per channel(0h ~ 7h, Fh)	W	8	Required
Fh, 7h-0h	0Eh	DEVICE_ID	Returns the DRAM's unique identifi-cation code	R	82	Required
Xh	0Fh	TEMPERATURE	Returns an 8-bits binary temperature code	R	8	Required
Fh, 7h-0h	10h	MODE_REGISTER_D UMP_SET	Returns and set the DRAM's Mode Register values.	W/R	128	Required
Fh, 7h-0h	11h	READ_LFSR_COMPARE_-STICKY	Reads the sticky bit error for LFSR Compare feature	R	175	Required
7h-0h	12h	SOFT_LANE_REPAIR	Soft Lane Remapping	W/R	72	Required
7h-0h	13h	HARD_LANE_REPAIR	Hard Lane Remapping	W/R	72	Required
	14h ~ 17Fh	RFU				
	80h-FFh	Vendor specific				

13.2.2.2. Wrapper Data Register Types

13.2.2.2.1. Read Only (R)

WDR bit fields that are specified as read only are required to capture data into the shift stage register when a CaptureWR event is performed. The read only WDRs are required to keep their state during an UpdateWR event and are not required to have an update stage register. Read only WDRs are shifted out during a ShiftWR event. Data shifted into WSI to the shift register during the ShiftWR event is required to be don't care.

13.2.2.2.2. Write Only (W)

WDR bit fields that are specified as write only are required to update all data bits into the update stage register simultaneously when an UpdateWR event is performed. When a write only WDR is connected between WSI and WSO, any CaptureWR event would have no effect on the WDR. Write only WDRs are shifted out during the ShiftWR event.

13.2.2.2.3. Read and Write (R/W)

R/W WDRs are required to operate as merged function of write only and read only WDRs. WDR bit fields that are specified as read/write types are required to capture data bits into the shift stage register during a CaptureWR event and they are also required to update bits from the shift stage into the update stage simultaneously when the UpdateWR event is performed.

13.2.2.2.4. WDR RESET State

All WDRs are required to place their update and or shift stages where applicable in a state that ensures the HBM device returns to mission mode operation and all test modes are disabled when WRST_n is logic LOW.

Asserting WRST_n asynchronously asserts these states on the HBM device's IEEE 1500 port logic:

- Sets WIR to BYPASS, effectively clearing any prior EXTEST_RX, EXTEST_TX, INTEST_RX, INTEST_TX, or CHANNEL_ID instruction, thus returning all functional pins to their normal functional mode. Boundary scan chains content is undefined.
- No change to any previously loaded SOFT_REPAIR, HARD_REPAIR, SOFT_LANE_REPAIR, HARD_LANE_REPAIR.
- The states of the DWORD_MISR and AWORD_MISR registers are undefined.
- Any previously loaded MISR_MASK is cleared (WDR set to all 1s).
- Sets AWORD_MISR_CONFIG Enable to 0 – Off.
- Terminates and disables any MBIST hardware.

13.2.3. Test Instructions

This section will outline test instructions that are supported for the HBM device. All instructions are required to have access through the standard IEEE Std 1500 HBM test port. Test instructions are used to enable test features that will be used at the final test steps of the assembled System in Package (SiP). Please refer to the test port description for connectivity details per channel.

Unused and unimplemented instructions will default to BYPASS instruction when the WIR is updated with the unimplemented encoding. Channels that are not selected by WIR[11:8] do not respond to the instruction. Unselected channels are required to ignore any Update, Capture and Shift signals. The Capture WR, Shift WR are required to be qualified by respective channel ID WIR[11:8], WDRs are required to shift ous the least significant bit on WSO port at the first WRCK of the shift sequence. WSO output timing and valid data window are defined per IEEE std 1500 standard.

13.2.3.1. BYPSS

BYPASS instruction selects a single bit WDR and connects this register between WSI and each WSO. Upon update of the BYPASS instructions, all channels should connect their respective BYPASS register in parallel between WSI and the channel specific WSO. Data is clocked from WSI to WSO through the one bit WDR by WRCK. BYPASS should be the default instruction after assertion of WRST_n.

Wrapper Data Register

When the BYPASS instruction is updated the data register as shown in Table 81 is connected between WSI and WSO.

CaptureWR

When BYPASS is the current instruction, the CaptureWR event will have no effect. The BYPASS instruction requires only the shift stage of the data register.

UpdateWR

When BYPASS is the current instruction, the UpdateWR event will have no effect. The BYPASS instruction does not require an update register and only requires the shift register stage.

Table 81 - BYPASS Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	BYPASS	R/W	Single bit bypass register per IEEE Std 1500.

13.2.3.2. EXTEST RX

EXTEST_RX is intended for DC IO connectivity testing similar to board level boundary scan. The receive notation designates that the HBM IO will sample the logic value and capture into the data register the value that is present at the micro bump interface. All HBM bidirectional IO and inputs are required to support this instruction. HBM differential inputs and outputs are also required to support EXTEST_RX on both the true and complement pins. Optionally, vendors may support EXTEST_RX on outputs as well.

While EXTEST_RX is the current instruction, all functional pins of the selected channel(s) enter a High-Z state, including the output-only pins AERR, DERR, RDQS_t/RDQS_c, TEMP[2:0] and CATTRIP. See also "Boundary Scan".

Wrapper Data Register

When the EXTEST RX instruction is updated the data register as shown in Table 82 is connected between WSI and WSO.

CaptureWR

When EXTEST RX is the current instruction, the CaptureWR event will capture the HBM input and bidirectional IO values into the shift stage of the WDR. The captured data is shifted out WSO during subsequent ShiftWR event.

UpdateWR

When EXTEST RX is the current instruction, the UpdateWR event will have no effect.

13.2.3.3. EXTEST_TX

EXTEST TX is intended for DC IO connectivity testing similar to board level boundary scan. The transmit notation designates that the HBM IO will preload the logic value shifted into the data register at the micro bump interface. All HBM bidirectional IO and transmit only outputs are required to support this instruction. HBM differential input and output signals are also required to support EXTEST TX on both the true and complement signals. IO signals are required to power up as input mode for default state. Upon update of EXTEST TX, the IOs will change to output mode and must at least remain in output mode until RESET of the test logic or until a different instruction is updated on the channel.

Wrapper Data Register

When the EXTEST TX instruction is updated the data register as shown in Table 82 is connected between WSI and WSO as specified by the vendor.

CaptureWR

When EXTEST TX is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When EXTEST TX is the current instruction, the UpdateWR event will update the outputs and bidirectional IOs in output mode to drive the values shifted into the WDR shift stage. Outputs are required to update simultaneously.

Table 82 - EXTEST_RX and EXTEST_TX (Boundary Scan) Wrapper Data Register

Bit Position	Bit Field	Type	Description
214	TEMP0 0	O I	Signals in MIDSTACK region - channel A only - channels B to H (reserved bit)
213	TEMP1 0	O I	Signals in MIDSTACK region - channel A only - channels B to H (reserved bit)
212	TEMP2 CATTRIP 0	O O I	Signals in MIDSTACK region - channel A only - channel B only - channels C to H (reserved bit)
211:164	DWORD3		DWORD 3 (same ordering as DWORD 0)
163:116	DWORD2		DWORD 2 (same ordering as DWORD 0)
115	AERR	O	AWORD
114	RR	I	
113	R[5]	I	
112	R[4]	I	
111	CK_c	I	
110	CK_t	I	
109	R[3]	I	
108	R[2]	I	
107	R[1]	I	
106	R[0]	I	
105	RC	I	
104	C[7]	I	
103	C[6]	I	
102	C[5]	I	
101	C[4]	I	
100	CKE	I	
99	C[3]	I	
98	C[2]	I	
97	C[1]	I	
96	C[0]	I	
95:48	DWORD1		DWORD 1 (same ordering as DWORD 0)
47	DWORD0_DBI[3]		Byte 3 of DWORD 0
46	DWORD0_DQ[31]	I/O	
45	DWORD0_DQ[30]	I/O	
44	DWORD0_DQ[29]	I/O	
43	DWORD0_DQ[28]	I/O	
42	RD1	I/O	
41	DERR0	I/O	
40	DWORD0_DQ[27]	I/O	
39	DWORD0_DQ[26]	I/O	
38	DWORD0_DQ[25]	I/O	
37	DWORD0_DQ[24]	I/O	
36	DWORD0_DM[3]	I/O	

35	DWORD0_DBI[2]	I/O	Byte 2 of DWORD 0
34	DWORD0_DQ[23]	I/O	
33	DWORD0_DQ[22]	I/O	
32	DWORD0_DQ[21]	I/O	
31	DWORD0_DQ[20]	I/O	
30	RDQS_c	O	
29	RDQS_t	O	
28	DWORD0_DQ[19]	I/O	
27	DWORD0_DQ[18]	I/O	
26	DWORD0_DQ[17]	I/O	
25	DWORD0_DQ[16]	I/O	
24	DWORD0_DM[2]	I/O	
23	DWORD0_DBI[1]	I/O	Byte 1 of DWORD 0
22	DWORD0_DQ[15]	I/O	
21	DWORD0_DQ[14]	I/O	
20	DWORD0_DQ[13]	I/O	
19	DWORD0_DQ[12]	I/O	
18	WDQS_c	I	
17	WDQS_t	I	
16	DWORD0_DQ[11]	I/O	
15	DWORD0_DQ[10]	I/O	
14	DWORD0_DQ[9]	I/O	
13	DWORD0_DQ[8]	I/O	
12	DWORD0_DM[1]	I/O	
11	DWORD0_DBI[0]	I/O	Byte 0 of DWORD 0
10	DWORD0_DQ[7]	I/O	
9	DWORD0_DQ[6]	I/O	
8	DWORD0_DQ[5]	I/O	
7	DWORD0_DQ[4]	I/O	
6	RD0	I/O	
5	PAR0	I/O	
4	DWORD0_DQ[3]	I/O	
3	DWORD0_DQ[2]	I/O	
2	DWORD0_DQ[1]	I/O	
1	DWORD0_DQ[0]	I/O	
0	DWORD0_DM[0]	I/O	

13.2.3.4. INTEST_TX

INTEST RX is intended for applying test data patterns internally to the inputs of the HBM device. The receive notation designates that the HBM IO will preload the logic value shifted into the data register to the HBM Receiver. It is required that the HBM intest cell design will block the logic values at the micro bump once the HBM is in intest mode. All HBM bidirectional IO and receive only inputs are required to support this instruction.

Wrapper Data Register

When the INTEST RX instruction is updated the data register as shown in Table 83 is connected between WSI and WSO as specified by the vendor.

CaptureWR

When INTEST RX is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When INTEST RX is the current instruction, the UpdateWR event will update and apply the values shifted into the WDR shift stage to the inputs and bidirectional IOs in input mode into the HBM. All values must update and apply simultaneously.

Table 83 - INTEST_RX Wrapper Data Register

Bit Position	Bit Field	Type	Description
vendor specific	SK Hynix specific	R	Each vendor is required to provide some type of description language view or connectivity description of the HBM device describing the boundary scan connection scheme per channel ID.

13.2.3.5. INTEST_TX

INTEST TX is intended for capturing output results internal to the HBM device. The transmit notation designates that the HBM IO will capture the logic value into the data register at the transmitter output and shift the data out via the WDR after the Capture event. It is required that the HBM intest cell design will block the input logic values at the micro bump once the HBM is in INTEST TX mode. All HBM bidirectional IO and transmit only outputs are required to support this instruction.

Wrapper Data Register

When the INTEST TX instruction is updated the data register as shown in Table 84 is connected between WSI and WSO as specified by the vendor.

CaptureWR

When INTEST TX is the current instruction, the CaptureWR event will capture the internal signal values present at the HBM outputs and IOs in output mode into the shift stage of the WDR.

UpdateWR

When INTEST TX is the current instruction, the UpdateWR event will have no effect.

Table 84 - INTEST_TX Wrapper Data Register

Bit Position	Bit Field	Type	Description
vendor specific	SK Hynix specific	R	Each vendor is required to provide some type of description language view or connectivity description of the HBM device describing the boundary scan connection scheme per channel ID.

13.2.3.6. HBM RESET

The HBM RESET instruction is intended to initiate an asynchronous functional RESET of the HBM upon update, equivalent to assertion of RESET_n. MR registers and HBM functional logic is RESET upon update of HBM RESET instruction. All HBM logic is RESET except for the following exclusions:

• IEEE Std 1500 WSP is not RESET by HBM RESET instruction update

• IEEE Std 1500 controller logic is not RESET by HBM RESET instruction update

• No IEEE Std 1500 WDRs are RESET by HBM RESET instruction update

• Direct access port signal pins are not reset by HBM_RESET instruction update

Wrapper Data Register (Optional)

When the HBM RESET instruction is updated the data register as shown in Table 85 is connected between WSI and WSO as specified by the vendor. The HBM RESET WDR is optional. If no data register is implemented, then the initiation of HBM RESET is required upon update of the instruction. The vendor shall specify time period and/or WRCK requirements if they are needed to perform the RESET.

CaptureWR

When HBM RESET is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When HBM RESET is the current instruction, the UpdateWR event will load the value from the shift stage into the update stage and initiate the RESET sequence.

Table 85 - HBM_RESET Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	HBM_RESET	W	Setting this bit to 1 and updating the WDR will initiate the reset described above. The vendor shall specify time period and/or WCK requirements if they are needed to perform the reset.

The HBM_RESET condition is not self-clearing. The host must explicitly set and clear the HBM_RESET state. To accomplish an HBM reset, the HBM_RESET state should be applied a minimum duration of t_{PW_RESET} (see "Initialization Sequence with Stable Power")

Note that the implementation of the WDR is optional for the HBM_RESET instruction. If interoperability is desired across HBM designs where some designs do and other designs do not implement the WDR bit, the suggested sequence the host should apply when using HBM_RESET is:

1. Shift in and update WIR = HBM_RESET;
2. Shift in and update WDR = 1;
3. Wait t_{PW_RESET} minimum;
4. Shift in and update WDR = 0;
5. Shift in and update WIR = BYPASS.

For HBM designs that do not implement the WDR bit, steps 1 and 5 accomplish asserting and clearing the internal reset signal, and steps 2 and 4 are ignored. At step 5, other methods of clearing the HBM_RESET instruction from the WIR include shifting in and updating a different instruction, and driving WRST_n LOW.

For HBM designs that do implement the WDR bit, steps 2 and 4 accomplish asserting and clearing the internal reset state. It is recommended, but not required, to clear the HBM_RESET instruction from the WIR.

Internally, the RESET_n pin and the HBM_RESET instruction are logically combined such that when either is true then the internal reset state is true. During power-up it is required that WRST_n be driven LOW, thus ensuring that the uninitialized 1500 port logic does not interfere with the power-up initialization sequence.

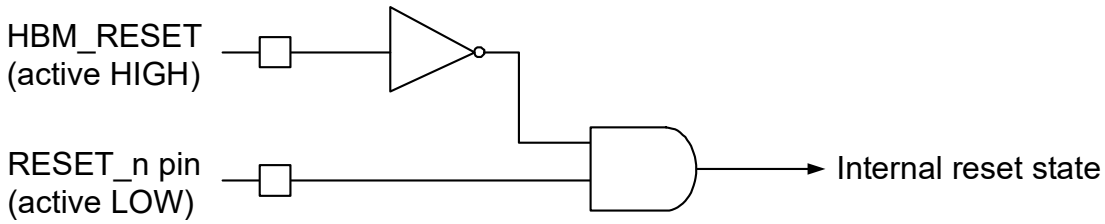


Figure 95. RESET_n and HBM_RESET Logic

After the power-up initialization, the RESET_n pin is HIGH, and subsequent stable-power resets may be asserted by either driving the RESET_n pin LOW, or by using the HBM_RESET instruction. Note that the HBM_RESET instruction may not be used to bring the HBM device out of reset while the external RESET_n pin is driven LOW. Similarly, the HBM device may not be brought out of reset using the RESET_n pin while reset is asserted using the HBM_RESET instruction.

Table 86 - RESET_n and HBM_RESET Truth Table

RESET_n	HBM_RESET	Description
0 (LOW)	0	Reset asserted by RESET_n
0 (LOW)	1	Reset asserted by both RESET_n and HBM_RESET
1 (HIGH)	0	Out of reset state
1 (HIGH)	1	Reset asserted by HBM_RESET

13.2.3.7. MBIST

The MBIST instruction is used for HBM device hosted memory built in self-test. HBM devices must support memory MBIST. This instruction format and data register field configuration is required for IEEE Std 1500 access to the test feature. MBIST engine clock source can be WRCK as a direct clock source or reference clock source or an internal clocked mode independent of WRCK and independent of any IO functional clocks is also acceptable.

Wrapper Data Register

When the MBIST instruction is updated the data register as shown in Table 87 is connected between WSI and WSO.

CaptureWR

When MBIST is the current instruction, the CaptureWR event will capture read or read/write bit fields into the shift stage of the WDR.

UpdateWR

When MBIST is the current instruction, the UpdateWR event will load the write and read/write bit fields from the shift stage to the update stage of the WDR simultaneously.

Table 87 - MBIST Wrapper Data REgister

Bit Position	Bit Field	Type	Description
MSB	MBIST_START	W	Initiates the MBIST test on the HBM. MBIST test is initiated by writing a 1 to this field and updating the WDR.
(MSB-1):0	Options and Status	R/W	SK hynix specific register

13.2.3.8. SOFT REPAIR

The SOFT REPAIR instruction allows the user to temporarily repair bit cells in the HBM without using permanent fusing mechanism to initiate the repair. This feature is intended to enable validation that the intended repair works as expected. Once a soft repair is validated, it is the user will then perform a fused hard repair via the HARD REPAIR instruction. The HBM vendor is required to specify the time to wait after updating the HARD REPAIR WDR as well as any requirements for WRCK clocking if required to perform the repair.

Wrapper Data Register

When the SOFT REPAIR instruction is updated the data register as shown in Table 88 is connected between WSI and WSO as specified by the vendor.

CaptureWR

When SOFT REPAIR is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When SOFT REPAIR is the current instruction, the UpdateWR event will load the write only bit fields from the shift stage into the update stage simultaneously. Completion of the update event will initiate the soft repair sequence.

Table 88 - SOFT_REPAIR Wrapper Data REgister

Bit Position	Bit Field	Type	Description
vendor specific	SOFT_REPAIR_START	W	Initiates the soft repair when updated.
	REPAIR_VECTOR	W	Vendor specific failing address from MBIST WDR. Vendor may also provide “logical address”-to-“repair vector” encoding.

13.2.3.9. HARD REPAIR

The HARD_REPAIR instruction is used to permanently repair failing bit cells detected in the HBM. It is required that a fuse rupture scheme is used to implement the repair. The repair sequence will be initiated on update of the data register. After some vendor specified time period fuse rupture automatically completes and repair is affected. Hard repair will be permanent. Completion of HARD_REPAIR requires a subsequent chip reset as described in "Interaction with Mission Mode Operation". The HBM vendor is required to specify the time to wait after updating the HARD_REPAIR WDR as well as any requirements for WRCK clocking if required to perform the repair.

Wrapper Data Register

When the HARD REPAIR instruction is updated the data register as shown in Table 89 is connected between WSI and WSO as specified by the vendor.

CaptureWR

When HARD REPAIR is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When HARD REPAIR is the current instruction, the UpdateWR event will load the write only bit fields from the shift stage into the update stage simultaneously. Completion of the update event will initiate the hard repair sequence.

Table 89 - HARD_REPAIR Wrapper Data Register

Bit Position	Bit Field	Type	Description
vendor specific	HARD_REPAIR_START	W	Initiates the HARD repair when updated.
	REPAIR_VECTOR	W	Vendor specific failing address from MBIST WDR. Vendor may also provide “logical address”-to-“repair vector” encoding.

13.2.3.10. DWORD MISR

This instruction is used to capture the DWORD MISR value and allows the value to be shifted out on the WSO output. The MISR in this instruction is associated with the Data Word IO test feature. Required data register bit positions are specified in the Data Register section of this instruction. Data register notation is "…_F" for bits clocked on falling edge and "…R" for bits clocked on rising edge. Note that some implementations may destroy the content of the MISR registers when read, thus the content of the MISR registers is not specified after shifting out MISR content. The host should reinitialize the MISR registers (such as MR7 Preset) before additional testing. See section "HBM Loopback Test Modes" for MISR mode features and usage.

Wrapper Data Register

When the READ DWORD MISR instruction is updated the data register as shown in Table 90 is connected between WSI and WSO.

CaptureWR

When READ DWORD MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR.

UpdateWR

When READ DWORD MISR is the current instruction, the UpdateWR event will have no effect.

Table 90 - DWORD_MISR Wrapper Data Register

Bit Position	Bit Field	Type	Description
319-240	DWORD3	R	DWORD 3(same ordering as DWORD 0)
239-160	DWORD2	R	DWORD 2(same ordering as DWORD 0)
159-80	DWORD1	R	DWORD 1(same ordering as DWORD 0)
79-60	DWORD0_BYTE3	R	Byte 3 of DWORD0 (Same ordering as BYTE0)
59-40	DWORD0_BYTE2	R	Byte 2 of DWORD0 (Same ordering as BYTE0)
39-20	DWORD0_BYTE1	R	Byte 1 of DWORD0 (Same ordering as BYTE0)

19	DWORD0_DBI0_F	R	BYTE 0 OF DWORD0
18	DWORD0_DBI0_R	R	
17	DWORD0_DQ_F[7]	R	
16	DWORD0_DQ_R[7]	R	
15	DWORD0_DQ_F[6]	R	
14	DWORD0_DQ_R[6]	R	
13	DWORD0_DQ_F[5]	R	
12	DWORD0_DQ_R[5]	R	
11	DWORD0_DQ_F[4]	R	
10	DWORD0_DQ_R[4]	R	
9	DWORD0_DQ_F[3]	R	
8	DWORD0_DQ_R[3]	R	
7	DWORD0_DQ_F[2]	R	
6	DWORD0_DQ_R[2]	R	
5	DWORD0_DQ_F[1]	R	
4	DWORD0_DQ_R[1]	R	
3	DWORD0_DQ_F[0]	R	
2	DWORD0_DQ_R[0]	R	
1	DWORD0_DM0_F	R	
0	DWORD0_DM0_R	R	

13.2.3.11. AWORD MISR

This instruction is used to capture the AWORD MISR value and allows the value to be shifted out on the configured WSO outputs. The MISR in this instruction is associated with the Address Word loopback test feature. Required data register bit positions are specified in the Data Register section of this instruction. Data register notation is "…_F" for bits clocked on falling edge and "…R" for bits clocked on rising edge. Note that some implementations may destroy the content of the MISR registers when read, thus the content of the MISR registers is not specified after shifting out MISR content. The host should reinitialize the MISR registers (such as AWORD_MISR_CONFIG Preset) before additional testing. See "HBM Loopback Test Modes" for MISR mode features and usage.

Wrapper Data Register

When the READAWORDMISR instruction is updated the data register as shown in Table 91 is connected between WSI and WSO.

CaptureWR

When READ AWORD MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR.

UpdateWR

When READ AWORD MISR is the current instruction, the UpdateWR event will have no effect.

Table 91 - AWORD_MISR Wrapper Data Register

Bit Position	Bit Field	Type	Description
29	R_F[5]	R	
28	R_R[5]	R	
27	R_F[4]	R	
26	R_R[4]	R	
25	R_F[3]	R	
24	R_R[3]	R	
23	R_F[2]	R	
22	R_R[2]	R	
21	R_F[1]	R	
20	R_R[1]	R	
19	R_F[0]	R	
18	R_R[0]	R	
17	C_F[7]	R	
16	C_R[7]	R	
15	C_F[6]	R	
14	C_R[6]	R	
13	C_F[5]	R	
12	C_R[5]	R	
11	C_F[4]	R	
10	C_R[4]	R	
9	CKE_F	R	
8	CKE_R	R	
7	C_F[3]	R	
6	C_R[3]	R	
5	C_F[2]	R	
4	C_R[2]	R	
3	C_F[1]	R	
2	C_R[1]	R	
1	C_F[0]	R	
0	C_R[0]	R	

13.2.3.12. CHANNEL ID

This instruction is intended to enable HBM channel identification. The channel(s) specified in WIR[11:8] will drive all TX IOs including RD, DM and PAR associated with the channel(s) upon update of this instruction with ENABLE=1. DM and PAR are driven even if the respective mission mode functions are disabled in the mode registers.

Wrapper Data Register (Optional)

When the CHANNELID instruction is updated the data register as shown in Table 92 is connected between WSI and WSO. The CHANNELID WDR is optional. If no data register is implemented, then the initiation of TX drive is required upon update of the instruction and all TXs return to default state when any instruction other than CHANNEL ID is updated to the WIR.

CaptureWR

When CHANNELID is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When CHANNELID is the current instruction, the UpdateWR event will load the enable bit from the shift stage into the update stage of the WDR. Completion of the UpdateWR event will initiate transmitters for the specified channel to drive based on the bit field value updated.

Table 92 - CHANNEL_ID Wrapper Data Register

Bit Position	Bit Field	Type	Description
0	ENABLE	W	Setting this bit to 1 and updating the instruction will drive all TX IOs to logical High.

13.2.3.13. MISR MASK

MISR_MASK instruction is used with AWORD MISR and DWORD MISR test modes. The DWORD MISR and AWORD MISR test modes must be configured prior to using the MISR_MASK instruction. The DWORD MISR test mode is enabled and configured via MODE_REGISTER_SET_DUMP instruction or mission mode access to Mode Register 7 and the AWORD MISR test mode is enabled and configured via the AWORD_MISR_CONFIG instruction. Updating this instruction's data register will mask out desired bit(s) during the MISR test according to the WDR bit field descriptions. See "HBM Loopback Test Modes" for MISR mode features and usage.

Wrapper Data Register

When the MISR MASK instruction is updated the data register as shown in Table 93 is connected between WSI and WSO.

CaptureWR

When MISR MASK is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When MISR MASK is the current instruction, the UpdateWR event will load the mask bit from the shift stage into the update stage of the WDR. Completion of the UpdateWR event will enable the mask for the specified MISR input. All mask values are required to update simultaneously.

Table 93 - MISR_MASK Wrapper Data Register

Bit Position	Bit Field	Type	Description
71-56	DWORD3_MASK[15:0]	W	Mask applied to DWORD 3. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
55-40	DWORD2_MASK[15:0]	W	Mask applied to DWORD 2. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
39-36	AWORD_RA_MASK[3:0]	R	Mask applied to address word. Masked bit is forced to 0 on corresponding MISR input. 0h - 5h: R0 - R5 mask 6h: CKE mask 7h - Eh: Reserved Fh: No mask. Default.
35-32	AWORD_CA_MASK[3:0]	R	Mask applied to address word.. Masked bit is forced to 0 on corresponding MISR input. 0h - 7h: C0 - C7 mask 8h - Eh: Reserved Fh: No mask. Default
31-16	DWORD1_MASK[15:0]	R	Mask applied to DWORD 1. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
15-12	DWORD0_BYTE3_MASK[3:0]	R	Mask applied to DWORD 0 Byte 3. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description
11-8	DWORD0_BYTE2_MASK[3:0]	R	Mask applied to DWORD 0 Byte 2 Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description

7-4	DWORD0_BYTE1_MASK[3:0]	R	Mask applied to DWORD 0 Byte 1. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description
3-0	DWORD0_BYTE0_MASK[3:0]	R	Mask applied to DWORD 0 Byte 0. Masked bit is forced to 0 on corresponding MISR input. 0h: DM0 Mask 1h - 8h: DQ0 - DQ7 Mask 9h: DBI Mask Ah - Eh: Reserved Fh: No mask. Default.

13.2.3.14. AWORD MISR CONFIG

This instruction will provide IEEE Std 1500 access to the AWORD MISR test instruction configuration specified in the data register. Configuration bits are set after the UpdateWR event. See "HBM Loopback Test Modes".

Wrapper Data Register

When the AWORD MISR CONFIG instruction is updated the data register as shown in Table 94 is connected between WSI and WSO.

CaptureWR

When AWORD MISR CONFIG is the current instruction, the CaptureWR event will have no effect.

UpdateWR

When AWORD MISR CONFIG is the current instruction, the UpdateWR event will load the configuration bits from the shift stage into the update stage of the WDR. Completion of the update event will enable the AWORD MISR and configure the register into the proper mode. All values are required to update simultaneously.

Table 94 - AWORD_MISR_CONFIG Wrapper Data Register

Bit Position	Bit Field	Type	Description
7-4	SKHYNIX SPECIFIC	W	Vendor will specify bit fields needed to enable and configure the AWORD MISR.
3	ENABLE	W	0 - Off 1 - On
2-0	MODE[2:0]	W	000 - Preset The AWORD MISR/LFSR is set to 0x2AAAAAAAh, the AWORD LFSR_COMPARE_STICKY bits are set to all zeros, and the AWORD preamble clock filter circuit is enabled.. 001 - Reserved 010 - Register mode AWORD transfers are captured directly to the MISR register without compression to directly set an alternate MISR seed value. Note: Register mode cannot be used to set an alternate seed value (see "Test method for AWORD (Write) Register mode") 011 - MISR mode 100 - LFSR Compare mode

13.2.3.15. DEVICE ID

This instruction allows shift out of the DEVICE ID WDR. WDR fields are required for both a global ID and a per channel ID. The per channel ID data registers are intended to support vendors who require additional resolution for identifying the device.

Wrapper Data Register

When the DEVICE ID instruction is updated the data register as shown in Table 95 is connected between WSI and WSO.

CaptureWR

When DEVICE ID is the current instruction, the CaptureWR event will load the respective identification field values into the shift stage of the WDR.

UpdateWR

When DEVICE ID is the current instruction, the UpdateWR event will have no effect.

Table 95 - DEVICE_ID Wrapper Data Register

Bit Position	Bit Field	Type	Description
81	GEN2_TEST	R	Gen-2 feature support: – Lane Remapping modes 1 & 2 with hard/soft repair and readable – RD, RR, RC micro-bumps in the BScan chains – MISR Preset to 0xAAAAAh / 0x2AAAAAAAh – MISRs writable for setting seeds (optional) – LFSR Compare – 3-bit AWORD_MISR_CONFIG – MISR/LFSR Compare features expect and preamble clock filter 0 - features not support 1 - features supported
80	ECC	R	ECC support 0 - no ECC support 1 - ECC supported
79-76	DENSITY	R	Memory density per channel. 0000 - Reserved 0001 - 1 Gb 0010 - 2 Gb 0011 - 4 Gb 0100 - 8 Gb 0101 - 16 Gb 0110 - 32 Gb 0111 - Reserved 1xxx - Reserved
75-72	MANUFACTURER_ID[3:0]		0000 - Reserved 0001 - Samsung 0010 - Reserved 0011 - Reserved 0100 - Reserved 0101 - Reserved 0110 - SK Hynix 0111 .. 1110 - Reserved 1111 - Micron
71-68	MANUFACTURING_LOCATION[3:0]	R	SKHYNIX SPECIFIC
67-60	MANUFACTURING_YEAR[7:0]	R	Binary encoded year from 2011 2011 = 00000000; 2015 = 00000100
59-52	MANUFACTURING_WEEK[7:0]	R	Binary encoded week WW52 = 00110100

51-18	SERIAL_NUMBER[33:0]	R	Unique ID per device
17-16	ADDRESSING_MODE[1:0]	R	Addressing Mode Support 01 = Only Pseudo Channel Mode Supported 10 = Only Legacy Mode Supported 00 = Illegal 11 = Illegal
15-8	CHANNEL_AVAILABLE	R	Channel Available 0 - Channel not present / not working 1 - Channel present / working Channel encoding (1 bit per channel): [0]: channel a [1]: channel b ... [6]: channel g [7]: channel h
7	HBM_STACK_HEIGHT	R	HBM Stack Height 0 = 2- or 4-High Stack 1 = 8-High Stack
6-0	MODEL_PART_NUMBER	R	SK HYNIX RESERVE

13.2.3.16. TEMPERATURE

This instruction captures the temperature sensor reading from the WDR. The digital value of the HBM temperature sensor is latched into the data register on Capture and shifted out on WSO. Temperature reporting in this register is specified as an 8-bit field. The MSB indicates temperature sensor valid status. The remaining 7 bits indicate the temperature in degrees Celsius.

Wrapper Data Register

When the TEMPERATURE instruction is updated the data register as shown in Table 96 is connected between WSI and WSO.

CaptureWR

When TEMPERATURE is the current instruction, the CaptureWR event will load the respective temperature field values into the shift stage of the WDR.

UpdateWR

When TEMPERATURE is the current instruction, the UpdateWR event will have no effect.

Table 96 - TEMPERATURE Wrapper Data Register

Bit Position	Bit Field	Type	Description
7	VALID[0]	R	Temperature sensor output valid 0 - Valid 1 - Invalid
6-0	TEMP[6:0]	R	Temperature in Degrees Celsius. Examples: 7'b 0000000 = 0 oC (or less) 7'b 0011001 = 25 oC 7'b 1111111 = 127 oC

13.2.3.17. MODE REGISTER DUMP SET

This instruction provides IEEE Std 1500 access to read and write the HBM Mode Registers. When this instruction is updated into the WIR, the Mode Registers values are loaded into the MODE REGISTER DUMP SET WDR on Capture and the values in the shift data register are updated to the Mode Register upon update. During a Capture event the existing MR state should be preserved while not affecting device operation. Per channel MR is accessed by selected channel WIR[11:8]. All channel select, WIR[11:8] = 4'hF, captures all MR values in parallel into each channel's WDR and shifts out each channel's WSO in parallel.

Wrapper Data Register

When the MODE REGISTER DUMP SET instruction is updated the data register as shown in Table 97 is connected between WSI and WSO.

CaptureWR

When MODE REGISTER DUMP SET is the current instruction, the CaptureWR event will capture bit fields into the shift stage of the WDR. The MODE REGISTER DUMP SET instruction is required to allow bit fields that correspond to unimplemented MRs to capture an unknown 'X' value.

UpdateWR

When MODE REGISTER DUMP SET is the current instruction, the Update WR event will load the bit fields from the shift stage to the update stage of the WDR simultaneously. When the update event is complete the mode register settings are required to take effect.

Table 97 - MODE_REGISTER_DUMP_SET Wrapper Data REgister

Bit Position	Bit Field	Type	Description
127-120	MR15	R/W	MR15[7:0]
119-112	MR14	R/W	MR14[7:0]
111-104	MR13	R/W	MR13[7:0]
103-96	MR12	R/W	MR12[7:0]
95-88	MR11	R/W	MR11[7:0]
87-80	MR10	R/W	MR10[7:0]
79-72	MR9	R/W	MR9[7:0]
71-64	MR8	R/W	MR8[7:0]
63-56	MR7	R/W	MR7[7:0]
55-48	MR6	R/W	MR6[7:0]
47-40	MR5	R/W	MR5[7:0]
39-32	MR4	R/W	MR4[7:0]
31-24	MR3	R/W	MR3[7:0]
23-16	MR2	R/W	MR2[7:0]
15-8	MR1	R/W	MR1[7:0]
7-0	MR0	R/W	MR0[7:0]

13.2.3.18. READ_LFSR_COMPARE_STICKY

This instruction is used to capture the LFSR Compare Sticky error data to be shifted out on the WSO output. The register in this instruction is associated with the AWORD and DWORD IO loop back test features. Required data register bit positions are specified in the Data Register section of this instruction in Table 98. Note that some implementations may destroy the content of the related MISR registers when the sticky error data is read, thus the content of the MISR registers is not specified after shifting out sticky error content. The host should reinitialize the MISR registers (such as with MR7 Preset and AWORD_ MISR_CONFIG preset) before additional testing. See section 6.12 for MISR mode features and usage.

While both the AWORD and DWORD sticky error bits share this common WDR, the bits are set and cleared only by their respective AWORD or DWORD Preset and LFSR Compare operations. For example, an AWORD_MISR_CONFIG Preset operation is defined to clear the AWORD sticky error bits, and the state of the DWORD sticky error bits is undefined; therefore, the host should ignore the DWORD sticky error bits when operating the AWORD LFSR Compare mode. Conversely, the DWORD_MISR_CONFIG Preset operation is defined to clear the DWORD sticky error bits, and the state of the AWORD sticky error bits is undefined; therefore, the host should ignore the AWORD sticky error bits when operating the DWORD LFSR Compare mode.

Wrapper Data Register

When the READ_LFSR_COMPARE_STICKY instruction is updated the data register as shown in Table 98 is connected between WSI and WSO.

Capture WR

When READ READ_LFSR_COMPARE_STICKY is the current instruction, the Capture WR event will load the sticky error values into the shift stage of the WDR.

Update WR

When READ_LFSR_COMPARE_STICKY is the current instruction, the Update WR event will have no effect.

Table 98 - READ_LFSR_COMPARE_STICKY Wrapper Data Register

Bit Position	Bit Field	Type	Description
174	DWORD3_DBI[3]	R	BYTE3 OF DWORD3
173	DWORD3_DQ[31]	R	
172	DWORD3_DQ[30]	R	
171	DWORD3_DQ[29]	R	
170	DWORD3_DQ[28]	R	
169	DWORD3_DQ[27]	R	
168	DWORD3_DQ[26]	R	
167	DWORD3_DQ[25]	R	
166	DWORD3_DQ[24]	R	
165	DWORD3_DM[3]	R	
164-155	DWORD3_BYTE2	R	BYTE2 OF DWORD3 (SAME BIT ORDERING AS BYTE3)
154-145	DWORD3_BYTE1	R	BYTE1 OF DWORD3 (SAME BIT ORDERING AS BYTE3)
144-135	DWORD3_BYTE0	R	BYTE0 OF DWORD3 (SAME BIT ORDERING ASBYTE3)
134-95	DWORD2	R	DWORD2(SAME BIT ORDERING AS DWORD3)

94	R[5]	R	AWORD
93	R[4]	R	
92	R[3]	R	
91	R[2]	R	
90	R[1]	R	
89	R[0]	R	
88	C[7]	R	
87	C[6]	R	
86	C[5]	R	
85	C[4]	R	
84	CKE	R	
83	C[3]	R	
82	C[2]	R	
81	C[1]	R	
80	C[0]	R	
79-40	DWORD1	R	DWORD1(SAME BIT ORDERING AS DWORD3)
39-0	DWORD0	R	DWORD0 (SAME BIT ORDERING AS DWORD3)

13.2.3.19. SOFT_LANE_REPAIR and HARD_LANE_REPAIR

The SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions are used to convey lane remapping and repair information. Both instructions use the same LANE_REPAIR WDR.

Wrapper Data Register

When SOFT_LANE_REPAIR or HARD_LANE_REPAIR is the current instruction, the LANE_REPAIR wrapper data register as shown in Table 99 is connected between WSI and WSO.

Please note that the encoding of the LANE_REPAIR WDR has intentionally been defined similar to the MISR_MASK WDR, to allow DRAM vendors to share hardware resources for both WDRs.

Figure 95 illustrates the interaction between SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions and the associated registers. It is pointed out that the actual I/O lane remapping is derived from the content of the lane repair shadow register.

CaptureWR

When either SOFT_LANE_REPAIR or HARD_LANE_REPAIR is the current instruction, the CaptureWR event will load the lane remapping data from the lane repair shadow register into the shift stage of the WDR. This internal lane repair shadow register is pre-loaded with the repair data from a preceding HARD_LANE_REPAIR operation upon HBM device initialization (RESET_n pulled Low). The memory controller may use these data to configure the lane repair accordingly at the ASIC; it may also use these data as a seed value for subsequent lane repair operations.

UpdateWR

When SOFT_LANE_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the lane repair shadow register and force the I/O lanes to be remapped accordingly. This remapping is non-persistent; it will be lost when RESET_n is pulled low or the device looses power. Pulling WRST_n low does not reset the lane repair shadow register.

When HARD_LANE_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the hard lane repair register. The controller must wait t_{HLREP} to allow the device to complete this operation and permanently store the repair vector.

Only a single broken lane can be repaired at a time, in order to limit the current constraint of the associated circuits. If multiple lanes are to be repaired, it is required to shift in the repair vectors for each broken lane sequentially, with all other lane repair setting = Fh, and initiate each actual lane repair with a separate UpdateWR event.

The UpdateWR event itself does not lead to an actual re-mapping of the I/O lanes. For such re-mapping to get effective it is required to initiate an HBM chip reset by pulling RESET_n Low, which copies the repair vector from the hard lane repair register into the lane repair shadow register as shown in Figure 96.

Table 99 - LANE_REPAIR Wrapper Data Register

Bit Position	Bit Field	Type	Description
71-56	DWORD3[15:0]	R/W	Lane remapping applied to DWORD 3. Encoding shown in DWORD0 description.
55-40	DWORD2[15:0]	R/W	Lane remapping applied to DWORD 2. Encoding shown in DWORD0 description.
39-36	AWORD_RA[3:0]	R/W	Lane remapping applied to address word. 0h - 5h: R0 - R5 6h - Eh: Reserved Fh: No lane remapping. Default.
35-32	AWORD_CA[3:0]	R/W	Lane remapping applied to address word. 0h - 7h: C0 - C7 8h - Eh: Reserved Fh: No lane remapping. Default.
31-16	DWORD1[15:0]	R/W	Lane remapping applied to DWORD 1. Encoding shown in DWORD0 description.
15-12	DWORD0_BYTE3[3:0]	R/W	Lane remapping applied to DWORD 0 byte 3. Encoding shown in DOWRD0_BYTE0 description.
11-8	DWORD0_BYTE2[3:0]	R/W	Lane remapping applied to DWORD 0 byte 2. Encoding shown in DWORD0_BYTE0 description.
7-4	DWORD0_BYTE1[3:0]	R/W	Lane remapping applied to DWORD 0 byte 1. Encoding shown in DWORD0_BYTE0 description.
3-0	DWORD0_BYTE0[3:0]	R/W	Lane remapping applied to DWORD 0 Byte 0. 0h: DM0 1h - 8h: DQ0 - DQ7 9h: DBI for lane remapping using Mode 2. Reserved for lane remapping using Mode 1. Ah - Dh: Reserved Eh: Reserved for lane repair using Mode 1. Enables/disables RD pin with lane repair in other byte using Mode 2. Fh: No lane remapping. Default.

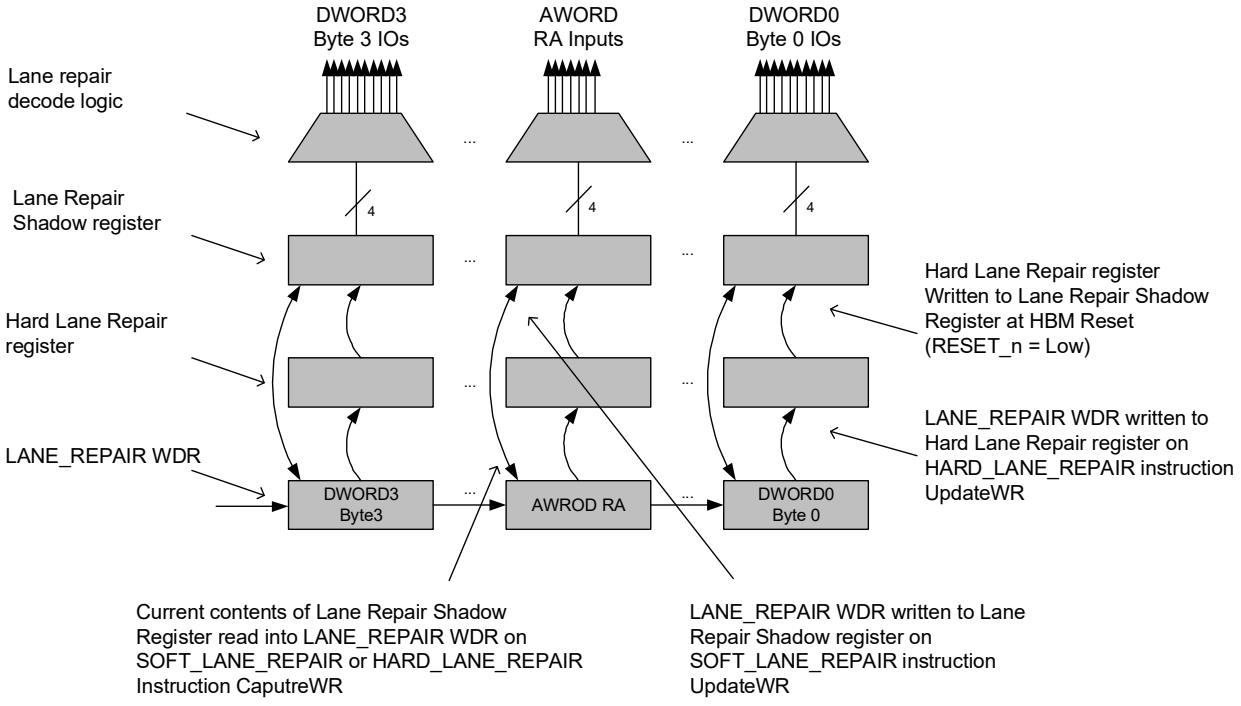


Figure 96. Registers associated with Lane Repair Instructions

13.2.4. Interaction with Mission Mode Operation

Table 100 defines the interaction of the various IEEE 1500 port instructions with mission mode operation, and any instruction exit requirements (see also Table 80 for all IEEE1500 instructions).

Table 100 - IEEE1500 PORT INSTRUCTION INTERACTIONS

Instruction	Interaction with Mission Mode	Post Instruction Requirements
BYPASS DWORD_MISR (1) AWORD_MISR (1) MISR_MASK (1) READ_LFSR_COMPARE_STICKY (1) DEVICE_ID TEMPERATURE MODE_REGISTER_DUMP_SET (dump)	Instructions may be used at any time. Core memory content is retained if refresh specifications are met.	None
SOFT_REPAIR (2) SOFT_LANE_REPAIR (2) MODE_REGISTER_DUMP_SET (set) AWORD_MISR_CONFIG (3)	Core memory content is retained if refresh specifications are met.	Meet IEEE1500 Port AC Timings (see Table 101)
EXTEST_RX, EXTEST_TX INTEST_RX, INTEST_TX MBIST CHANNEL_ID HARD_REPAIR (4) HARD_LANE_REPAIR (4)	HBM interface state and core memory content is not defined.	Reset
NOTE 1 While accessing these MISR-related registers has no interaction with mission mode, operating the AWORD and DWORD MISR modes may result in memory content loss unless the channel is put into self-refresh mode. See "HBM Loopback Test Modes". NOTE 2 Soft memory array and lane repairs imply that memory content is at least partially incorrect. While the HBM device imposes no restrictions on the interface state and memory content, the host should consider the health of the memory content based on the repair(s) being applied. NOTE 3 See "HBM Loopback Test Modes" for proper sequencing of the AWORD MISR test modes. NOTE 4 Hard memory array and lane repairs involve blowing fuses. Normal operation on any channel is not supported when the hard repair operations are used. A reset is required after hard repair operations before returning the HBM to normal operation.		

13.2.5. IEEE1500 Port AC Timing Parameters

Table 101 - IEEE1500 Port AC Timings 1,2

Parameter	Symbol	Value		Unit	Notes
		MIN	MAX		
IEEE 1500 Port I/O Timings					
WRCK clock period	t_{CKTP}	20		ns	
WRCK clock high pulse width	t_{CKTPH}	0.45		t_{CKTP}	
WRCK clock low pulse width	t_{CKTPL}	0.45		t_{CKTP}	
WRST_n pulse width low	t_{WRSTL}	100		ns	
IEEE1500 port operation after WRST_n deassertion	t_{WINIT1}	3		t_{CKTP}	
Rising WRST_n edge to WRCK setup time	t_{SWRST}			ns	
WSP input setup time to WRCK rising edge	t_{SR}			ns	3
WSP input hold time from WRCK rising edge	t_{HR}			ns	3
WSP input setup time to WRCK falling edge	t_{SF}			ns	4
WSP input hold time from WRCK falling edge	t_{HF}			ns	4
WSO output valid time from WRCK falling edge	t_{OVWSO}			ns	5
EXTEST_RX Instruction RElated Timings					
Input setup time to WRCK rising edge	t_{SEXT}		-	ns	6
Input hold time from WRCK rising edge	t_{HEXT}		-	ns	6
EXTEXT_TX Instruction Related Timing					
Output valid time from WRCK falling edge	t_{OVEXT}		-	ns	7
HBM_RESET Instruction Related Timing					
HBM_RESET Instructionminimum active time	t_{RES}	t_{INT1}	-	ns	8
SOFT_REPAIR and HARD_REPAIR Instruction Related Timings					
SOFT_REPAIR minimum waiting time	t_{SREP}		-	ns or µs	9
HARD_REPAIR minimum waiting time	t_{HREP}		-	ns or µs	10
DWORD_MISR and AWORD_MISR Instruction RElated Timing					
DWORD and AWORD MISR data capture to WDR data capture delay	t_{SMISR}		-	ns	11
CHANNEL_ID Instruction Related Timings					
Output high time from WRCK falling edge	t_{OVCHN}			ns	12
Output return to default state delay	t_{OZCHN}			ns	13
MODE_REGISTER_DUMP_SET Instruction Related Timings					
WDR update to Mode REgister valid delay	t_{UPDMR}		-	ns	14
MRS command to WDR data capture delay	t_{MRSS}	t_{MOD}	-	nCK	15
AWORD_MISR_CONFIG and MISR_MASK Instruction Related Timings					
AWORD MISR config. or AWORD Mask config. to MISR operation delay	t_{CMISR}		-	ns	16
SOFT_LANE_REPAIR and HARD_LANE_REPAIR Instruction Related Timings					
SOFT_LANE_REPAIR minimum waiting time	t_{SLREP}		-	ns or µs	17
HARD_LANE_REPAIR minimum waiting time	t_{HLREP}		-	ns or µs	18

NOTE 1 AC timing parameters apply to each channel of the HBM device independently except for timings related to IEEE1500 input pins that are common to all channels. No timing parameters are specified across channels, and all channels operate independently of each other.

NOTE 2 All parameters assume proper device initialization.

NOTE 3 Parameter applies to WSI, SelectWIR, ShiftWR and CaptureWR inputs.

NOTE 4 Parameter applies to UpdateWR input.

NOTE 5 Parameter applies to WSO output changes resulting from Wrapper Instruction Register (WIR), Wrapper Bypass Register (WBY) or any Wrapper Data Register (WDR) shift operation.

NOTE 6 Parameter applies to all HBM inputs and bidirectional IOs in the CaptureWR cycle when the active instruction is EXTEST_RX.

NOTE 7 Parameter applies to all HBM outputs and bidirectional IOs in the UpdateWR cycle when the active instruction is EXTEST_TX.

NOTE 8 Parameter applies when the active instruction is HBM_RESET; it is measured from either the falling WRCK edge that loads the HBM_RESET instruction in the UpdateWIR cycle (in case no WDR is associated with the instruction) or the falling WRCK edge that sets the WDR bit to '1' in the UpdateWR cycle (in case a WDR is associated with the instruction) until either the HBM_RESET instruction is invalidated or the WDR bit is set back to '0'. The minimum value equals the RESET_n minimum low time with stable power.

NOTE 9 Parameter applies when the active instruction is SOFT_REPAIR; it describes the minimum time for the HBM device to perform the internal soft repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.

NOTE 10 Parameter applies when the active instruction is HARD_REPAIR; it describes the minimum time for the HBM device to perform the internal hard repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.

NOTE 11 Parameter applies when the active instruction is DWORD_MISR or AWORD_MISR; it is measured from the last CK clock that updates the data in the respective MISR until the rising WRCK edge associated with the CaptureWR cycle that copies the MISR data into the WDR shift register.

NOTE 12 Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets the CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '1' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs return to their default state.

NOTE 13 Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets any instruction other than CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '1' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs drive a High.

NOTE 14 Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the Mode Registers from the WDR shift register until any valid command other than RNOP and CNOP can be issued at the command interface.

NOTE 15 Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the last MRS command that loads any Mode Register and the rising WRCK edge in the CaptureWR cycle that copies the Mode Register content into the WDR shift register.

NOTE 16 Parameter applies when the active instruction is AWORD_MISR_CONFIG or MISR_MASK; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the AWord MISR configuration or MISR mask data until the MISR configuration is valid for any subsequent AWORD or DWORD MISR operation in the CK clock domain.

NOTE 17 Parameter applies when the active instruction is SOFT_LANE_REPAIR; it describes the minimum time for the HBM device to perform the internal soft lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.

NOTE 18 Parameter applies when the active instruction is HARD_LANE_REPAIR; it describes the minimum time for the HBM device to perform the internal hard lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.

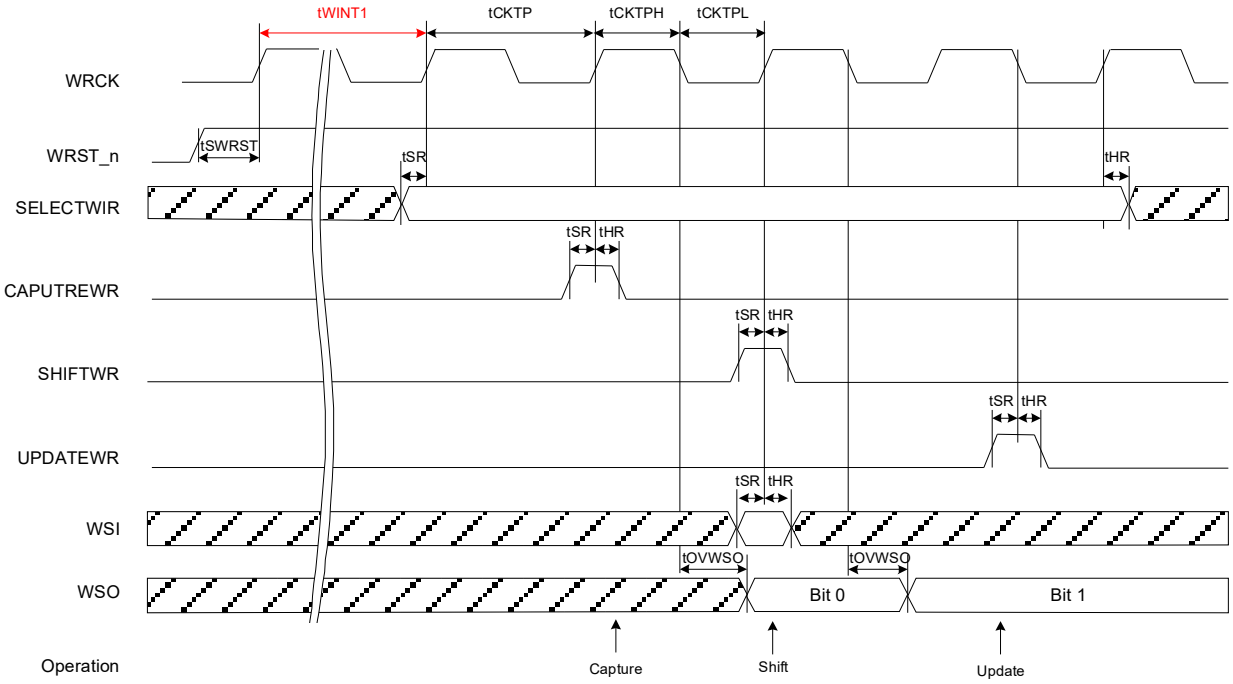


Figure 97. IEEE1500 Port Input and Output Timings

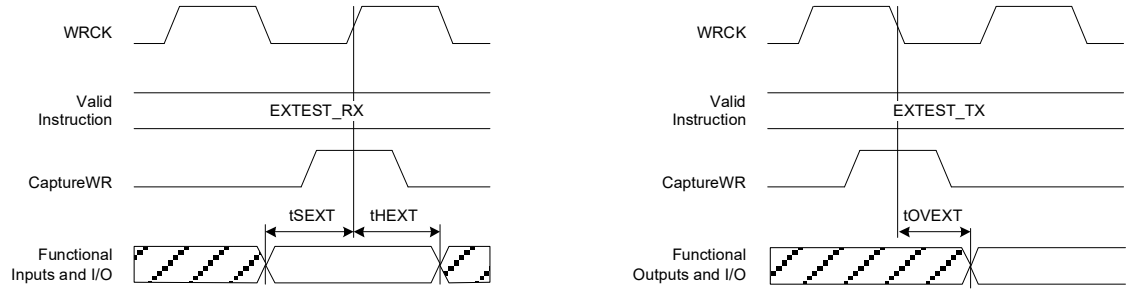


Figure 98. IEEE1500 EXTEST_RX and EXTEST_TX Instruction Related Timings

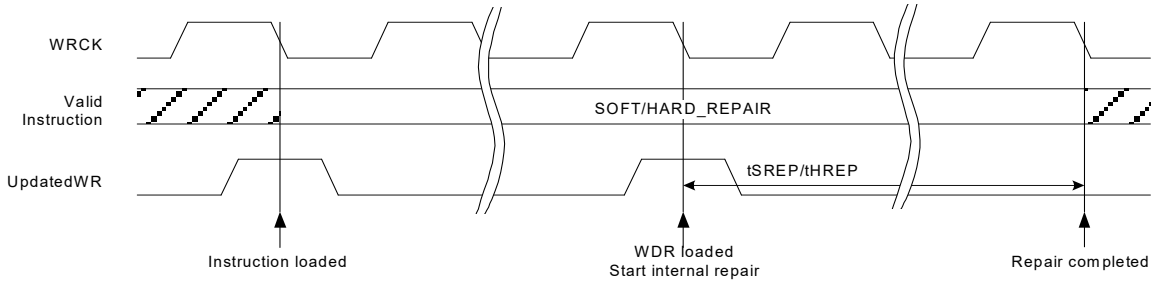


Figure 99. IEEE1500 SOFT_REPAIR and HARD_REPAIR Instruction Related Timings

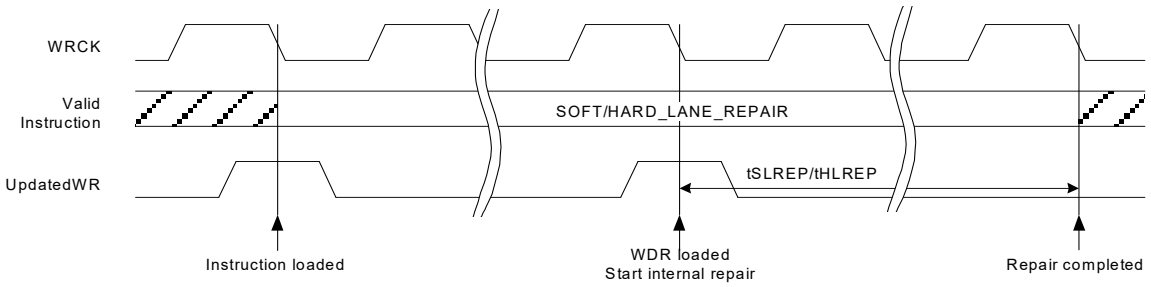
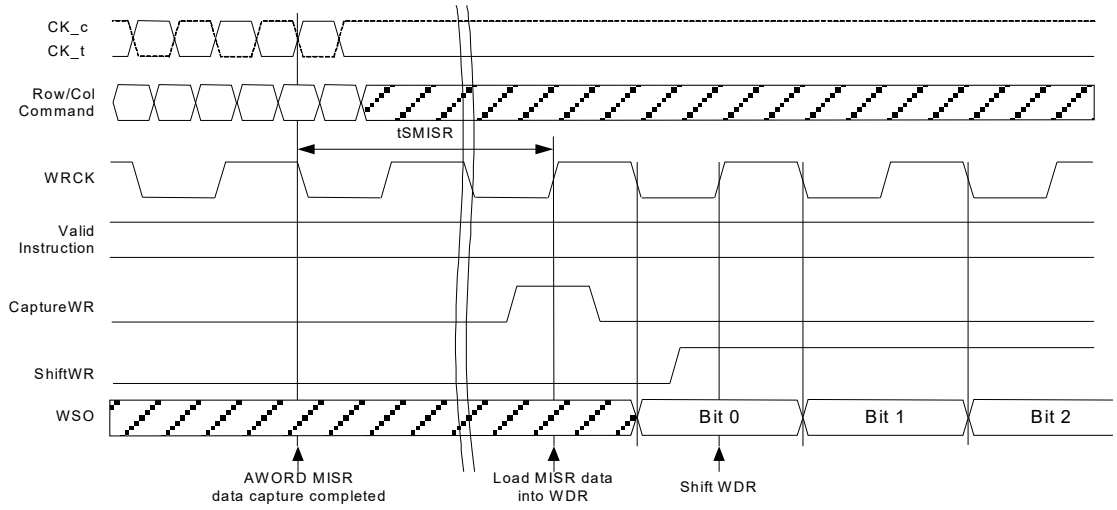
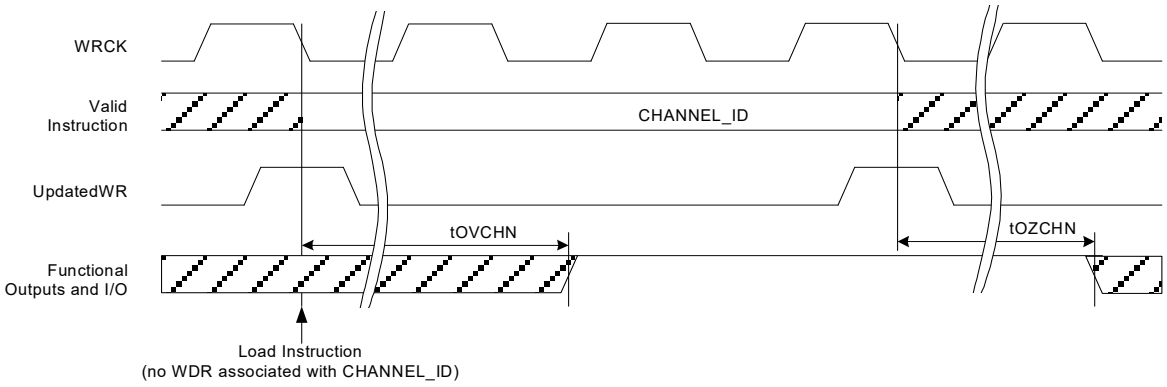


Figure 100. IEEE 1500 SOFT_LANE_REPAIR and HARD_LANE_REPAIR Instruction related Timings



Note 1 : Same timings for data inputs and DWORD MISR with DWORD_MISR instruction.
Note 2 : tOVWSO = 0 for illustration purpose.

Figure 101. IEEE1500 DWORD_MISR / AWORD_MISR Instruction Related Timings



Note : tOCVHN and tOZCHN refer to set/reset of Enable bit in WDR if optional WDR is implemented with CHANNEL_ID instruction

Figure 102. IEEE1500 CHANNEL_ID Instruction Related Timings

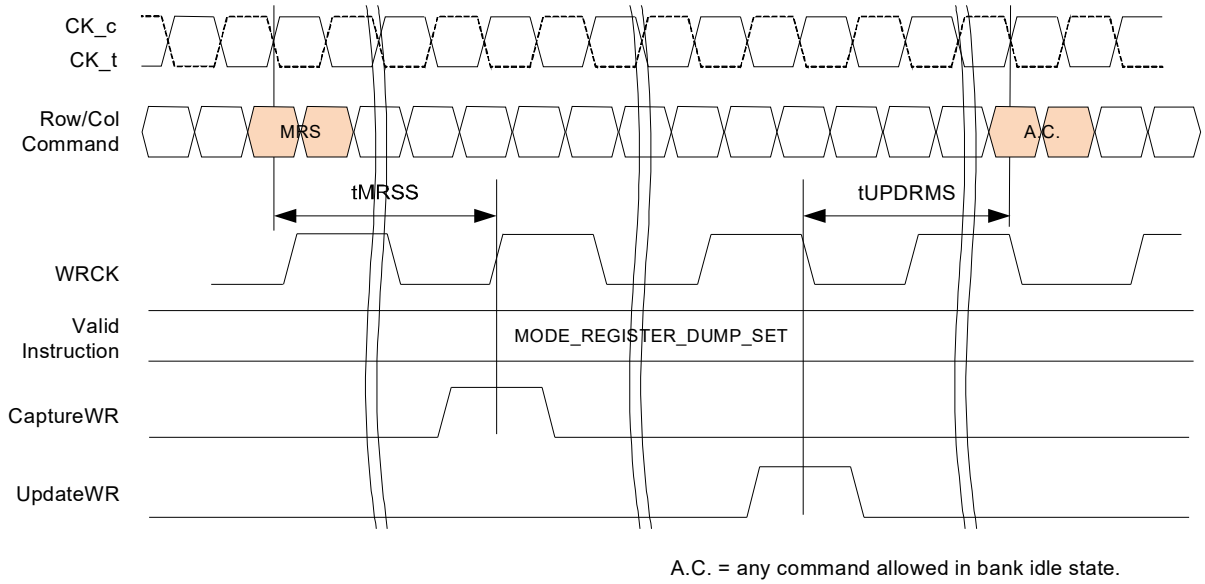


Figure 103. IEEE1500 MODE_REGISTER_DUMP_SET Instruction Related Timings

13.3. Boundary Scan

The HBM DRAM implements a boundary scan chain per channel via the IEEE 1500 port. The boundary scan operation is associated with IEEE1500 port instructions "EXTEST_TX" and "EXTEST RX".

Scan data is shifted in through WSI and out through the respective WSO, based on the active channel selections in the WIR (see Table 79). All functional pins are included in the boundary scan chains. Table 82 lists the micro-bump boundary scan chain order. Bit position 0 is the first bit shifted in on WSI and out on the WSOs.

Four pins in the mid-stack area are routed to the channel a and b scan chains: TEMP[2:0] are associated with channel a, and CATTRIP is associated with channel b. The boundary scan chain length for all channels is 215 bits, with dummy WDR bit padding as needed on the MSB end of the chains. Matched length boundary scan chains allows all channel chains to be loaded with matching data with one shift operation when WIR[11:8] = Fh.

Specific bits within the boundary scan chains are input-only, output-only or input/output (bidirectional), consistent with the micro-bump functional definitions. For example, the row and column command signals are functional inputs, and are defined as input-only (EXTEST_RX only) in the boundary scan chains. The state captured on EXTEST_RX for output pins is undefined.

While EXTEST_RX is the current instruction, all functional pins of the selected channel(s) enter a High-Z state, including the output-only pins AERR, DERR, RDQS_t/RDQS_c, TEMP[2:0] and CATTRIP.

Optionally (vendor specific), the input-only and output-only pins may be implemented as bi-directionals to aid in SIP package level testing and fault isolation. If an HBM implementation supports bidirectional boundary scan, then all pins will support both EXTEST_RX and EXTEST_TX operations. During EXTEST_RX, all pins will float and capture, including pins that are functional outputs (AERR, DERR, RDQS_t/RDQS_c, TEMP[2:0] and CATTRIP). Similarly, during EXTEST_TX, all pins will output the boundary scan chain states, including the input-only pins (the AWORD signals and WDQS_t/WDQS_c).

Note that a host design should consider possible contention if the HBM device should support driving of signals that are normally inputs during EXTEST_TX.

Scan mode entry may be asserted at any time after device initialization and during normal memory operation including when the HBM memory device is in power-down or self refresh mode. All I/O buffers are enabled when either EXTEST_RX or EXTEST_TX is the current instruction. Upon exiting the scan mode, the states of the HBM memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required before returning to normal operation.