野马士YeMaS

DDR4 UDIMM Memory Module Specifications

288pin Unbuffered DDR4 2Rx8 16GB UDIMM

Part Number

YMSDN4X-16S26C

Datasheet

V1.0

Ordering Information

Memory Type	Density	Speed (MT/S)	Organization	Component Composition	#of ranks
DDR4 UDIMM 16G	16GB	2666	1024Mx64bit	1024X8 16c	2

Description

YeMaS DDR4 UDIMM high-speed memory module that uses 16pcs of 1024Mx8 bits DDR4 SDRAM in FBGA package and a 4K bits Serial EEPROM on a 288-pin printed circuit board. YeMaS DDR4 UDIMM is Dual-Rank Dual In-Line Memory Module and is intended for mounting into 288-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- VDD = VDDQ = 1.2V ±60mV
- VPP = 2.5V, –125mV/+250mV
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- TC of 0°C to 85°C– 64ms, 8192-cycle refresh at 0°C to 85°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 bit pre-fetch
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write and read leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort • Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination(ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)

- Per-DRAM addressability
- Post package repair (PPR) and soft post package repair (sPPR) modes
- JEDEC JESD-79-4 compliant

Addressing

Parameter	1024Meg × 8bit
Number of bank groups	4
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row addressing	32K (A[15:0])
Column addressing	1K (A[9:0])
Page size	1KB

x8 Package Ball out (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c				DM_n/DBI_n TDQS_t	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

Pin Assignments

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DMO n,DBIO n,NC	151	VSS	78	EVENT n	222	PARITY
8	NC	152	DQS$_0$ c	79	A0	223	VDD
9	VSS	153	DQS0 t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DM1 n,DBI1 n,NC	162	VSS	89	CS1 n	233	VDD
19	NC	163	DQS1 c	90	VDD	234	NC
20	VSS	164	DQS1 t	91	ODT1	235	NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	NC	237	NC,CS3 n,C1
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DM4 n,DBI4 n,NC	243	VSS
29	DM2 n,DBI2 n,NC	173	VSS	100	NC	244	DQS4 c
30	NC	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45

Pin	Front Side	Pin	Back Side	Pin	Front Side	Pin	Back Side
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	DM5 n,DBI5 n, NC	254	VSS
40	DM3 n, DBI3 n,NC	184	VSS	111	NC	255	DQS5_c
41	NC	185	DQS3 c	112	VSS	256	DQS3 t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4,NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5, NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1, NC	121	DM6_n,DBI6 n,NC	265	VSS
51	DM8_n,DBI8_ n,NC	195	VSS	122	NC	266	DQS6_c
52	NC	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6, NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7, NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3, NC	128	DQ60	272	VSS
58	RESET n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	DM7_n,DBI7_ n,NC	276	VSS
62	ACT_n	206	VDD	133	NC	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT n	135	DQ62	279	VSS
65	A12/BC n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	213	VDD	139	SA0	283	VSS
69	A6	214	A5	140	SA1	284	VDDSPD
70	VDD	215	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I2C slave address select for SPD/TS
RAS_n	SDRAM row address strobe	VDD	SDRAM core & I/O power supply (1.2V ±0.06V)
CAS_n	SDRAM column address strobe	VPP	SDRAM activating power supply
WE_n	SDRAM write enable	VREFCA	SDRAM command/address reference supply
CS0_n, CS1_n	Rank Select Lines	VSS	Power supply return (ground)
CKE0, CKE1	SDRAM clock enable lines	VDDQ	SDRAM I/O power supply (1.2V ±0.06V)
ODT0, ODT1	SDRAM on-die termination control lines	VSSQ	Power supply return for I/O buffers
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	RESET_n	Set SDRAMs to a Known State
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	VTT	Termination supply for the Address, Command and Control bus
DM0_n–DM8_n	SDRAM data masks / DBI_n for data bus inversion	NC	No connection
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)		
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

Input/Output Pin Functional Descriptions

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15, and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other command defined in command truth table.
DM_n/DBI_n	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be

Symbol	Type	Function
		accessed during a MRS cycle. For x4/8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components, only BG0 is valid.
BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/ BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
DQS_t, DQS_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.
SA0, SA1	Input	Device address for the SPD.
RFU	—	Reserved for Future Use. No on DIMM electrical connection is present.
NC	—	No Connect: No on DIMM electrical connection is present.
VSS	Supply	Ground (core).
VSSQ	Supply	Ground (I/O).
VTT	Supply	Termination Power Supply: 0.6 V for Address, Command and Control bus.
VREFCA	Supply	Reference voltage for CA (Command/Address) bus.
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD.
SCL, SDA	I/O	I2C serial bus clock and data line for SPD/TS.
SA2	Input	SPD slave address select for SPD/TS.

Note:

1.For PC4, VDD 1.2V. For PC4L VDD is TBD.

2. For PC4, VTT is 0.6V. For PC4L VTT isTBD.

AC & DC Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Operating Temperature Range	0 to 85	°C	1,2

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.

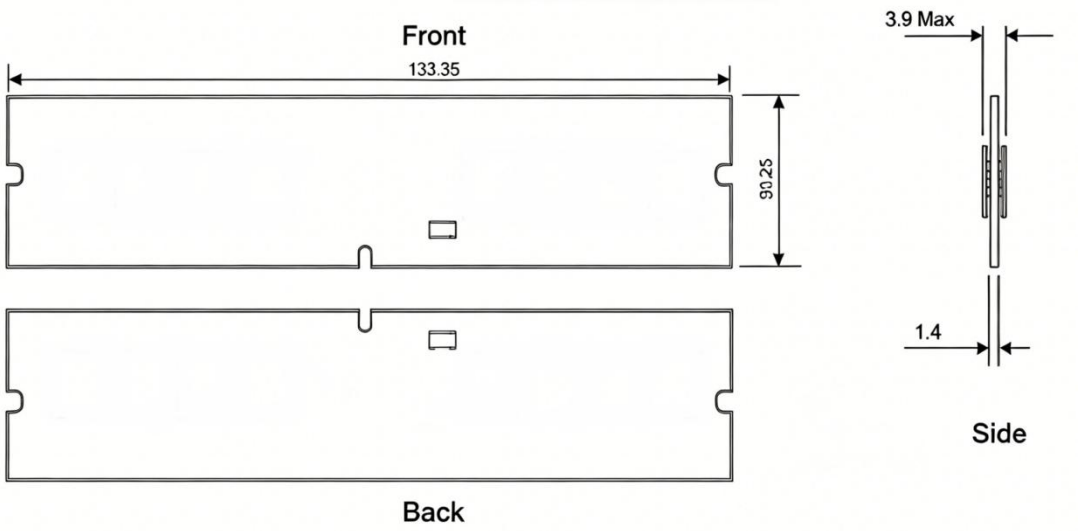
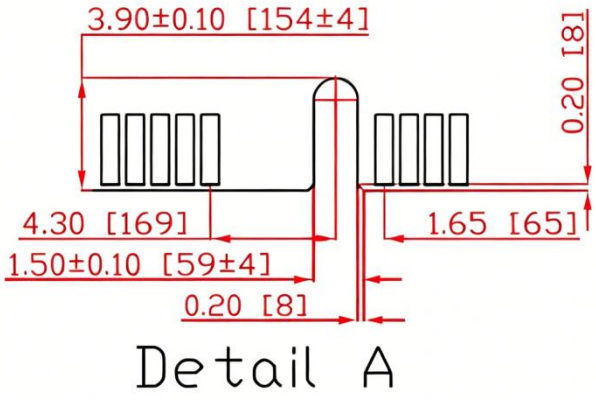
Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
VIN, VOUT	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1
TSTG	Storage Temperature	-55 to +100	°C	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indi-cated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

DDR4-2666U Speed Bins

Speed Bin		DDR4-2666U		Unit
CL - nRCD - nRP		19-19-19		
Parameter	Symbol	min	max	
Internal read command to first data	t_{AA}	13.75	18.00	ns
Internal read command to first data with read DBI enabled	t_{AA_DBI}	tAA(min) + 3nCK	tAA(max) +3nCK	ns
ACT to internal read or write delay time	t_{RCD}	13.75	-	ns
PRE command period	t_{RP}	13.75	-	ns
ACT to PRE command period	t_{RAS}	32	9 x tREFI	ns
ACT to ACT or REF command period	t_{RC}	45.75	-	ns

Module Dimensions